2023

Semiconductor Wafer
Test Asia Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

Thursday, November 2

8:00 – 17:00	Attendee Registration Check-In
8:00 – 10:00	Exhibitor Registration Check-In
8:00 – 9:30	Exhibitor Setup in EXPO Hall
8:45 – 9:00	Chairman's Welcome
9:00 – 10:00	Keynote 1
10:00 – 10:30	Tea Break in EXPO Hall
10:00 – 15:30	EXPO Open
10:30 – 12:00	Session 1 – New Probe MFG
12:00 – 14:00	Lunch
12:25 – 13:45	Tech Showcase 1-3
14:00 – 15:30	Session 2 – Electrical Challenge
15:30 – 16:00	Tea Break in EXPO Hall
15:35 – 15:55	Tech Showcase 4
16:00 – 17:30	Session 3 – AI in Probing Tech
17:30 – 18:30	Welcome Reception in EXPO Hall

Friday, November 3

8:00 – 17:00	Attendee Registration Check-In
8:45 – 9:00	Friday Program Intro
9:00 – 10:00	Keynote 2
10:00 – 10:30	Tea Break in EXPO Hall
10:15 – 10:25	Tech Showcase 5
10:00 – 16:00	EXPO Open
10:30 – 12:00	Session 4 – Marketing & Innovation
12:00 – 14:00	Lunch
12:25 – 13:45	Tech Showcase 6-8
14:00 – 15:30	Session 5 – KGD Technology
15:30 – 16:00	Tea Break in EXPO Hall
15:35 – 15:55	Tech Showcase 9
16:00 – 17:00	Session 6 – AI in Probing Tech
17:00 – 17:15	Awards for Best Presentations
17:15 – 19:00	Taiwan Street Food Festival

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November 2, 2023 (Thursday)	
8:45 – 10:00	**Welcome and Keynote 1**
8:45 – 9:00	**Welcome Address for SWTest Asia 2023** Jerry BROZ, PhD, SWTest General Chair (Delphon – USA)
9:00 – 10:00	**KEYNOTE 1** **Advanced Electronic Heterogeneous Integration and Testing** **Wei-Chung LO, PhD** *Deputy General Director* ***Electronic and Optoelectronic System Research Laboratories (EOSL)*** ***Industrial Technology Research Institute (ITRI)*** **Abstract:** Next wave of semiconductor is going to be two major trends, one is feature size scaling (more Moore) and the other is system scaling/heterogeneous integration (More than Moore). The presentation is to share the key aspects of future applications in semiconductor era: High frequency (Beyond 5G or 6G), High speed/HPC (AI chips or High-performance computing) and High power applications. We believe that the semiconductor IC will keep the momentum to speed up the market-oriented research and development to fulfill the domain needs of smart living, quality of life and sustainable environment by adopting advanced semiconductor technology. The up-to-date results and development of WBG semiconductor (eg. GaN & SiC) as well as Si-based advance AI-related devices based on heterogeneous integration (side- by-side or 3D stacking) will be highlighted. The challenge of testing multiple dies through the limited interconnect will also be discussed including but not limited to the new test board, equipment, and methodologies. **Biography:** Dr. Wei-Chung (Robert) Lo is currently the Deputy General Director of Electronic and Optoelectronic System Research Laboratories (EOSL). Dr. Lo joined Industrial Technology Research Institute to work in advanced electronic packaging, such as WLP, 3D IC/3D stacking, fan-out, heterogeneous integration technology for more than 20 years, 85 papers and 40 patents granted. Dr. Lo received his MS and PhD degrees from National Taiwan University and is an alumnus of the University of Pennsylvania Wharton Business School AMP program. Dr. Lo serves as TWG chair of IoT Chapter of IEEE Heterogenous Integration Roadmap (HIR). He has been actively involved with IEEE and iMAPS working with various Interconnect Committees. Currently, he is the Chairman of International Microelectronics Assembly and Packaging Society (IMAPS)-Taiwan Chapter and is the Co-Chair of SEMI Packaging and Test committee as well as a Tech Consultant/Committee member of TPCA.

Wei-Chung LO, PhD

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November 2, 2023 (Thursday)	
10:00 – 10:30	**Tea Break in EXPO Hall**
10:30 – 12:00	**SESSION 1: New Probe MFG** **Session Chair: Eric CHIA-CHANG (Intel – USA)**
10:30 – 11:00	**Characteristics of The New Pd-based Alloy for Probe-pins, TK-FS, which has three unique features: High Hardness/High Electrical Conductivity/High Ductility** Takeshi FUSE, Kunihiro SHIMA, and Takeyuki SAGAE (TANAKA KIKINZOKU KOGYO K.K. -Japan)
11:00 – 11:30	**Application of MD (Molecular Dynamics) methodology in the development and verification of advanced MEMS materials for future wafer probe cards** Young Jun PARK, Jin-Wook JANG, Sang Dan KIM, Song Ho KIM, In Suk LEE, Joon Young CHOI (Korea Instrument - South Korea), Changhyun CHO, Joonyeon KIM (Samsung Electronics - South Korea)
11:30 – Noon	**Cutting Cost and Resolution Enabled by Novel Photonic Technologies for Next-Generation Probe Cards Manufacturing** Ksenija VARGA and Thomas UHRMANN (EV Group – Austria)
12:00 – 14:00	**LUNCH (Tech Showcase 1 – 3)**
14:00 – 15:30	**SESSION 2: Electrical Challenge** **Session Chair: Alan FERGUSON (Oxford Lasers - UK)**
14:00 – 14:30	**Contact Resistance Application in Parametric Testing** Iwan KURNIAWAN, Kar Loong LOW and Thiam Seng YIP (Micron Semiconductor Asia Pte. Ltd. – Singapore)
14:30 – 15:00	**SiC, GaN and more: Probing Technologies for HV/HC Power Devices** Rainer GAGGL (T.I.P.S. Messtechnik GmbH – Austria)
15:00 – 15:30	**Current Carrying Capacity Maximization in Probe Cards And the Path to An Unburnable Probe** Hadi NAJAR (Form Factor Inc. – USA)
15:30 – 16:00	**Tea Break in EXPO Hall (Tech Showcase 4)**

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November 2, 2023 (Thursday)	
16:00 – 17:30	**SESSION 3: AI in Probing Tech** **Session Chair: Muru MEYYAPPAN (Marvell Technology - USA)**
16:00 – 16:30	**Seamless ATE test program generation using a ML approach – Multi-label classification** SenthilKumar DHAMODHARAN, Vaishnavi SARAVANAN, Dinesh ARIVALAGAN, and Lavanya RAJU (Caliber Interconnect Solutions Pvt Ltd – India)
16:30 – 17:00	**Probes Cleaning Effectiveness challenges for fine pitch and high density Logic Probe Cards with MEMS tips** WENJUNG CHANG (Micron – Taiwan)
17:00 – 17:30	**Probe Card Maintenance with Artificial Intelligence Assistance System** Adolph CHENG, Ying-Jen CHEN and Anthony FAN (MPI Corporation – Taiwan) Jia-Yu PENG and Prof. Chen-Fu CHIEN (AIMS Research Center, NSTC – Taiwan)
17:30 – 18:30	**Welcome Reception in EXPO Hall**

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November 3, 2023 (Friday)	
8:45 – 10:00	**Intro and Keynote 2**
8:45 – 9:00	**Friday Program Intro** Jerry BROZ, PhD, SWTest General Chair (Delphon – USA)
9:00 – 10:00	**KEYNOTE 2** **Wafer in, SSD out – Famous Last Words of a Test engineer to Manufacturing: "Test All Bits!"** **Pradip GHIMIRE** *Vice President of Memory Product Solutions* ***Western Digital, Inc.*** **Abstract:** 3D NAND technology has made significant advancements, progressing from only a few cell layers to today's impressive 3D skyscraper-like designs with hundreds of layers. This allows rapid growth in bit density, gross die per wafer and large flash capacity enablement from mobile phones to data centers and reduce the overall cost of the product so the world can store more data at a reasonable cost. The technology advancement has also created an immense complexity in how we do manufacturing test from wafer level all the way to the final SSD product, which is a crucial process to ensure product quality and customer compliance. However, it also drives to higher CapEx investment, longer cycle time, increased factory space requirement, and yield loss. The industry is adapting multi-dimensional approaches to overcome these challenges. During this keynote address, we will explore into the future of factory automation, sustainability, and the advantage of vertically integrated model from wafer-in to SSD-out. We will delve into the challenges faced in future high-volume NAND manufacturing testing and share our proactive approach to address these challenges through talented Engineers. **Biography:** Pradip Ghimire believes there is a tremendous value creation at the intersection of technology development and high-volume manufacturing through Engineering innovations. Over the past 20 plus years, Pradip has been at the forefront of leading NAND, ASIC, and DRAM based products from technology definition to high volume manufacturing. Currently, he serves as the Vice President of Memory Product Solutions at Western Digital, responsible for NAND productization and manufacturing testing for entire WD flash product portfolio. Pradip has held leadership positions at Micron and SanDisk in product Engineering prior to Western Digital.

Pradip GHIMIRE

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	Biography (cont.) Pradip holds a Bachelor's Degree in Electrical Engineering from Montana State University. He has completed Stanford Executive program and is an alumnus of Stanford Graduate School of Business. During his free time in California, USA, he enjoys reading about philosophy and technology, basketball, and spending time with his family.
10:00 – 10:30	**Tea Break in EXPO Hall (Tech Showcase 5)**
10:30 – 12:00	**SESSION 4: Marketing & Innovation** **Session Chair: Kenny TANG (TSMC Corporation – Taiwan)**
10:30 – 11:00	**3D microprinted probes for testing at sub 20 ¬µm pitch** Wabe KOELMANS, Sam LIN, Anita HUANG, Angus WANG, Edgar HEPP, Francesco COLANGELO, Patrik SCHÜRCH (Exaddon AG – Switzerland)
11:00 – 11:30	**Silicon Photonic On-Wafer Test** Choon Leong LOU and Ban Ban LIM (STAr Technologies, Inc. – Taiwan), Soon Leng TAN and Wei Liang SIO (CompoundTek Pte Ltd – Singapore)
11:30 – Noon	**Probe Card Market Dynamics and Cost of Test Analysis** Panchami Divakar PHADKE (TechInsights – USA)
12:00 – 14:00	**LUNCH (Tech Showcase 6 – 8)**
14:00 – 15:30	**SESSION 5: KGD Technology** **Session Chair: Alex YANG (MPI Corporation - Taiwan)**
14:00 – 14:30	**Waveform consideration of shared driver** Shoichi MATSUO (Micron Memory Japan Inc. – Japan)
14:30 – 15:00	**AMT 5000: KGD Testing at the Die Level Optimized for HBM** Calvin PARK (AMT. CO. LTD. – South Korea)
15:00 – 15:30	**KGD 56G PAM4 High Speed Testing for data center product – Setup Stability Improvement at Wafer Sort** Wei Hoong YAP (Marvell Technology Inc. – Singapore)
15:30 – 16:00	**Tea Break in EXPO Hall**

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16:00 – 17:00	**SESSION 6: High Speed Challenge** **Session Chair: Joey WU (SWTest Conference - Taiwan)**
16:00 – 16:30	**High Speed Probe Card architecture for High End Devices** Alberto BERIZZI, Alice GHIDONI, Xin-Reng FOO, Chee-Hoe LIN, Ivan GIUDICEANDREA, Giancarlo BRIVIO, Raffaele VALLAURI (Technoprobe – Italy)
16:30 – 17:00	**Complex Impedance Matching Structures for Advanced On–Wafer AiP Testing** Pratik GHATE (FormFactor, Inc – USA)
17:00 – 17:15	**Awards for Best Presentations** Jerry BROZ, PhD, SWTest General Chair (Delphon – USA)
17:15 – 19:00	**Taiwan Street Food Festival in Chapel and Gardens**