SWTEST ASIA

PROBE TODAY, FOR TOMORROW

2023 CONFERENCE

Conference eProceedings

November 2 to 3, 2023
Sheraton Hsinchu Hotel
Zhubei City, Taiwan

SWTest Asia 2023

Welcome to Beautiful Taiwan!

Hello SWTest Asia 2023 Attendees!

On behalf of the SWTest Team it is our great pleasure to welcome you to SWTest Asia 2023 Conference and EXPO at the Sheraton in Hsinchu, Taiwan. We are extremely pleased to be back once again at the beautiful Sheraton Hsinchu Hotel in Zhubei City, Taiwan.

At SWTest Asia, we create a friendly environment for attendees to learn about industry innovations and connect face-to-face with colleagues, top suppliers, and service providers. The SWTest EXPO and Technology Showcase feature key suppliers from around the globe that are integral to the support of wafer probe industry. Throughout the program, we schedule many opportunities for networking in a relaxed setting.

We thank all our conference sponsors (9-platinum, 8-gold, and 6-silver), the 40 industry exhibitors, and the committee members as well as the volunteers that make SWTest Asia such a valuable event for the Asian wafer test industry. We want to welcome the Fukuoka Prefecture Visitor Bureau, who are introducing our attendees to Fukuoka City, which will be the site for SWTest Asia 2024 held October 24 to 26, 2024, at the Hilton Seahawk Hotel.

SWTest Asia events "kicked-off" on Wednesday with the Sponsors and Exhibitors Golf Tournament at the Royal Kuan-Hsi Golf Club. This terrific benefit tournament promotes relaxed discussions, networking, and supports the funding behind our student travel grant awards.

On Thursday morning, our Visionary Keynote Speaker will be Dr. Wei-Chung (Robert) Lo, Deputy General Director Electronic and Optoelectronic System Research Laboratories (EOSL) for the Industrial Technology Research Institute (ITRI). Dr. Lo will explore key aspects for the future mega-trends and applications needed in the accelerating semiconductor era. After the Visionary Keynote, the Thursday Technical Program will have three focused sessions, the EXPO will be open during most of the day, and the popular "Sponsor's Tech Showcase" will feature presentations from Platinum Sponsors (that do not conflict with the technical session schedule). Following the Technical Program, we will have a hosted reception held in the Expo Hall.

On Friday morning, our second Visionary Keynote Speaker will be Mr. Pradip Ghimire, Vice President of Memory Product Solutions at Western Digital, Inc. Mr. Ghimire will explore the future of factory automation, sustainability, and the advantage of a vertically integrated model from wafer-in to SSD-out as well as delve into the challenges faced in high-volume NAND manufacturing. After the Visionary Keynote, the Friday Technical Program will consist of three focused sessions, the EXPO will be open during most of the day, and the "Sponsor's Tech Showcase" will continue. Once the conference adjourns, we will have a hosted "Taiwan Street Food Festival" in the Hotel Chapel Courtyard.

Thank you for being a part of the SWTest Asia Conference and EXPO in 2023.

Jerry Broz, PhD
General Chair
SWTest Conferences

Clark Liu
Taiwan Program Chair
SWTest Asia

Rey Rincon
Technical Program
SWTest Conferences

Maddie Harwood
Finance Chair
SWTest Conferences

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HTSI Hermes Testing Solutions Inc.

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PROGRAM SCHEDULE

Thursday, November 1

	Thursday, November 2nd, 2023		
	Technical Sessions	EXPO	Tech Showcase
8:00		Exhibitor Move-in	
8:45	Welcome address		
9:00	Keynote Speaker 1		
9:30			
10:00	Break	EXPO open	
10:30	Session 1: New Probe MFG		
11:00			
11:30			
12:00	Lunch		
12:30			Tech Showcase 1-3
13:00			
13:30			
14:00	Session 2: Electrical Challenge		
14:30			
15:00			
15:30	Break		Tech Showcase 4
16:00	Session 3: AI in Probing Tech		
16:30			
17:00			
17:30		Welcome Reception in EXPO Hall	
18:00			
18:30			

Friday, November 2

	Friday, November 3rd, 2023		
	Technical Sessions	EXPO	Tech Showcase
8:00			
8:45	Friday Program Intro		
9:00	Keynote Speaker 2		
9:30			
10:00	Break	EXPO open	Tech Showcase 5
10:30	Session 4: Marketing & Innovation		
11:00			
11:30			
12:00	Lunch		
12:30			Tech Showcase 6-8
13:00			
13:30			
14:00	Session 5: KGD Technology		
14:30			
15:00			
15:30	Break		Tech Showcase 9
16:00	Session 6: High Speed Challenge	Exhibitor Move-out	
16:30			
17:00	Awards		
17:15		Taiwan Street Festival	
17:30			
18:00			
18:30			
19:00			

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SPONSOR TECH SHOWCASE

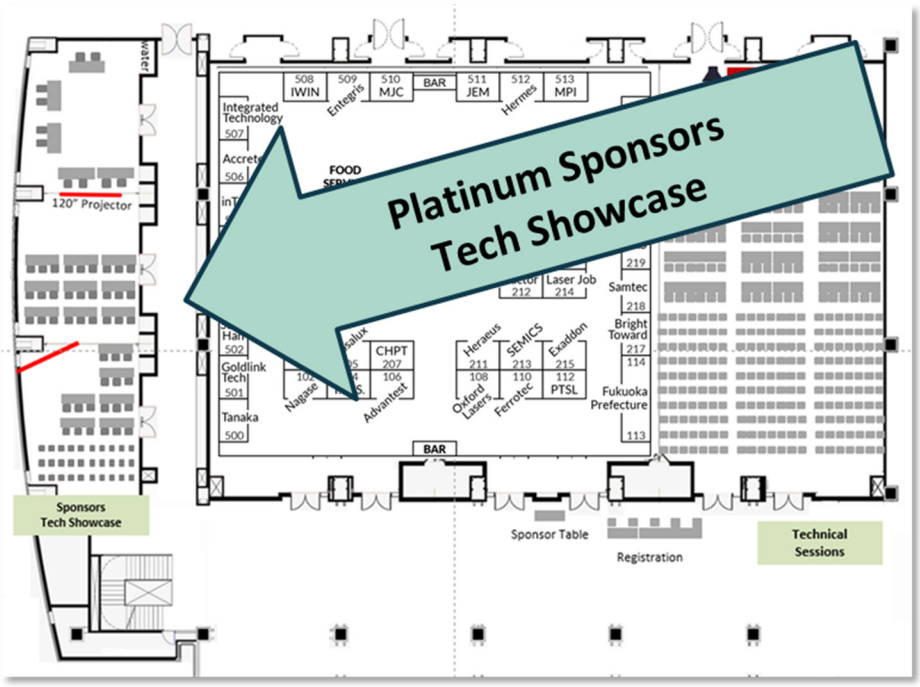
Platinum Sponsor Tech Showcase

Thursday, November 2

- **Tech Showcase #1**
  12:25 – 12:45
  PTSL
- **Tech Showcase #2**
  12:55 – 13:15
  Gel-Pak
- **Tech Showcase #3**
  13:25 – 13:45
  Teradyne
- **Tech Showcase #4**
  15:35 – 15:55
  Oxford Laser

Friday, November 3

- **Tech Showcase #5**
  10:05 – 10:25
  Technoprobe
- **Tech Showcase #6**
  12:25 – 12:45
  CHPT
- **Tech Showcase #7**
  12:55 – 13:15
  STAr Technologies
- **Tech Showcase #8**
  13:25 – 13:45
  Taiwan MJC



2023

Semiconductor Wafer Test Asia Conference

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PROGRAM SCHEDULE

Program Overview

SWTest Asia 2023 conference is a probe technology forum where attendees come to learn about recent developments in the industry and exchange ideas. SWTest Asia attracts attendees from the local and regional semiconductor industry to include ASE, TSMC, Ardentec, KYEC, SPIL, Micron, ChipMOS, UMC, Winbond, PTI, and more. Due to quarantine restrictions, a limited number of international attendees from Japan, Korea, Singapore, Philippines, and Malaysia. Conference registration includes all meals, refreshments, social activities, technical program, EXPO, and the eProceedings. There is very friendly atmosphere with Technical Sessions, an EXPO, and a Tech Showcase in a relaxed environment for networking.

November 1, 2023 (Thursday)

8:45 – 10:00	Welcome and Keynote 1
8:45 – 9:00	**Welcome Address for SWTest Asia 2023** Jerry BROZ, PhD, SWTest General Chair (Delphon – USA)
9:00 – 10:00	**KEYNOTE 1** **Advanced Electronic Heterogeneous Integration and Testing** **Wei-Chung LO, PhD** *Deputy General Director* ***Electronic and Optoelectronic System Research Laboratories (EOSL)*** ***Industrial Technology Research Institute (ITRI)*** **Abstract:** Next wave of semiconductor is going to be two major trends, one is feature size scaling (more Moore) and the other is system scaling/heterogeneous integration (More than Moore). The presentation is to share the key aspects of future applications in semiconductor era: High frequency (Beyond 5G or 6G), High speed/HPC (AI chips or High-performance computing) and High power applications. We believe that the semiconductor IC will keep the momentum to speed up the market-oriented research and development to fulfill the domain needs of smart living, quality of life and sustainable environment by adopting advanced semiconductor technology. The up-to-date results and development of WBG semiconductor (eg. GaN & SiC) as well as Si-based advance AI-related devices based on heterogeneous integration (side- by-side or 3D stacking) will be highlighted. The challenge of testing multiple dies through the limited interconnect will also be discussed including but not limited to the new test board, equipment, and methodologies. **Biography:** Dr. Wei-Chung (Robert) Lo is currently the Deputy General Director of Electronic and Optoelectronic System Research Laboratories (EOSL). Dr. Lo joined Industrial Technology Research Institute to work in advanced electronic packaging, such as WLP, 3D IC/3D stacking, fan-out, heterogeneous integration technology for more than 20 years, 85 papers and 40 patents granted.

Wei-Chung LO, PhD

	Biography (cont.) Dr. Lo received his MS and PhD degrees from National Taiwan University and is an alumnus of the University of Pennsylvania Wharton Business School AMP program. Dr. Lo serves as TWG chair of IoT Chapter of IEEE Heterogenous Integration Roadmap (HIR). He has been actively involved with IEEE and iMAPS working with various Interconnect Committees. Currently, he is the Chairman of International Microelectronics Assembly and Packaging Society (IMAPS)-Taiwan Chapter and is the Co-Chair of SEMI Packaging and Test committee as well as a Tech Consultant/Committee member of TPCA.

November 1, 2023 (Thursday)	
10:00 – 10:30	**Tea Break in EXPO Hall**
10:30 – 12:00	**SESSION 1: New Probe MFG** **Session Chair: Eric CHIA-CHANG (Intel – USA)**
10:30 – 11:00	**Characteristics of The New Pd-based Alloy for Probe-pins, TK-FS, which has three unique features: High Hardness/High Electrical Conductivity/High Ductility** Takeshi FUSE, Kunihiro SHIMA, and Takeyuki SAGAE (TANAKA KIKINZOKU KOGYO K.K. -Japan)
11:00 – 11:30	**Application of MD (Molecular Dynamics) methodology in the development and verification of advanced MEMS materials for future wafer probe cards** Young Jun PARK, Jin-Wook JANG, San Dan KIM, Song Ho KIM, In Seok LEE, Jun Young CHOI, C.H. CHO, J.Y. KIM (Korea Instrument – South Korea)
11:30 – Noon	**Cutting Cost and Resolution Enabled by Novel Photonic Technologies for Next-Generation Probe Cards Manufacturing** Ksenija VARGA and Thomas UHRMANN (EV Group – Austria)
12:00 – 14:00	**LUNCH (Tech Showcase 1 – 3)**
14:00 – 15:30	**SESSION 2: Electrical Challenge** **Session Chair: Alan FERGUSON (Oxford Lasers - UK)**
14:00 – 14:30	**Contact Resistance Application in Parametric Testing** Kar Loong LOW and Thiam Seng YIP (Micron Semiconductor Asia Pte. Ltd. – Singapore)
14:30 – 15:00	**SiC, GaN and more: Probing Technologies for HV/HC Power Devices** Rainer GAGGL (T.I.P.S. Messtechnik GmbH – Austria)
15:00 – 15:30	**Current Carrying Capacity Maximization in Probe Cards And the Path to An Unburnable Probe** Hadi NAJAR and David RASCHKO (Form Factor Inc. – USA)
15:30 – 16:00	**Tea Break in EXPO Hall (Tech Showcase 4)**

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PROGRAM SCHEDULE

November 1, 2023 (Thursday)	
16:00 – 17:30	**SESSION 3: AI in Probing Tech** **Session Chair: Muru MEYYAPPAN (Marvell Technology - USA)**
16:00 – 16:30	**Seamless ATE test program generation using a ML approach – Multi-Label Classification** SenthilKumar DHAMODHARAN, Vaishnavi SARAVANAN, Dinesh ARIVALAGAN, and Lavanya RAJU (Caliber Interconnect Solutions Pvt Ltd – India)
16:30 – 17:00	**Probes Cleaning Effectiveness challenges for fine pitch and high-density Logic Probe Cards with MEMS tips** WENJUNG CHANG (Micron – Taiwan)
17:00 – 17:30	**Probe Card Maintenance with Artificial Intelligence Assistance System** Adolph CHENG, Ying-Jen CHEN and Anthony FAN (MPI Corporation – Taiwan) Jia-Yu PENG and Prof. Chen-Fu CHIEN (AIMS Research Center, NSTC – Taiwan)
17:30 – 18:30	**Welcome Reception in EXPO Hall**

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Semiconductor Wafer Test Asia Conference

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PROGRAM SCHEDULE

November 2, 2023 (Friday)	
8:45 – 10:00	**Intro and Keynote 2**
8:45 – 9:00	**Friday Program Intro** Jerry BROZ, PhD, SWTest General Chair (Delphon – USA)
9:00 – 10:00	**KEYNOTE 2** **Wafer in, SSD out – Famous Last Words of a Test engineer to Manufacturing: "Test All Bits!"** **Pradip GHIMIRE** *Vice President of Memory Product Solutions* ***Western Digital, Inc.*** **Abstract:** 3D NAND technology has made significant advancements, progressing from only a few cell layers to today's impressive 3D skyscraper-like designs with hundreds of layers. This allows rapid growth in bit density, gross die per wafer and large flash capacity enablement from mobile phones to data centers and reduce the overall cost of the product so the world can store more data at a reasonable cost. The technology advancement has also created an immense complexity in how we do manufacturing test from wafer level all the way to the final SSD product, which is a crucial process to ensure product quality and customer compliance. However, it also drives to higher CapEx investment, longer cycle time, increased factory space requirement, and yield loss. The industry is adapting multi-dimensional approaches to overcome these challenges. During this keynote address, we will explore into the future of factory automation, sustainability, and the advantage of vertically integrated model from wafer-in to SSD-out. We will delve into the challenges faced in future high-volume NAND manufacturing testing and share our proactive approach to address these challenges through talented Engineers. **Biography:** Pradip Ghimire believes there is a tremendous value creation at the intersection of technology development and high-volume manufacturing through Engineering innovations. Over the past 20 plus years, Pradip has been at the forefront of leading NAND, ASIC, and DRAM based products from technology definition to high volume manufacturing. Currently, he serves as the Vice President of Memory Product Solutions at Western Digital, responsible for NAND productization and manufacturing testing for entire WD flash product portfolio. Pradip has held leadership positions at Micron and SanDisk in product Engineering prior to Western Digital.

Pradip GHIMIRE

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Semiconductor Wafer Test Asia Conference

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PROGRAM SCHEDULE

November 2, 2023 (Friday)	
	Biography (cont.) Pradip holds a Bachelor's Degree in Electrical Engineering from Montana State University. He has completed Stanford Executive program and is an alumnus of Stanford Graduate School of Business. During his free time in California, USA, he enjoys reading about philosophy and technology, basketball, and spending time with his family.
10:00 – 10:30	**Tea Break in EXPO Hall (Tech Showcase 5)**
10:30 – 12:00	**SESSION 4: Marketing & Innovation** **Session Chair: Kenny TANG (TSMC Corporation – Taiwan)**
10:30 – 11:00	**3D microprinted probes for testing at sub 20 ¬µm pitch** Wabe KOELMANS, Sam LIN, Anita HUANG, Angus WANG, Edgar HEPP, Francesco COLANGELO, Patrik SCHÜRCH (Exaddon AG – Switzerland)
11:00 – 11:30	**Silicon Photonic On-Wafer Test** Choon Leong LOU and Ban Ban LIM (STAr Technologies, Inc. – Taiwan), Soon Leng TAN and Wei Liang SIO (CompoundTek Pte Ltd – Singapore)
11:30 – Noon	**Probe Card Market Dynamics and Cost of Test Analysis** Panchami Divakar PHADKE (TechInsights – USA)
12:00 – 14:00	**LUNCH (Tech Showcase 6 – 8)**
14:00 – 15:30	**SESSION 5: KGD Technology** **Session Chair: Alex YANG (MPI Corporation - Taiwan)**
14:00 – 14:30	**Waveform consideration of shared driver** Shoichi MATSUO (Micron Memory Japan Inc. – Japan)
14:30 – 15:00	**AMT 5000: KGD Testing at the Die Level Optimized for HBM** Calvin PARK (AMT. CO. LTD. – South Korea)
15:00 – 15:30	**KGD 56G PAM4 High Speed Testing for data center product – Setup Stability Improvement at Wafer Sort** Wei Hoong YAP (Marvell Technology Inc. – Singapore)
15:30 – 16:00	**Tea Break in EXPO Hall (Tech Showcase 9)**

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PROGRAM SCHEDULE

November 2, 2023 (Friday)	
16:00 – 17:00	**SESSION 6: High Speed Challenge** **Session Chair: Joey WU (SWTest Conference - Taiwan)**
16:00 – 16:30	**High Speed Probe Card architecture for High End Devices** Alberto BERIZZI, Alice GHIDONI, Xin-Reng FOO, Chee-Hoe LIN, Ivan GIUDICEANDREA, Giancarlo BRIVIO, Raffaele VALLAURI (Technoprobe – Italy)
16:30 – 17:00	**Complex Impedance Matching Structures for Advanced On–Wafer AiP Testing** Pratik GHATE (FormFactor, Inc – USA)
17:00 – 17:15	**Awards for Best Presentations** Jerry BROZ, PhD, SWTest General Chair (Delphon – USA)
17:15 – 19:00	**Taiwan Street Food Festival in Chapel and Gardens**

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Semiconductor Wafer
Test Asia Conference

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EXPO

SWTest Asia Expo – Exhibitor List

- ACCRETECH
- Advantest
- Bright Toward Ind., Co., Ltd.
- Caliber Interconnects Private Limited
- Celadon Systems, Inc.
- Chain-Logic International Corp.
- Chunghwa Precision Test Tech. Co., Ltd. (CHPT)
- Entegris
- ERS electronic GmbH
- Exaddon AG
- Feinmetall GmbH
- Ferrotec Material Technologies Corporation
- FormFactor Inc.
- Fukuoka Prefecture Visitor Bureau
- Gel-Pak
- Heraeus Deutschland GmbH & Co. KG
- Hermes Testing Solutions Inc.
- HIOKI E.E. CORPORATION
- Integrated Technology Corp.
- inTEST EMS
- IWIN
- JEM Taiwan Probe Corp.
- Laser Job Inc.
- Lincstech Co., Ltd.
- MPI Corporation
- NAGASE (Taiwan) Co., Ltd. – 台灣長瀨股份有限公司
- Nidec SV Probe
- Oxford Lasers
- Posalux SA
- PTSL
- Qualmax Testech Inc.
- Samtec
- SEMICS Inc.
- STAr Technologies, Inc.
- Sung Han Co., Ltd
- T.I.P.S. Messtechnik GmbH
- Taiwan MJC Co., Ltd
- TANAKA Precious Metals – 田中貴金属工業株式会社
- Technoprobe America Inc
- Teradyne
- Zhejiang Goldlink Tech Co.,Ltd

2023
Semiconductor Wafer
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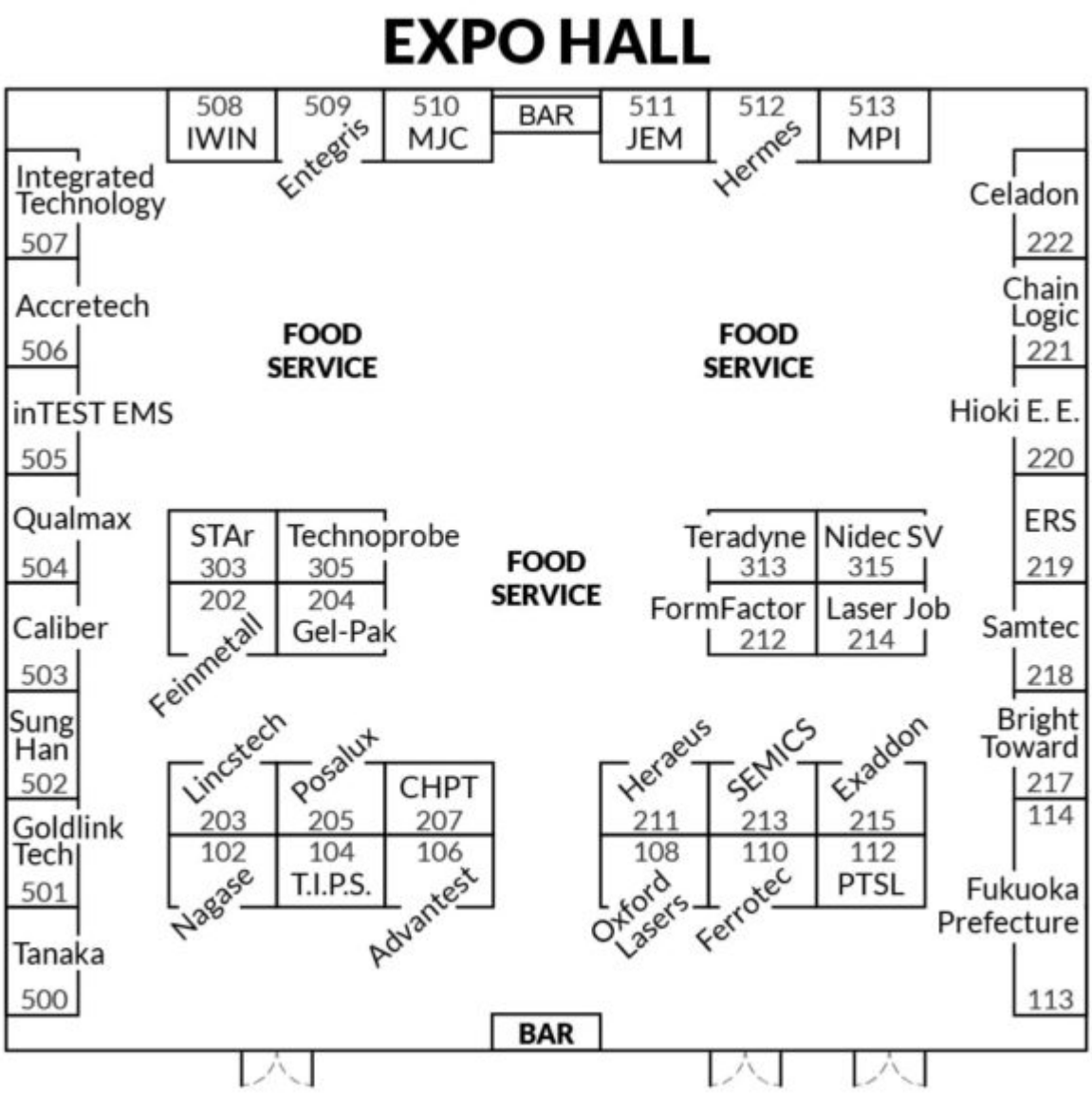
EXPO

SWTest Asia Expo – Exhibitor Map



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SAVE THE DATES

Save the Dates for 2024

SWTest 2024 in San Diego
June 3 to 5, 2024
Omni - La Costa, Carlsbad, CA

SWTest Asia 2024 in Fukuoka, Japan
October 24 to 26, 2024
Hilton Fukuoka Sea Hawk, Fukuoka, Japan

Technical Program
SWTest Asia 2023

4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

Thursday, November 2, 2023

8:45 to 9:00 – Welcome to SWTest Asia

Dr. Jerry Broz (SWTest Asia General Chair) and Clark Liu (SWTest Program Chair)

9:00 to 10:00 – Visionary Keynote Speaker

Advanced Electronic Heterogeneous Integration and Testing

Wei-Chung LO, PhD

Deputy General Director of EOSL

ITRI
Industrial Technology Research Institute

Thursday, November 2, 2023

10:30 to 12:00 – New Probe Manufacturing

Characteristics of The New Pd-based Alloy for Probe-pins, TK-FS: High Hardness/High Electrical Conductivity/High Ductility

Takeshi FUSE, Kunihiro SHIMA, and Takeyuki SAGAE
(TANAKA KIKINZOKU KOGYO K.K. – Japan)

Application of MD (Molecular Dynamics) methodology in the development and verification of advanced MEMS materials for future wafer probe cards

Young Jun PARK, Jin-Wook JANG, San Dan KIM, Song Ho KIM, In Seok LEE, Jun Young CHOI, C.H. CHO, J.Y. KIM (Korea Instrument – South Korea)

Cutting Cost and Resolution Enabled by Novel Photonic Technologies for Next-Generation Probe Cards Manufacturing

Ksenija VARGA and Thomas UHRMANN (EV Group – Austria)

Thursday, November 2, 2023

14:00 to 15:30 – Electrical Challenges

Contact Resistance Application in Parametric Testing

Iwan KURNIAWAN, Kar Loong LOW and Thiam Seng YIP

(Micron Semiconductor Asia Pte. Ltd. – Singapore)

SiC, GaN and more: Probing Technologies for HV/HC Power Devices

Rainer GAGGL (T.I.P.S. Messtechnik GmbH – Austria)

Current Carrying Capacity Maximization in Probe Cards And the Path to An Unburnable Probe

Hadi NAJAR (Form Factor Inc. – USA)

Thursday, November 2, 2023

16:00 to 17:30 – AI in Probing Technologies

Seamless ATE test program generation using a ML approach Multi-label classification

SenthilKumar DHAMODHARAN, Vaishnavi SARAVANAN, Dinesh ARIVALAGAN, and Lavanya RAJU (Caliber Interconnect Solutions Pvt Ltd – India)

Probes Cleaning Effectiveness challenges for fine pitch and high-density Logic Probe Cards with MEMS tips

Wen Jung CHANG (Micron – Taiwan)

Probe Card Maintenance with Artificial Intelligence Assistance System

Adolph CHENG, Ying-Jen CHEN and Anthony FAN (MPI Corporation – Taiwan) Jia-Yu PENG and Prof. Chen-Fu CHIEN (AIMS Research Center, NSTC – Taiwan)

Technical Program
SWTest Asia 2023

Friday, November 3, 2023

Friday, November 3, 2023

8:45 to 9:00 – Welcome to SWTest Asia

Dr. Jerry Broz (SWTest Asia General Chair) and Clark Liu (SWTest Program Chair)

9:00 to 10:00 – Visionary Keynote Speaker

Wafer in, SSD out – Famous Last Words of a Test engineer to Manufacturing: "Test All Bits!"

Pradip GHIMIRE
Vice President
Memory Product Solutions

Western Digital.

Friday, November 3, 2023

10:30 to 12:00 – Innovation and Market

3D microprinted probes for testing at sub 20 ¬µm pitch

Wabe KOELMANS, Sam LIN, Anita HUANG, Angus WANG, Edgar HEPP, Francesco COLANGELO, Patrik SCHÜRCH (Exaddon AG – Switzerland)

Silicon Photonic On-Wafer Test

Choon Leong LOU and Ban Ban LIM (STAr Technologies, Inc. – Taiwan),
Soon Leng TAN and Wei Liang SIO (CompoundTek Pte Ltd – Singapore)

Probe Card Market Dynamics and Cost of Test Analysis

Panchami Divakar PHADKE (TechInsights – USA)

Friday, November 3, 2023

14:00 to 15:30 – KGD Technology

Waveform consideration of shared driver

Shoichi MATSUO (Micron Memory Japan Inc. – Japan)

AMT 5000: KGD Testing at the Die Level Optimized for HBM

Calvin PARK (AMT. CO. LTD. – South Korea)

KGD 56G PAM4 High Speed Testing for data center product – Setup Stability Improvement at Wafer Sort

Wei Hoong YAP (Marvell Technology Inc. – Singapore)

Friday, November 3, 2023

16:00 to 17:00 – High Speed Challenges

High Speed Probe Card architecture for High End Devices

Alberto BERIZZI, Alice GHIDONI, Xin-Reng FOO, Chee-Hoe LIN, Ivan GIUDICEANDREA, Giancarlo BRIVIO, Raffaele VALLAURI (Technoprobe – Italy)

Complex Impedance Matching Structures for Advanced On–Wafer AiP Testing

Pratik GHATE (FormFactor, Inc – USA)

Focusing on a New Challenge within Advanced Vertical Probe Card Guide Plate Drilling

Chris STOKES (Oxford Lasers – UK)

Technical Program
SWTest Asia 2023

Thursday, November 2, 2023

Welcome to the 4th Annual SWTest Asia Taiwan

Jerry Broz, PhD
General Chair, SWTest Asia
Delphon Industries, LLC.

Clark Liu
Technical Program Chair, SWTest Asia
Taiwan MJC Co., Ltd.

It’s Great to Be Back in Taiwan !

SWTEST ASIA

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2023 Conference and Expo

SWTest San Diego and SWTest Asia

34 Years of Combined Probe Technology

12,000+ Attendees have participated from 60+ Countries

1,000+ Technical Podium and Poster Presentations

Repeat Multinational Sponsors and Premier Exhibitors

SWTEST

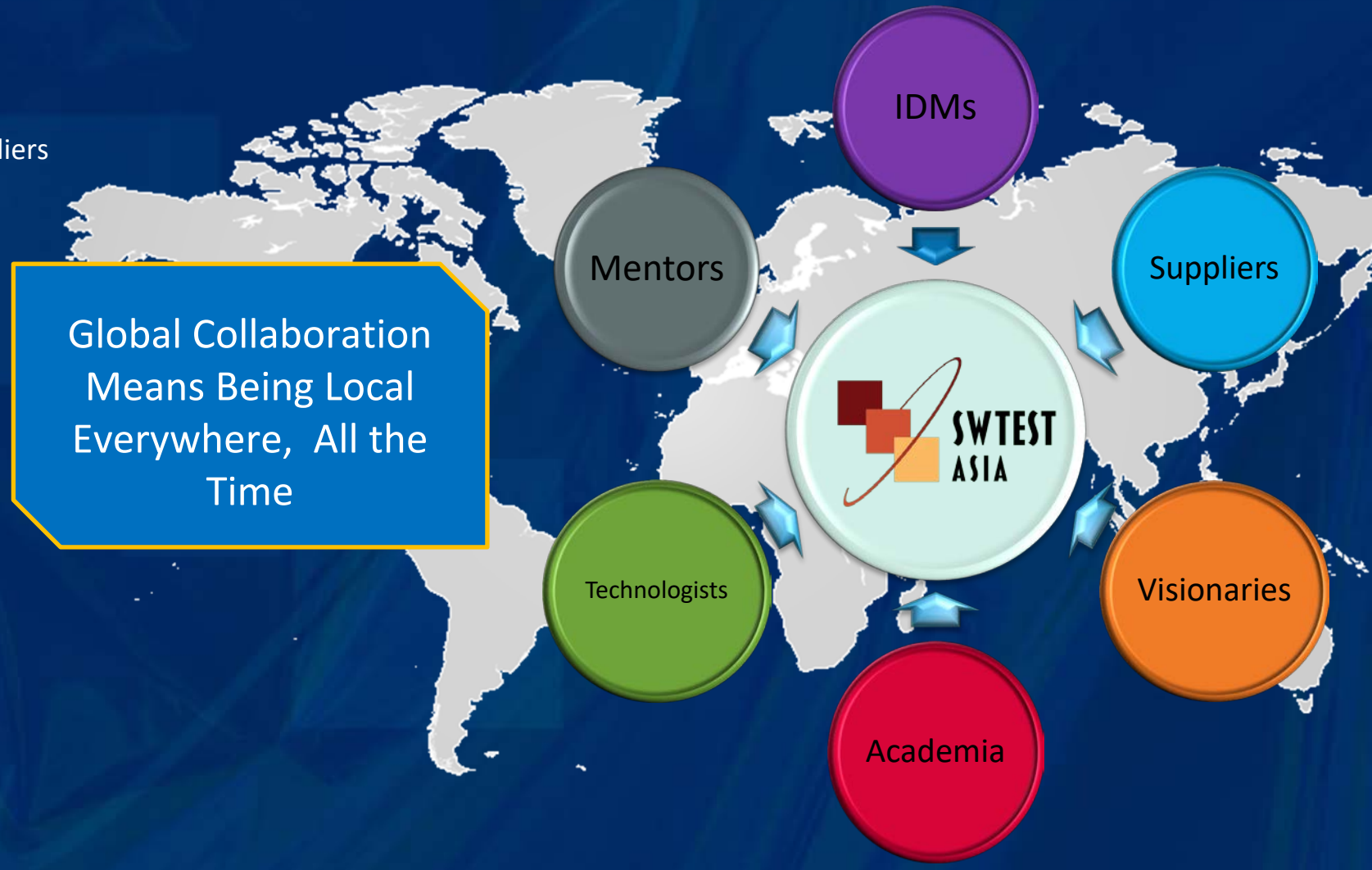
SWTEST ASIA

SWTest US : 1994 to present
SWTest Asia : 2018 to present

SWTest Asia Fosters Collaboration and Growth

- **Wafer Test Technology Forum**
  - Collaborative opportunities for attendees
  - Unique balance of technologists and suppliers
  - Practical solutions to real problems
- **Professional Development**
  - Staying current on recent innovations
  - Focused technical exchange
  - Mentoring and career building
  - Educate the next generation
- **Relaxed Networking**
  - "Workshop Style" environment
  - Build relationships with colleagues
  - Share knowledge and experience
  - Meet new people and have a little fun

Global Collaboration Means Being Local Everywhere, All the Time



Save the Date !

SWTEST ASIA
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2024 Conference and Expo

- **SWTest Asia Japan Program Chair**
  - Nobuhiro Kawamata (Formfactor, K.K.)
- **SWTest Asia Japan Coordinator**
  - Haruko Yoshii (Formfactor, K.K.)

SWTest Asia 2024

October 24 to 26, 2024
Hilton Sea Hawk, Fukuoka, Japan

Message from Fukuoka Prefecture Governor

Seitaro Hattori
Governor
Fukuoka Prefecture

Fukuoka Prefecture

Welcome SWTest Asia 2024 to Fukuoka City

SWTest Asia Chairs and Committee

- **SWTest Executive Team**
  - Jerry Broz, PhD, General Chair (Delphon Industries)
  - Maddie Harwood, Finance Chair / Conference Manager
  - Rey Rincon, Technical Chair (PTSL)
  - Patrick Mui, Technical Co-Chair (JEM America)

- **SWTest Asia Program Chairs**
  - Nobuhiro Kawamata, Japan Program Chair (Formfactor, K.K.)
  - Clark Liu, Taiwan Program Chair (Taiwan MJC)

Held During
Every October
In Asia Region

SWTest Asia is coordinated and executed through the efforts of international colleagues.

SWTest Asia International Steering Committee

- John Caldwell (MJC Electronics Corp.)
- Eric Chia-Cheng Chang, PhD (Intel – USA)
- Alan Ferguson, PhD (Oxford Lasers, Inc. – UK)
- Joonyeon Kim (Samsung – Korea)
- Kuroki Yoichi (Tera Probe – Japan)
- Muru Meyyappan (Marvell Technology – USA)
- Masahide Ozawa (Industrial Advisor – Japan)
- Kenny Tang (TSMC – Taiwan)
- Joey Wu (SWTest Asia Member at Large – Taiwan)
- Alex Yang (MPI Corporation – Taiwan)

SWTest Asia – November 1, 2023

老爺關西高爾夫球場
Royal Kuan-Hsi Golf Club

Student Benefit Golf Tournament
Travel Grants for Students

SWTest Asia 2023 – Day 1 (November 2)

- **Visionary Keynote from Dr. Wei-Chung LO**
  - Deputy General Director of EOSL

- **Technical Program with 3-podium sessions**
  - 1030 – 1200: New Probe Manufacturing
  - 1400 – 1530: Electrical Challenges
  - 1600 – 1730: AI in Probing Technology

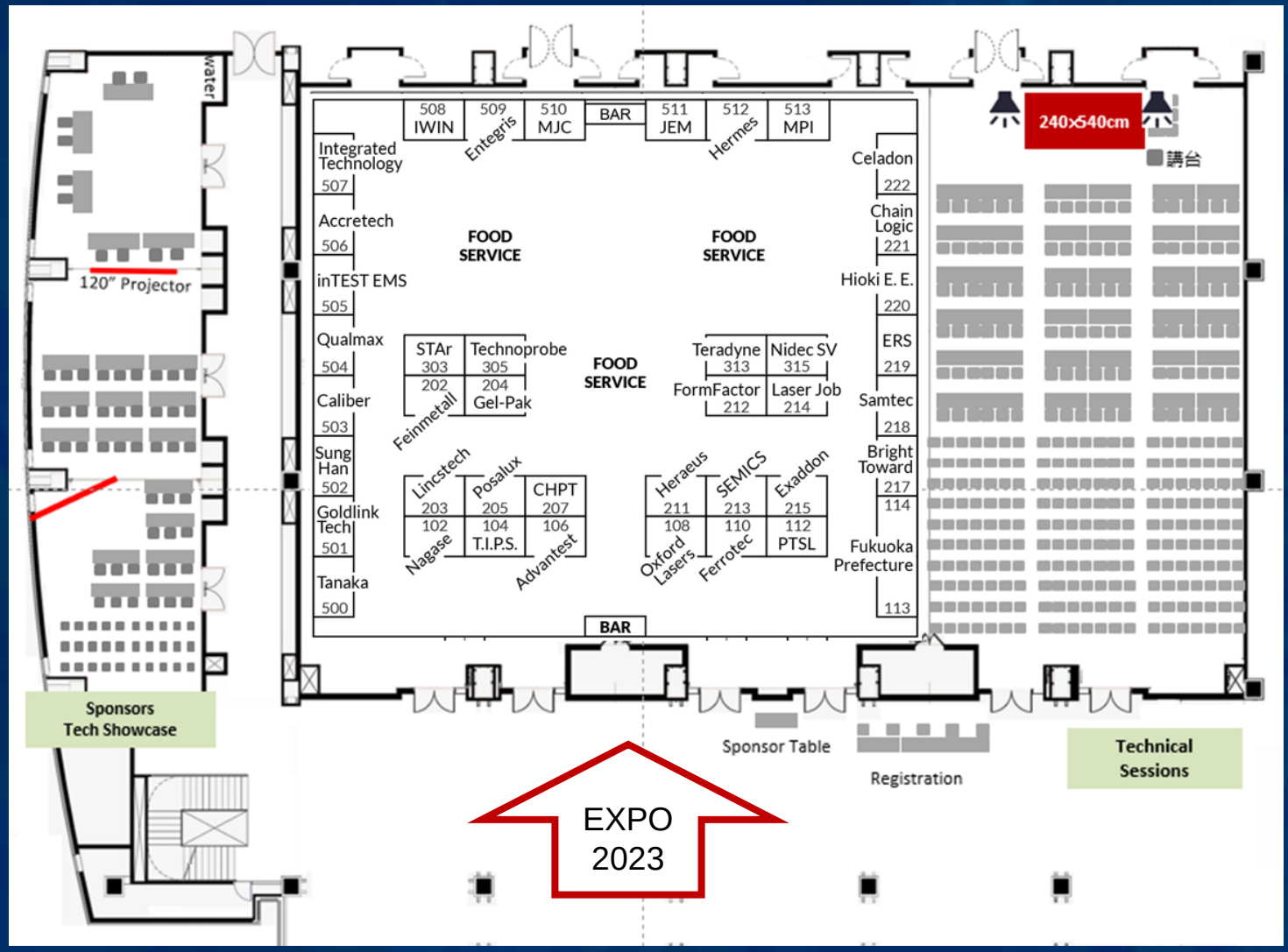
- **SWTest Asia EXPO 2023 with key suppliers**
- **Technology Showcase Presentations by Platinum Sponsors**
- **Welcome Reception in Expo Hall**

SWTest Asia 2023 – Day 2 (November 3)

- **Visionary Keynote from Pradip GHIMIRE**
  - VP of Memory Products at Western Digital

- **Technical Program with 3-podium sessions**
  - 1030 – 1200: Innovation and Marketing
  - 1400 – 1530: KGD Technology
  - 1600 – 1700: High Speed Challenges
  - Awards for “Best Presentations” selected by committee.
- **SWTest Asia EXPO 2023 with key suppliers**
- **Technology Showcase Presentations by Platinum Sponsors**
- **“Taiwan Street Market Celebration” in Sheraton Open Air Courtyard**

Map of the Area



Platinum Sponsors Technology Showcase

Technical Program

SWTest Asia 2023 Conference App

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SWTest Asia 2023

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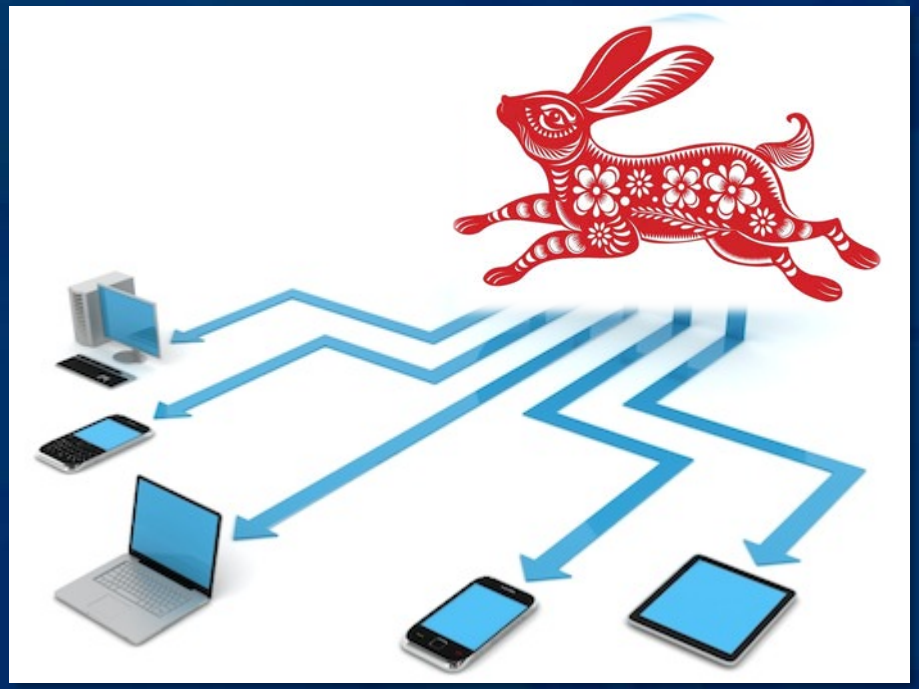
- Up-to-the-minute Event Info
- Connect with the Sponsors and Exhibitors
- Program Schedule in the Auditorium
- View Exhibitor and Sponsor Videos
- Read the Literature from the Exhibitors
- Connect with Attendees that have “opted-in”

SWTest Asia 2023 eProceedings



ePROceedings Password:

rabbit

- Conference e-Version is available for download in a password protected file.
- Free WiFi access will be available during the entire conference to allow attendee access to the downloads.
- Password for the download files will be announced throughout each day and at the registration desk.
- Non-password locked files (including the Keynote presentations) will be made available in the SWTest Asia Archives after the conference adjourns

352 Attendees at SWTest Asia 2022

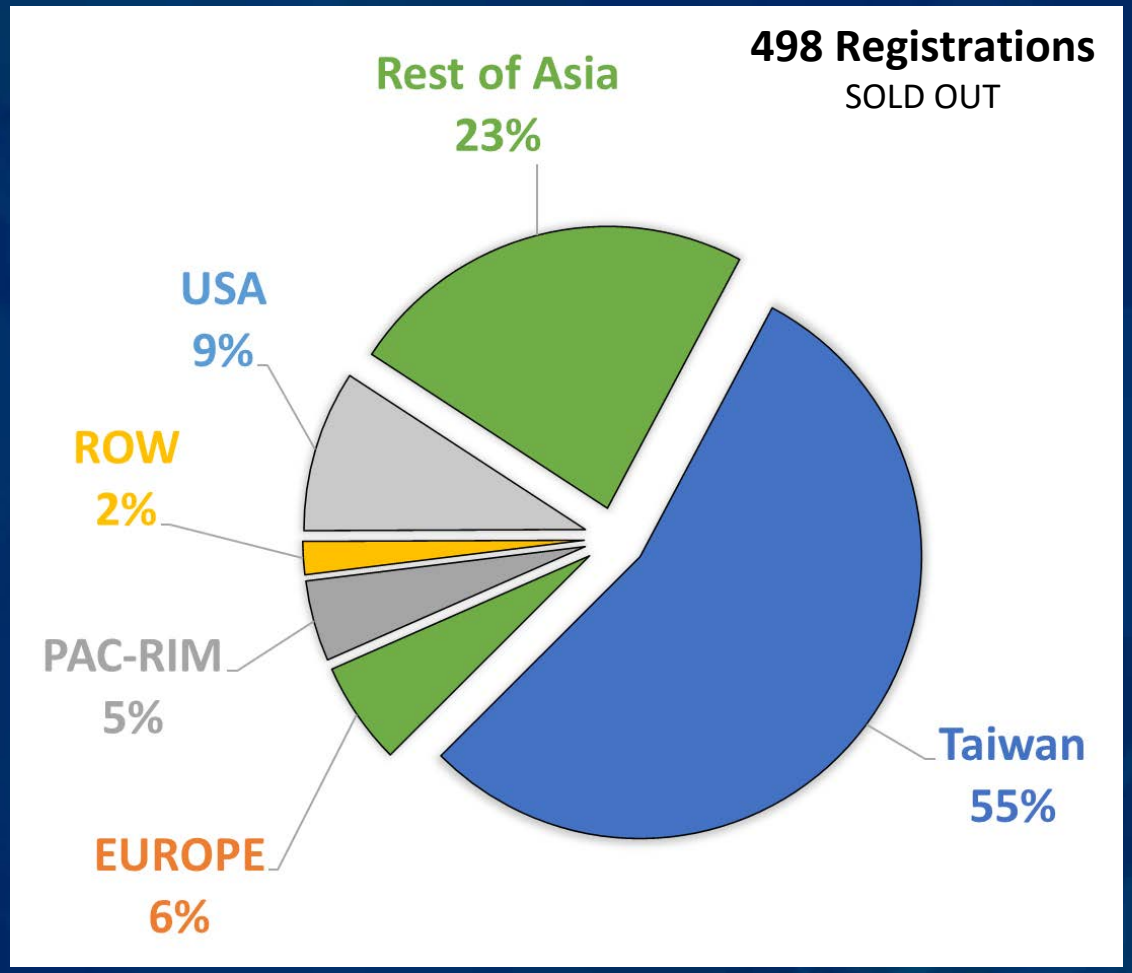
Challenges and Improvement Actions for HPC Wafer Testing

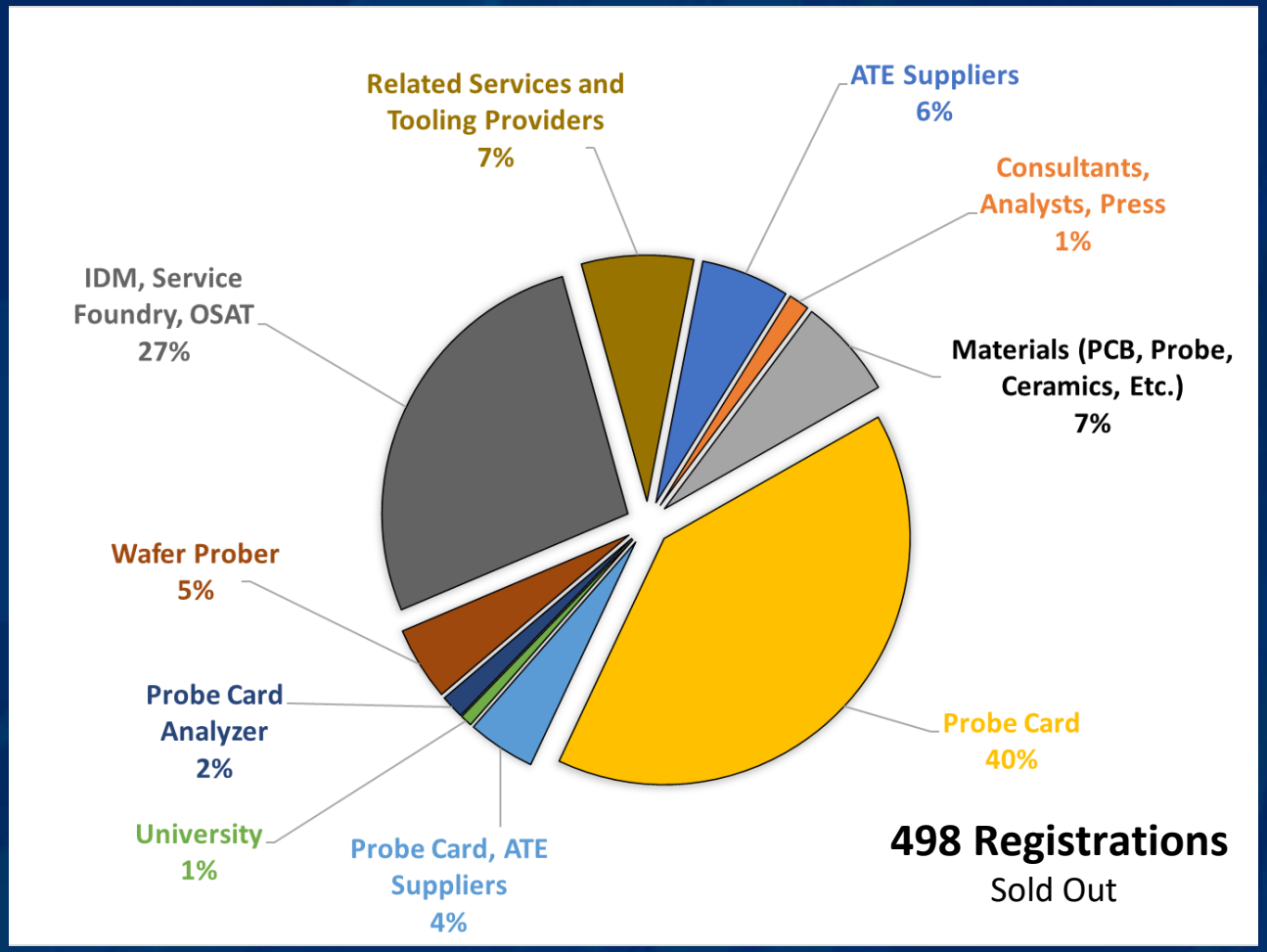
Oscar Lee, Harvey Lin, and Hung Tsai
TSMC – Taiwan

Advanced Testing Technology for Future Requirements

Scott Huang
Kore Semiconductor Co., Ltd. – China

SWTest Asia 2023





Platinum Sponsors (alphabetically)

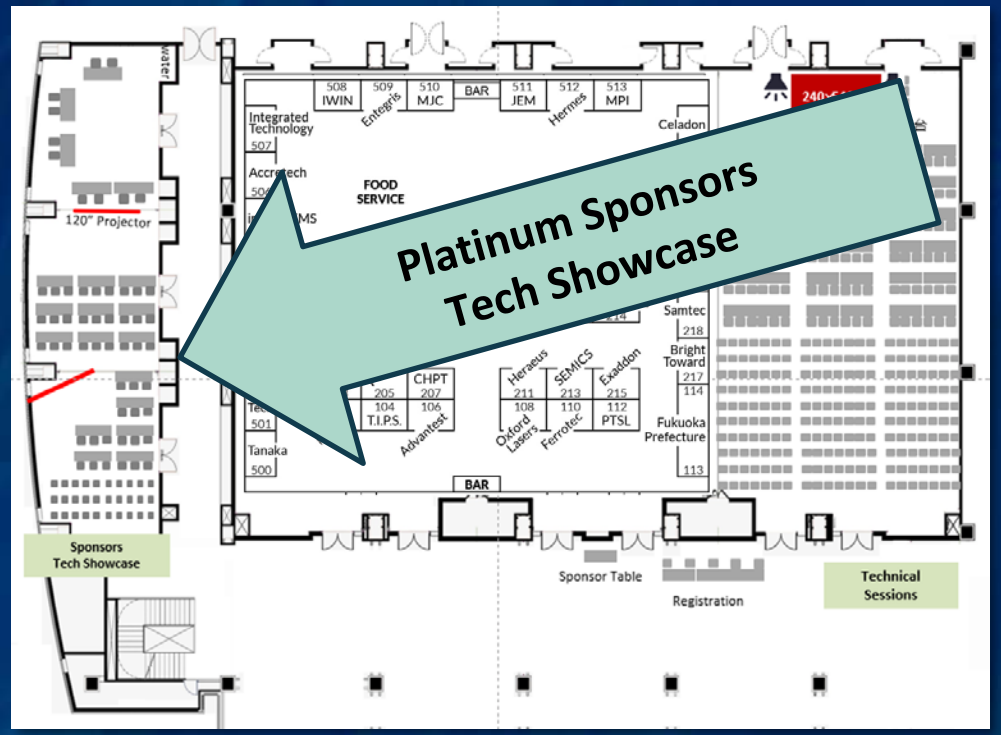
Platinum Sponsor Tech Showcase

Thursday, November 2

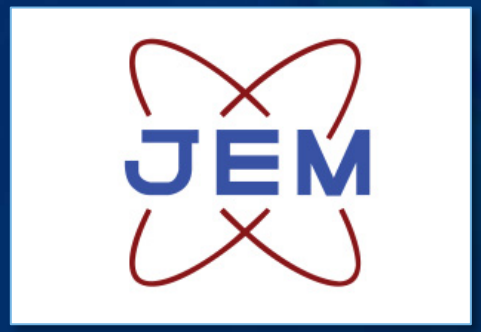
- **Tech Showcase #1**
  12:25 – 12:45
  PTSL
- **Tech Showcase #2**
  12:55 – 13:15
  Gel-Pak
- **Tech Showcase #3**
  13:25 – 13:45
  Teradyne
- **Tech Showcase #4**
  15:35 – 15:55
  Oxford Laser

Friday, November 3

- **Tech Showcase #5**
  10:05 – 10:25
  Technoprobe
- **Tech Showcase #6**
  12:25 – 12:45
  CHPT
- **Tech Showcase #7**
  12:55 – 13:15
  STAr Technologies
- **Tech Showcase #8**
  13:25 – 13:45
  Taiwan MJC



Gold Sponsors (alphabetically)



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- Chain-Logic International Corp.
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- Entegris
- ERS electronic GmbH
- Exaddon AG
- Feinmetall GmbH
- Ferrotec Material Technologies Corporation
- FormFactor Inc.
- Fukuoka Prefecture Visitor Bureau
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- HIOKI E.E. CORPORATION
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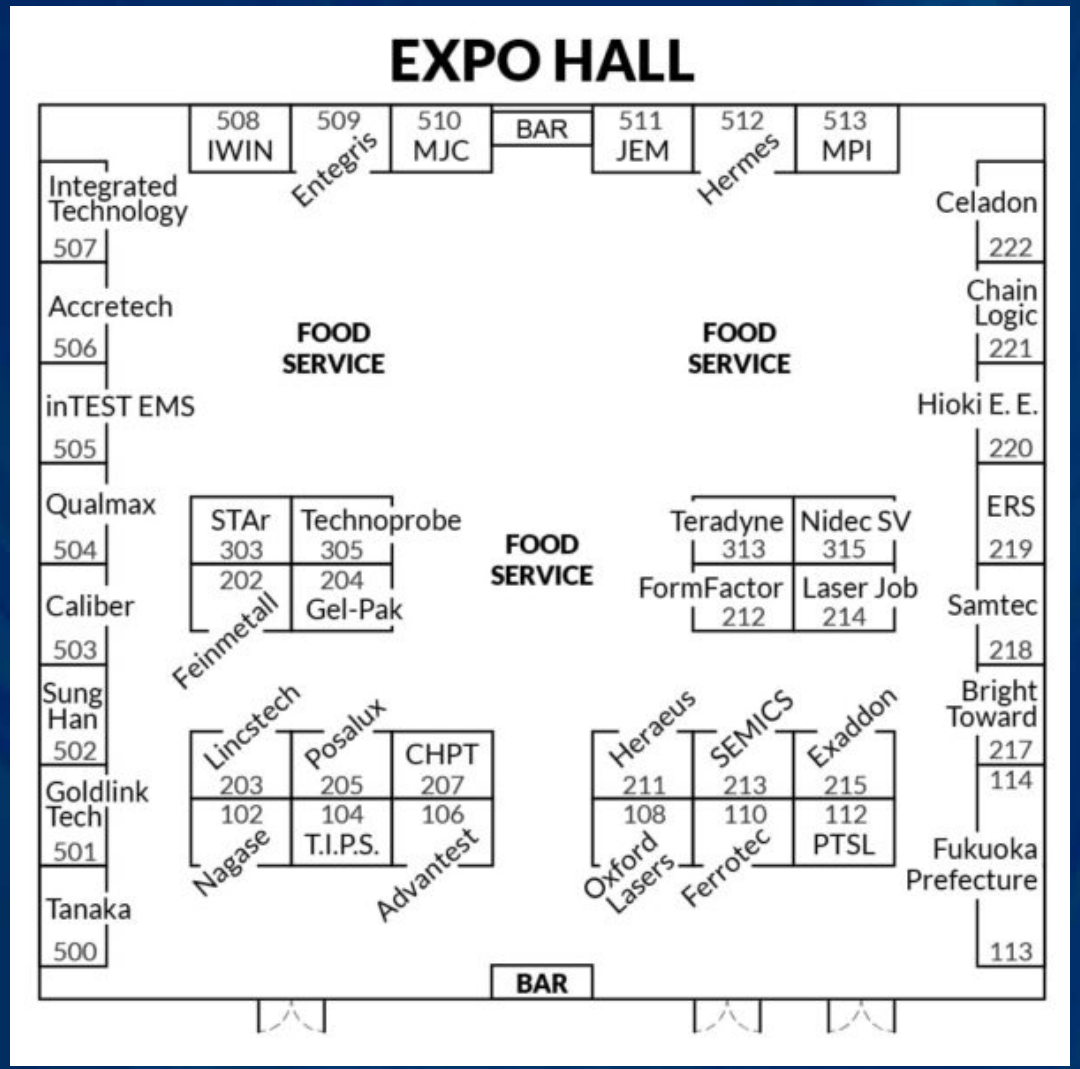
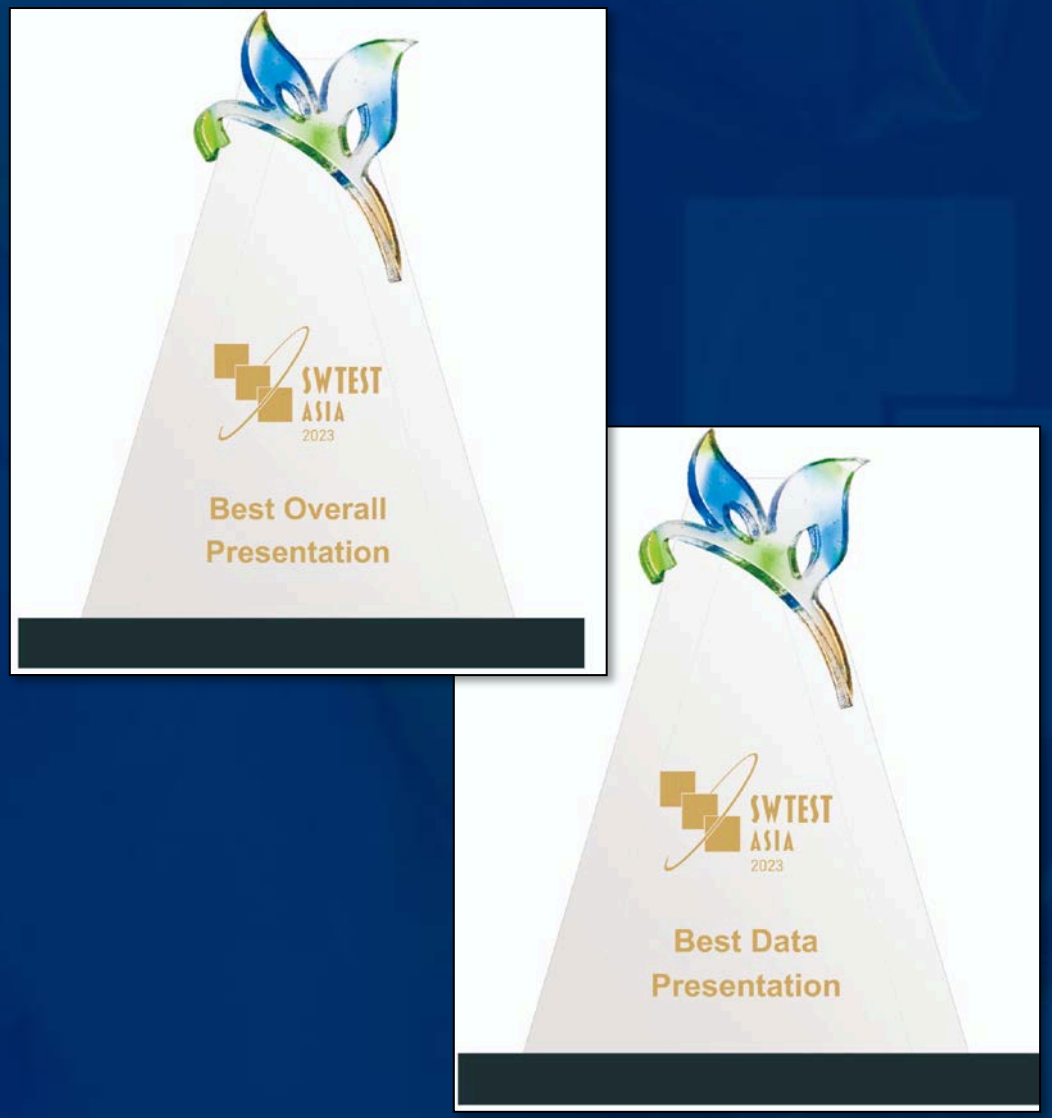
- inTEST EMS
- IWIN



- JEM Taiwan Probe Corp.
- Laser Job Inc.
- Lincstech Co., Ltd.
- MPI Corporation
- NAGASE (Taiwan) Co., Ltd. – 台灣長瀨股份有限公司
- Nidec SV Probe
- Oxford Lasers
- Posalux SA
- PTSL
- Qualmax Testech Inc.
- Samtec
- SEMICS Inc.
- STAr Technologies, Inc.
- Sung Han Co., Ltd
- T.I.P.S. Messtechnik GmbH
- Taiwan MJC Co., Ltd
- TANAKA Precious Metals – 田中貴金属工業株式会社
- Technoprobe America Inc
- Teradyne
- Zhejiang Goldlink Tech Co.,Ltd

Awards



SWTEST ASIA
PROBE TODAY, FOR TOMORROW
2023 Conference and Expo

- **Best Overall Presentation**
- **Best Data Presentation**

Taiwan Street Food Friday Social

Update for 2023 - Save the Dates !

SWTest Asia 2024 will be in Japan !

October 24 to 26, 2024
Hilton Sea Hawk, Fukuoka, Japan

SWTest 2024 will be Back in San Diego !

June 3 to 5, 2024
Omni La Costa, California

Thanks for your Support !

- **Contact the SWTest Asia Team with any questions**

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Characteristics of The New Pd-based Alloy for Probe-pins, TK-FS, which has three unique features: High Hardness/High Electrical Conductivity/High Ductility

Takeshi FUSE
Kunihiro SHIMA, Takeyuki SAGAE

4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

Outline

- ABOUT TANAKA PRECIOUS METALS
- Probe-pins types required in semiconductor manufacturing process
- Characteristics of materials required for each types of Probe-pins
- Characteristics of The New Pd-based Alloy for Probe-pins, TK-FS
- Manufacturing process of TK-FS

ABOUT TANAKA PRECIOUS METALS

Group Network

TANAKA HOLDINGS Co., Ltd.

Strategic and efficient group management and management group companies as the holding company at the center of the TANAKA PRECIOUS METALS.

TANAKA KIKINZOKU KOGYO K.K.

Sales of precious metals (platinum, gold, silver, and others). Manufacture, sales, import and export of various types of industrial precious metals products. Refining and recycling of precious metals.

TANAKA DENSHI KOGYO K.K.

Manufacturing of various holding wires, and provision of technical services globally.

EEJA Ltd.

Development, manufacture, sales and export of precious metal and base metal plating solutions, additives and surface treatment-related chemicals.

Metalor Technologies International SA

Precious metals recovery and refining, production and sales of electrical contacts, and production and sales of plating solutions and plating equipment.

TANAKA KIKINZOKU JEWELRY K.K.

Retailing of gold and platinum jewelry, diamond jewelry, bridal jewelry and precious metals art objects, selling and buying of gold and platinum bullion bars and coins, remodeling and recycling used jewelry (RE:TANAKA).

ABOUT TANAKA PRECIOUS METALS

1885

Started Money Exchange business as "Tanaka Shoten" in Tokyo

2022

680 Billion JPY

Net sales (consolidated)

5,355

Employees (consolidated)

In your hard disk

In your computer

In your cell phone

In influenza diagnosis kits

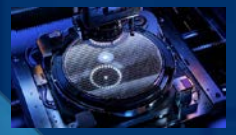
In fuel cell vehicles

Probe-pins types required in semiconductor manufacturing process

Design

Front-end process

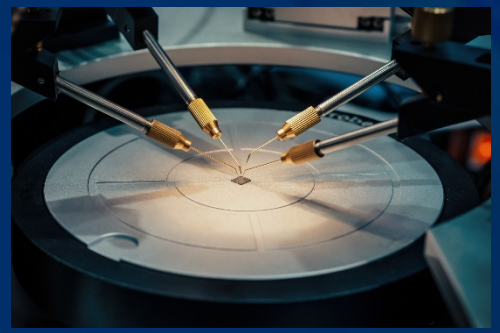
Oxide film/ thin film formation



Resist coating

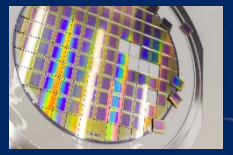
Exposure/ etching

Ion implantation/ wiring formation



Wafer test

Cantilever-type
Vertical-type
Wire-probe



Dicing

Back-end process

Mounting

Bonding

Molding

Final test

Pogo pin Type

Characteristics of materials required for each types of Probe-pins

Cantilever
（Wafer test）

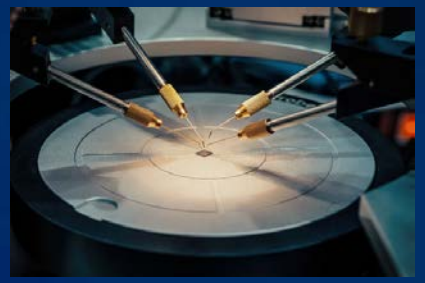
- High Electrical Conductivity
- High Ductility

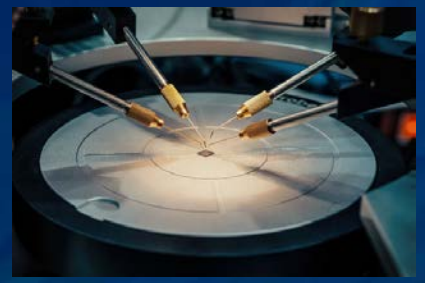
Vertical
（Wafer test）

- High Hardness（Long life）
- High Electrical Conductivity

Pogo pin
（Final test）

- High Hardness（Long life）



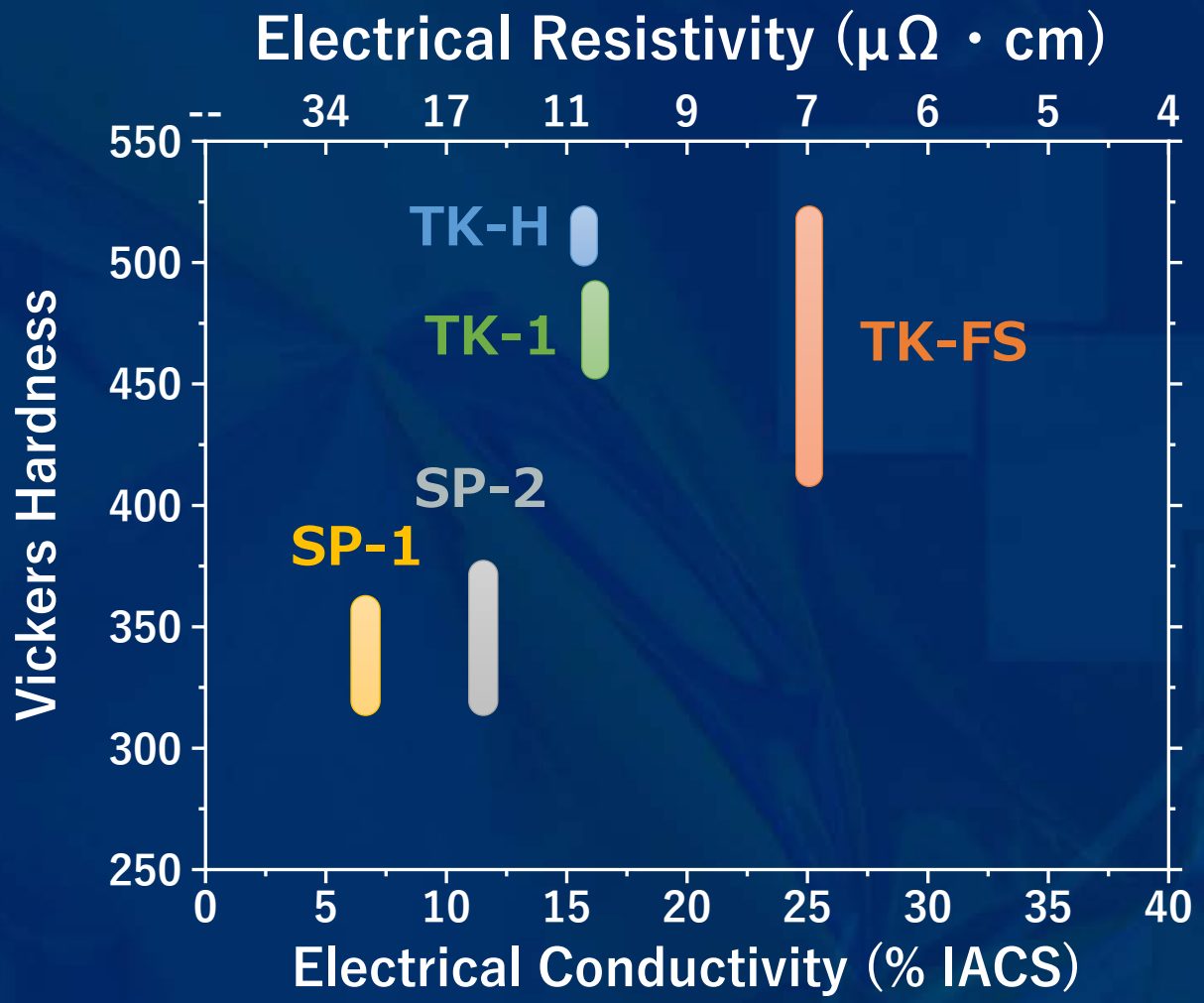


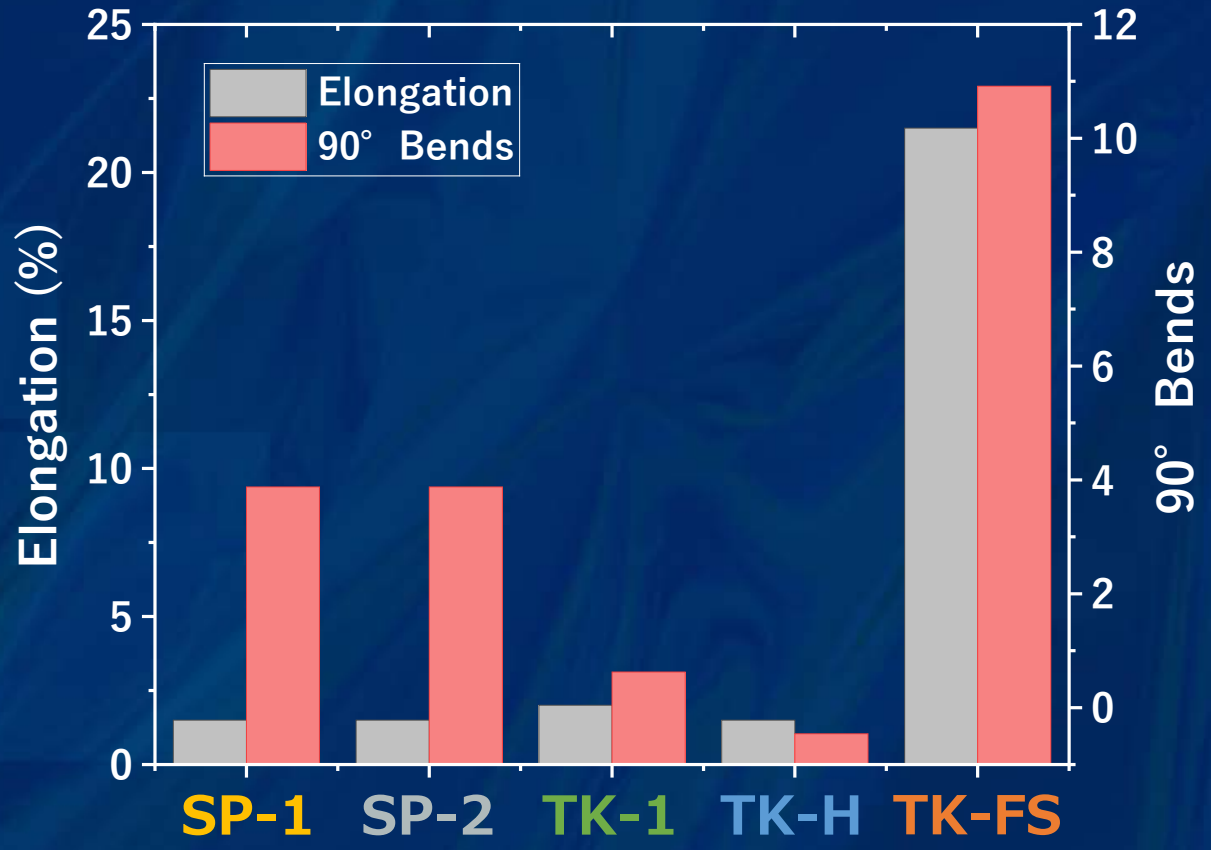
Major Materials for Probe-pins at TANAKA PRECIOUS METALS

	SP-1 (Pd-Ag-Cu-Pt-Au)	SP-2 (Au-Ag-Cu-Pt)	TK-1 (Pd-Ag-Cu)	TK-H (Pd-Ag-Cu)	**TK-FS* (Pd-Ag-Cu)**	Rh*	Ir*
Hardness (HV)	300-350	300-360	460-490	500-520	**400-520**	400-550	500-750
Young's modulus (GPa)	112	106	110	112	**150**	380	530
Electrical Conductivity (%IACS)	6.9	13.3	16.6	16.3	**25-29**	35.9	30.8
Elongation at failure (%)	1-2	1-2	1-3	1-2	**13-30**	1-2	1-2
90° Bends (times)	3-6	3-6	1-2	0-1	**8-14**	-	-

*Patent registered

Comparison of Major Materials for Probe-pins





Characteristics of The New Pd-based Alloy for Probe-pins, "TK-FS"

Conductivity

25-29%IACS

TK-1: 16.6%IACS

Hardness

(**Adjustable widely**)

Max.**520 H V**

～Min. 400HV

TK-1:460-490HV

Ductility

EL: **13-30%**

90°Bends: **8-14**

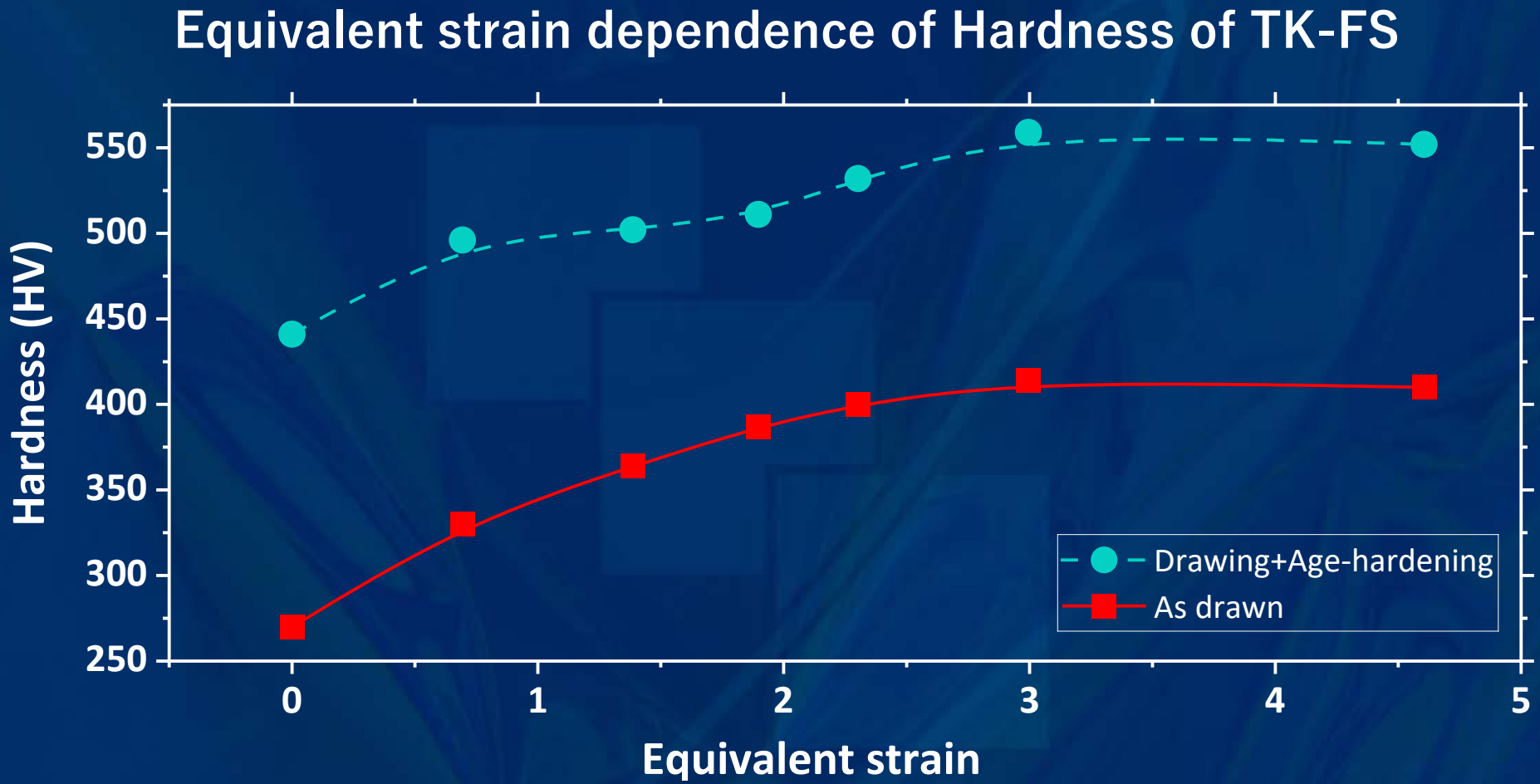
TK-1:

EL: 1-3%

90°Bends: 1-2

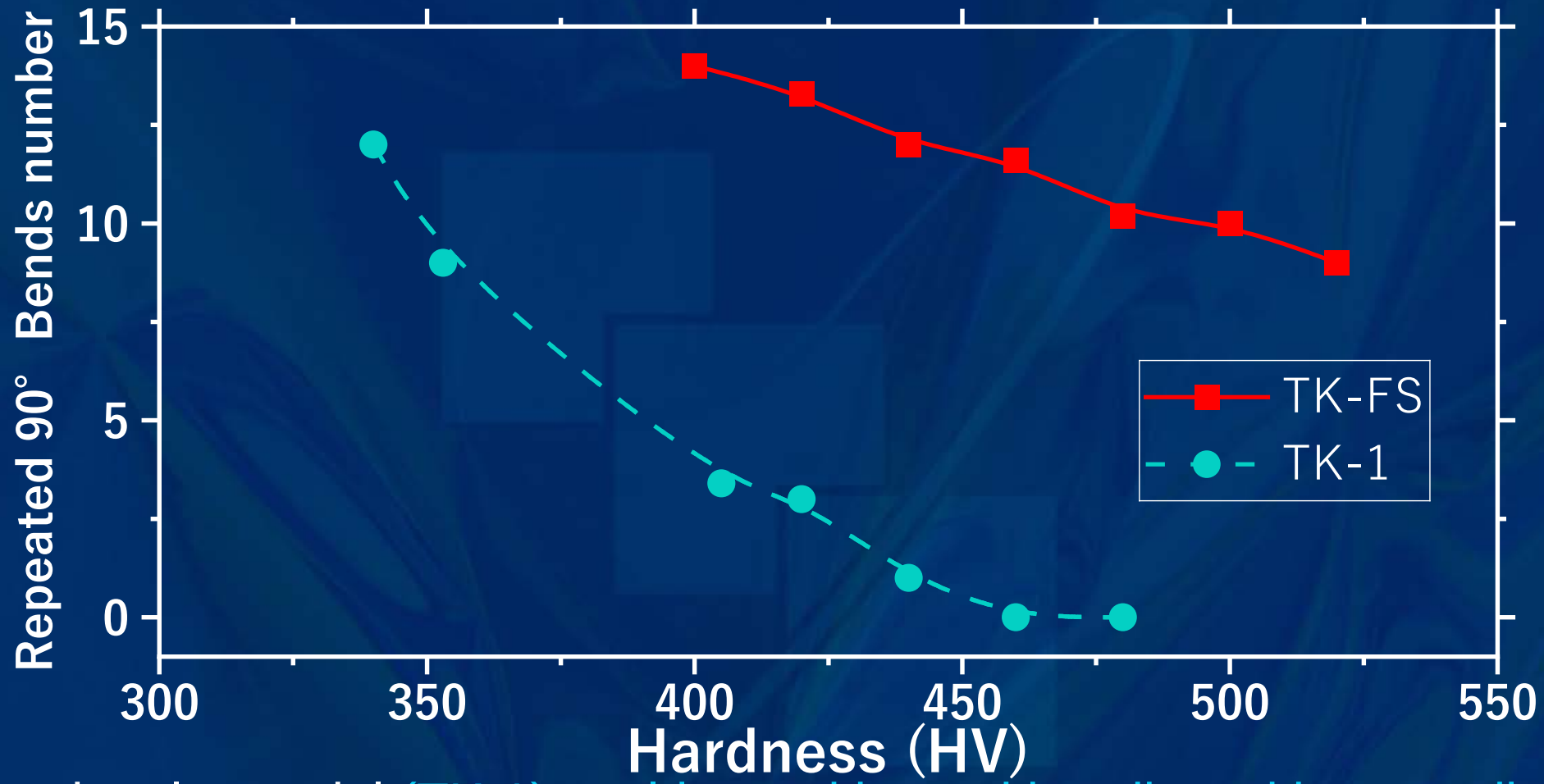
TK-FS can be applied to various types of Probe-pins

Work hardening behavior of “TK-FS”



TK-FS becomes harder with increasing Equivalent strain, saturating in hardness at 3 or higher.

Hardness vs 90° Bends (comparison of “TK-FS” and TK-1)



The conventional material (TK-1) could not withstand bending with exceeding 450HV.
However, TK-FS exhibits **excellent bending durability even over 500HV**.

Wear test

Test Condition

Probe Material: TK-FS/TK-H/TK-1

Probe Dimension: φ0.93mm×16mmL

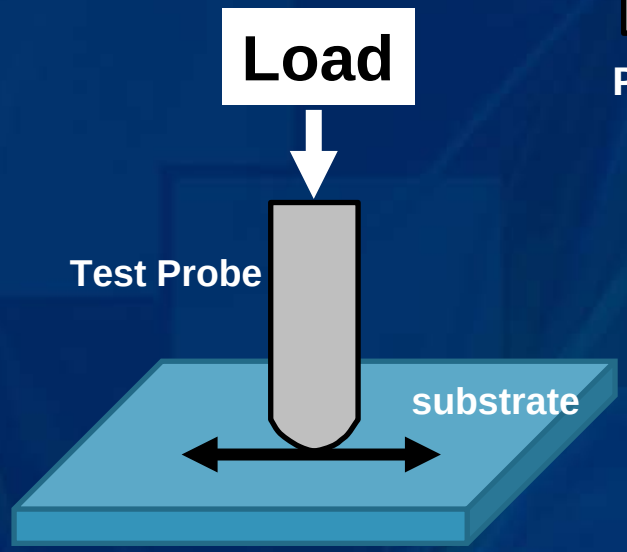
Probe Tip Shape: SR0.03-0.05

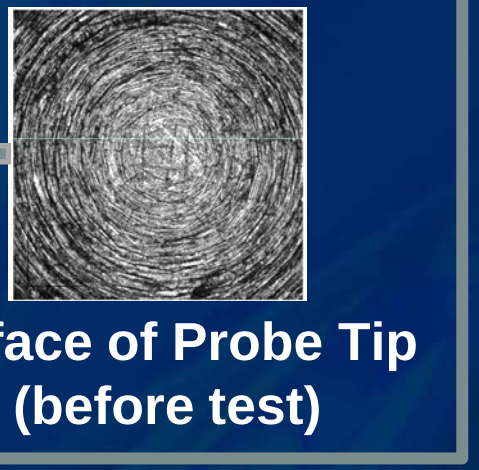
Stroke: About 1mm

Test Speed: 20mm/sec (10Hz)

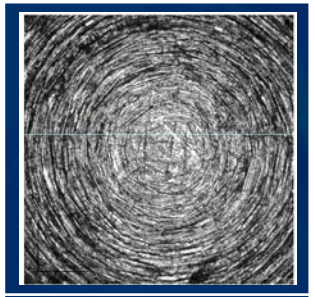
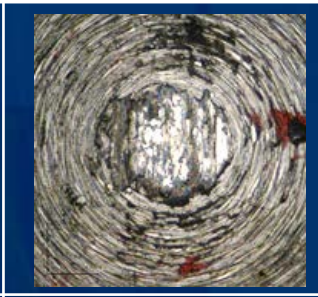
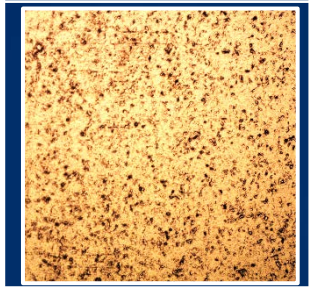
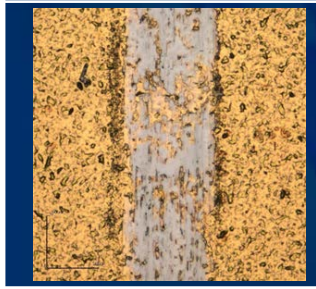
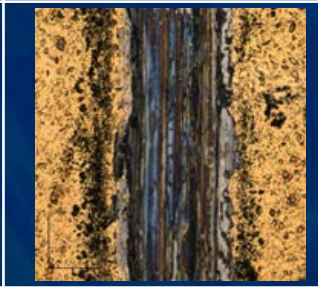
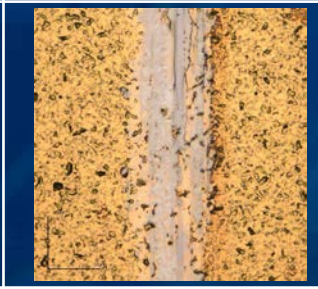
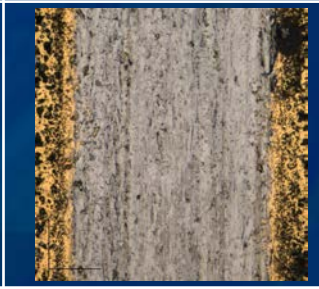
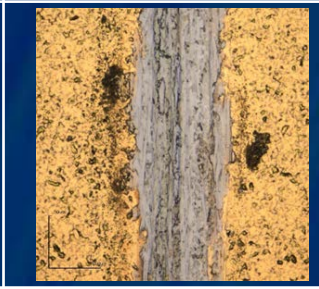
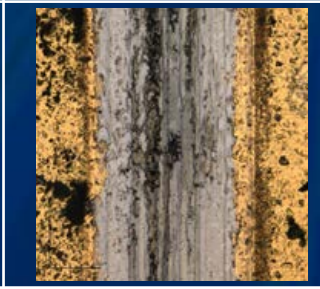
Test Load: 20, 40gf

Test Temperature: R.T.

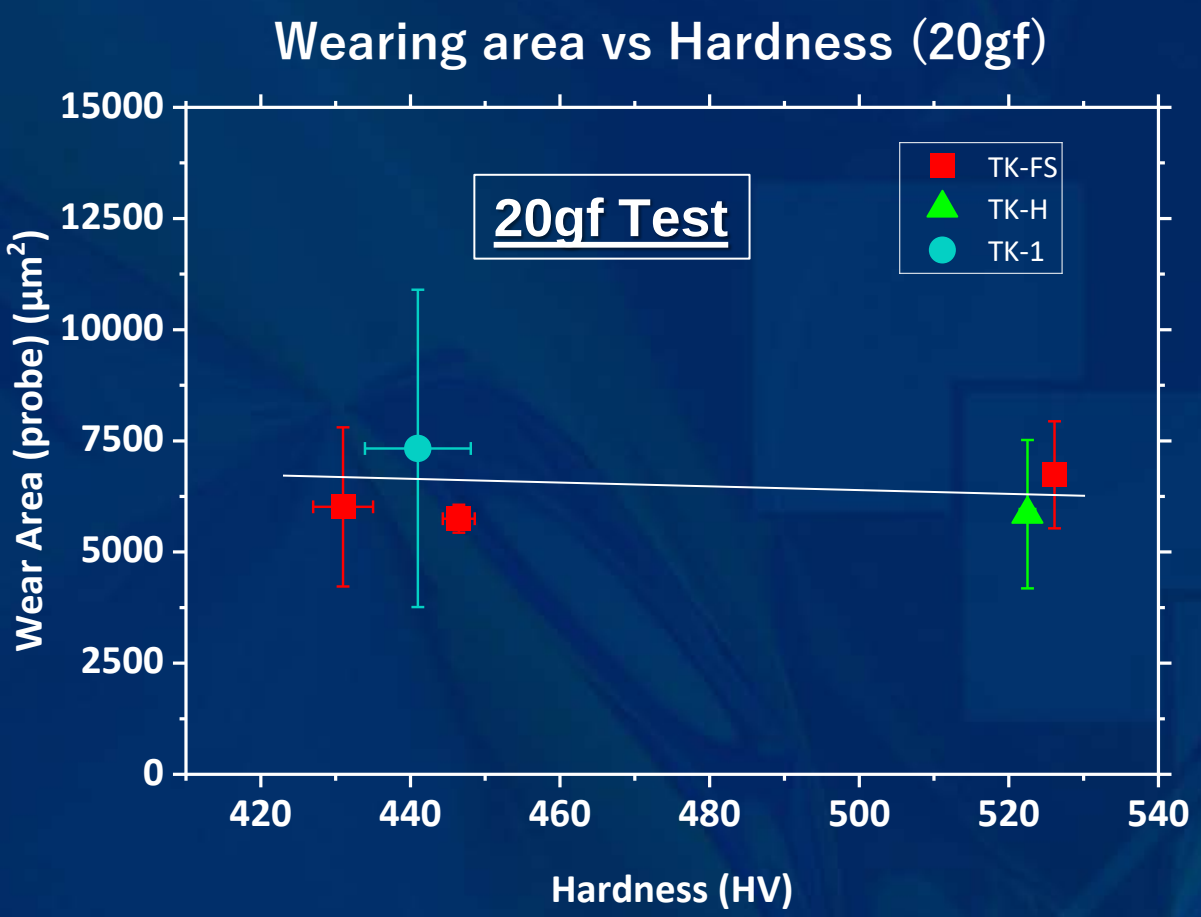


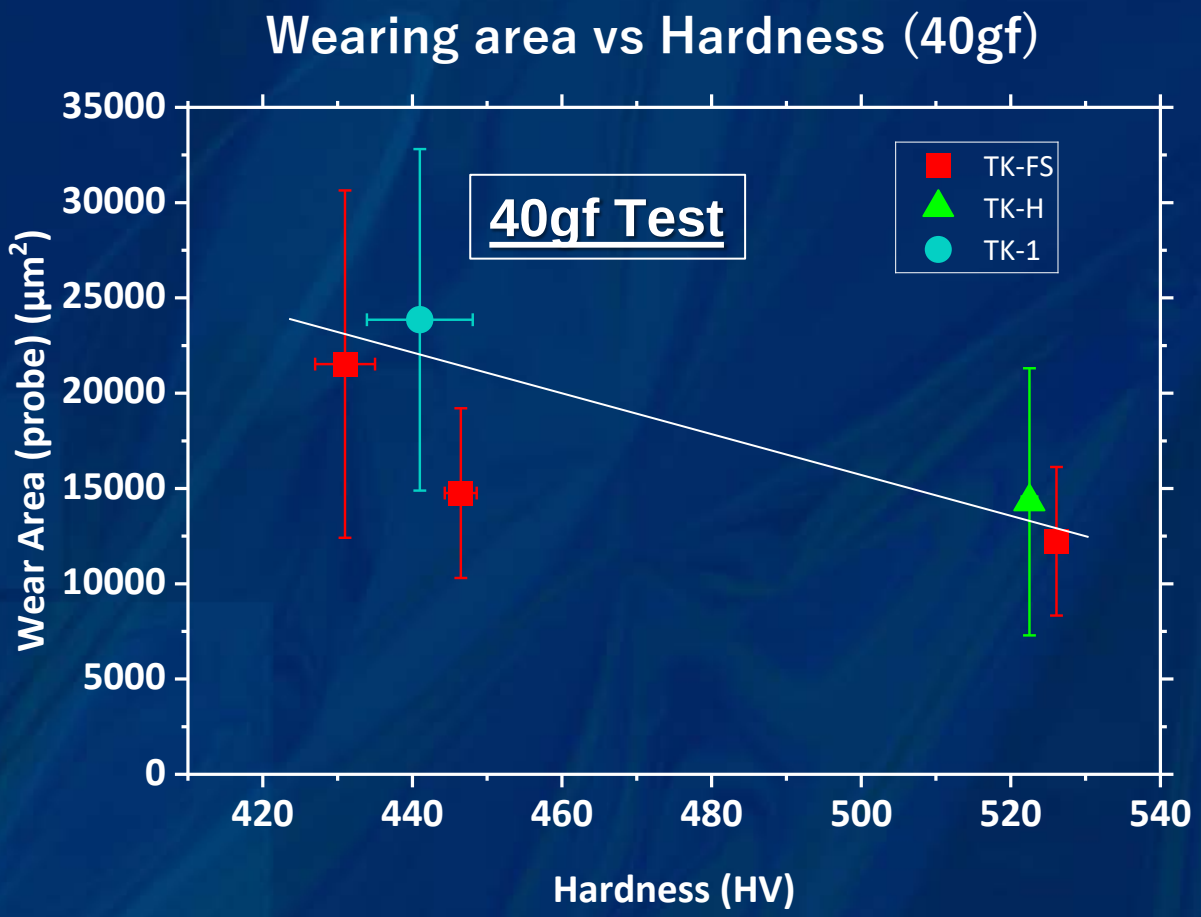


Surface of Probe tip and substrate (before / after test)

	Before	After					
		TK-FS (520HV)		TK-1 (440HV)		TK-H (520HV)	
		20gf	40gf	20gf	40gf	20gf	40gf
Tip							
Substrate							

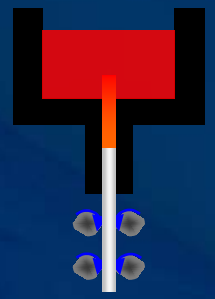
Wearing behavior of Pd-based materials



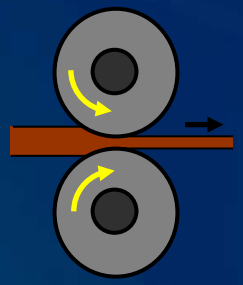


20gf test: Wear area shows almost same, **NOT affected by the hardness** of materials.
40gf test: Wearing area **decreases with increasing the hardness** of materials.

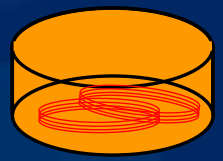
Manufacturing Process of Pd-based materials



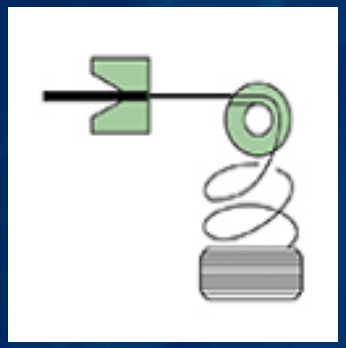
Continuous casting



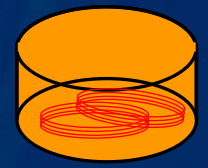
Groove rolling



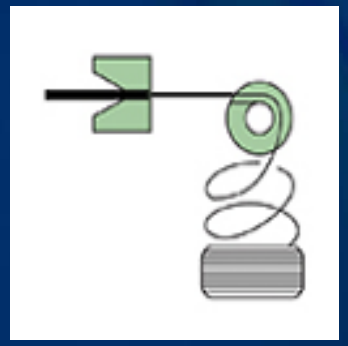
Heat treatment



Drawing



Heat treatment



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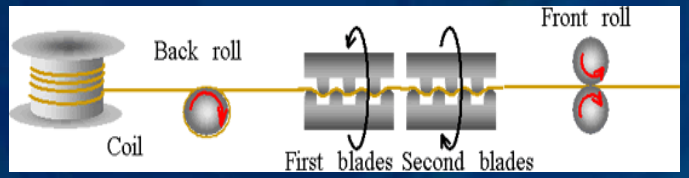
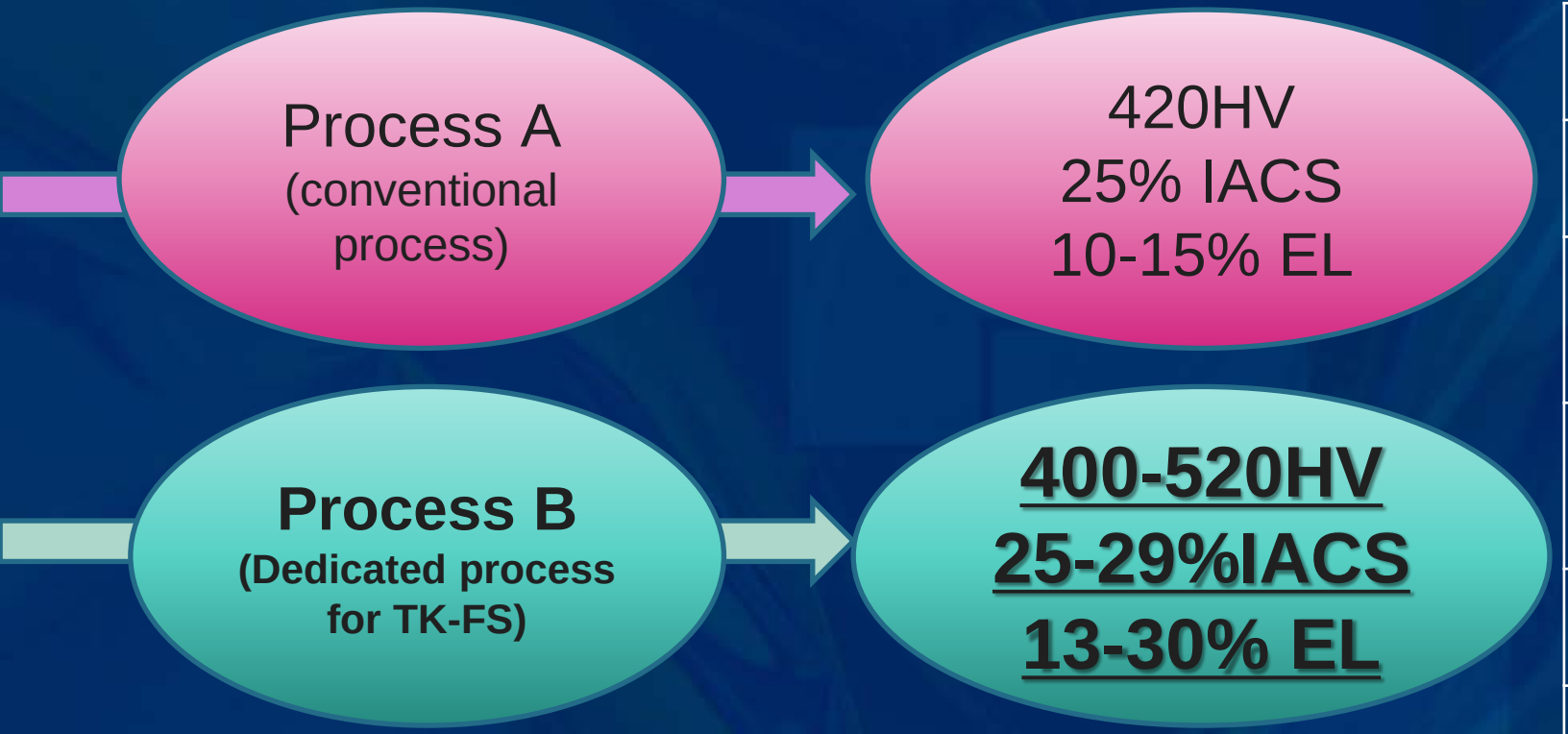


Straightening

Inspection

Shipping

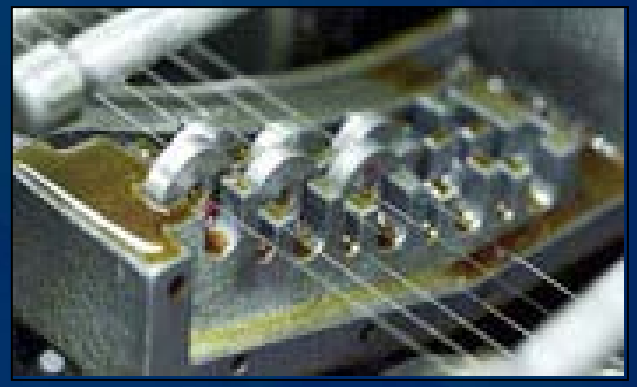
Manufacturing Process of TK-FS

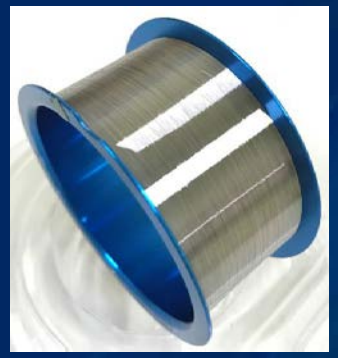


	Process A	**Process B**
Hardness (HV)	420	**400-520**
Young's modulus (GPa)	115	**150**
Electrical Conductivity (%IACS)	25	**25-29**
Elongation (%)	10-15	**13-30**
90° Bends	8-10	**8-14**

The TK-FS dedicated process (Our know-how) allows a wide range of adjustments in each characteristics, although only a limited range of properties could be achieved with the conventional process.

Capable wire diameter / Future business of “TK-FS”





We have already succeeded in manufacturing **0.03 to 1.0mm in diameter,** and are trying to manufacture less than 0.03mm products.

Foil type products (0.02~0.1mm in thickness) are also been trying to establish manufacturing process.

We plan to **replace various current Pd-based Probe-pins materials with TK-FS** in the future!

Conclusion

- Depending on the types of probe-pins using in the semiconductor manufacturing process, high hardness, high electrical conductivity and high ductility are required for Probe-pins materials.
- TK-FS can be applied to various types of Probe-pins. TK-FS is manufactured by the dedicated process and its characteristics are widely adjustable.
- In the wear test, the results are different in the test load. (At high load test, Wearing area decreases with increasing the hardness of materials.)
- We have already succeeded in manufacturing TK-FS fine wire with 0.03 to 1.0mm in diameter, and are trying to manufacture less than 0.03mm in diameter, and also foil products with 0.02~0.1mm in thickness.
- We plan to replace various current Pd-based Probe-pins materials with TK-FS in the future.

THANK YOU !

Let’s discuss in detail about “TK-FS” at Our Exhibition Booth (#500)!!

Web Site: https://tanaka-preciousmetals.com/en/products/detail/probe-pins/

Application of MD (molecular dynamics) methodology in the development and verification of advanced MEMS materials for future wafer probe cards

Young Jun Park, Sang Dan Kim, Song Ho Kim, Jin Wook Jang
Korea Instrument Co., Ltd.
Changhyun Cho, Joonyeon Kim
Samsung Electronics Co., Ltd.

4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

Overview

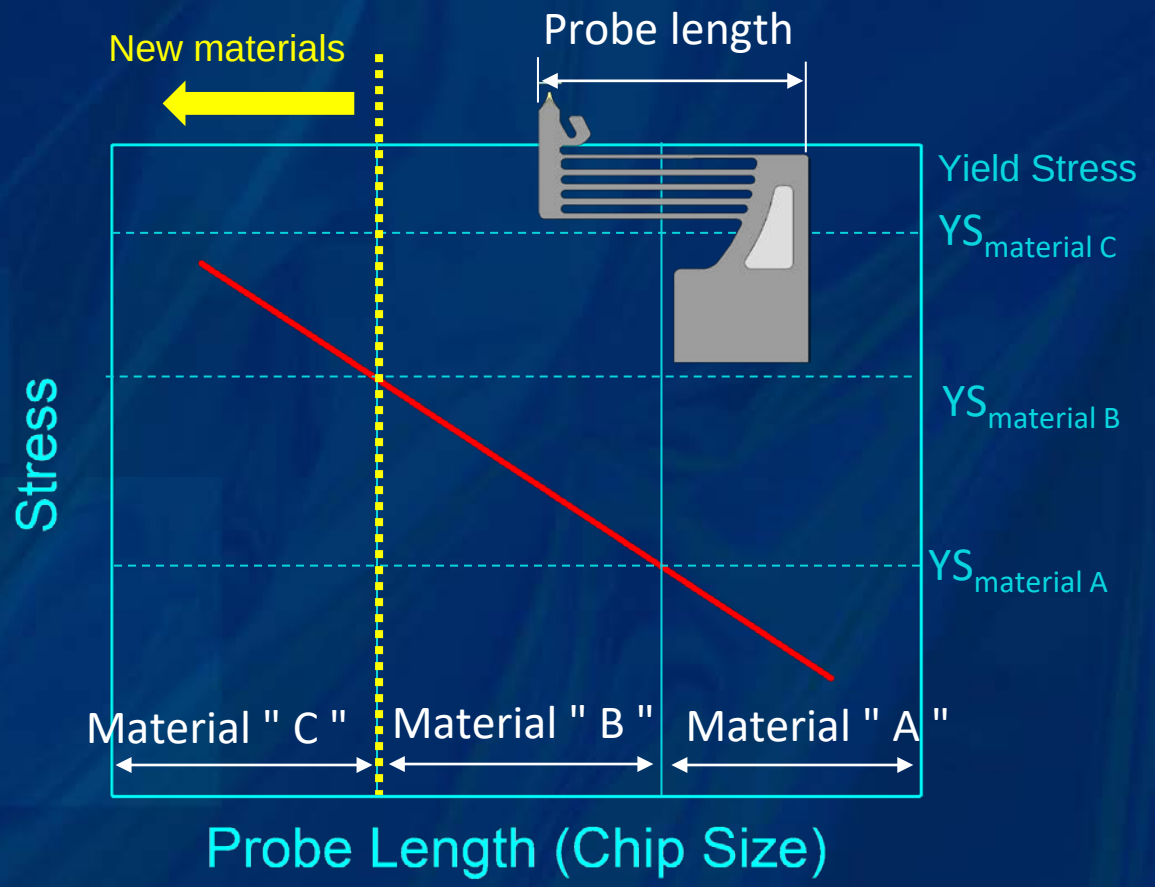
- Needs of new materials for the probes in a probe card
- Brief introduction of simulation hierarchy
- Molecular dynamics (MD) simulation
  - ✓ Conventional methods to measure materials properties
  - ✓ Importance of simulation methodology in predicting the materials properties
  - ✓ Data processing for crystal defect and density functional theory (DFT) simulation
- Cognitive simulation with a real MEMS Probe
  - ✓ Mechanical data and Multi-physical (Mech/Elec/Ther) data
  - ✓ Analysis of the gaps between simulation and measurement data
- Summary
- Future works

Objective of our study with a simulation hierarchy

Trend of chip size and the number of probes in a wafer

- **Smaller chip size links to shorter probe length, which in turn necessitates the development of new materials with unique properties**

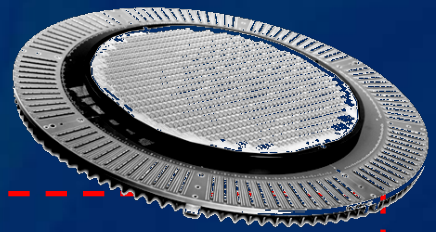
✓ **Trend of chip size vs. the number of probes**



✓ **Requirement of probe length vs. yield stress**

Simulations hierarchy from materials to systems

- Technical level of simulations to help develop new probes



Digital twin : " Real world = Simulation world "

" What is the level 0? "

Level 0

Materials properties

Level 1

- 3D Modeling & analysis
- Structure simulation

Level 2

- Test data matching
- Multi-physics simulation

- CAE Model
- Test result data

Level 3

- Analysis / Prediction
- Structure Optimization

A.I. study

Deep learning

Machine learning

Process of Molecular Dynamic (MD) Simulation

Evaluation of materials properties by conventional methods

- **Tensile test**
  - ✓ The most basic method to obtain elastic/plastic properties
  - ✓ **Risk point :** Change in the properties w.r.t. the specimen size (e.g. test coupon vs. actual probe)
    Supplementary method : Micro tensile test
- **Micro indentation test**
  - ✓ A method to obtain a variety of mechanical properties in a localized region
  - ✓ **Risk point :** Change in the properties w.r.t. indentation depth (due to the effects of surface and/or substrate)
- **Micro Compression test**
  - ✓ **Method to make up for micro-indentation test**
  - ✓ **Risk point : Difficulty in predicting the tensile data**

- **Above three methods are used interchangeably and complementally**

Limitation of the conventional measurement methods

- **A number of tedious iterations during the development of new materials**
  - ✓ High cost and time-consuming process

Make the

for MEMS

Necessary conditions to evaluate new materials

1. A much faster method

2. A much more affordable method

3. A method to determine the direction of development

Prediction of the properties using simulation methodology

- **Need to determine the direction of new materials development**
  - ✓ Sometimes very hard to make all the candidates with real substances

Experimental evaluation for material properties

Simulation for material properties

Steps for the prediction of properties via molecular dynamics

- **Concept to simulate the properties of a chosen alloy**

Structure/defects with random distribution → Density Functional Theory (DFT) → Molecular Dynamics(MD)

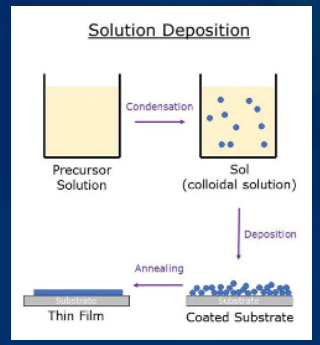
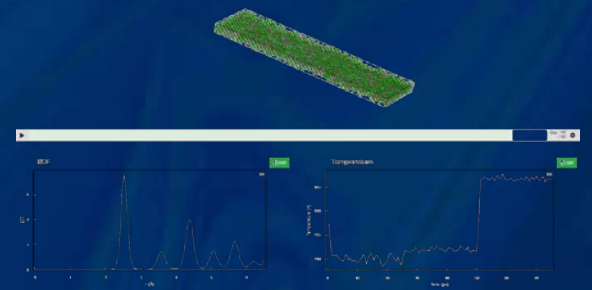


Image source : Sigmaaldrich



✓ **Basic Assumption of candidates alloys**

✓ **Selection of an alloy**

✓ **Verification of properties for a selected alloy**

Step I : Data acquisition from existing known alloys

- **First step to predict the properties of alloy (used in MEMS probes)**

Structure/defects with random distribution

Data Acqusition

Data Processing

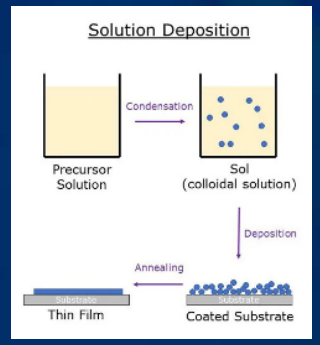
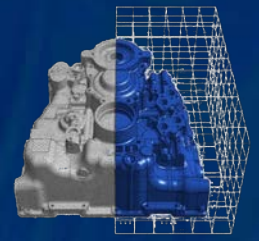


Image source : Sigmaaldrich

In our study, real data was used as the first step



- ✓ **Basic Assumption of candidates alloys**
- ✓ **EBSD**
- ✓ **TEM**
- ✓ **Mesh free method**
- ✓ **Confirmed with FEM**

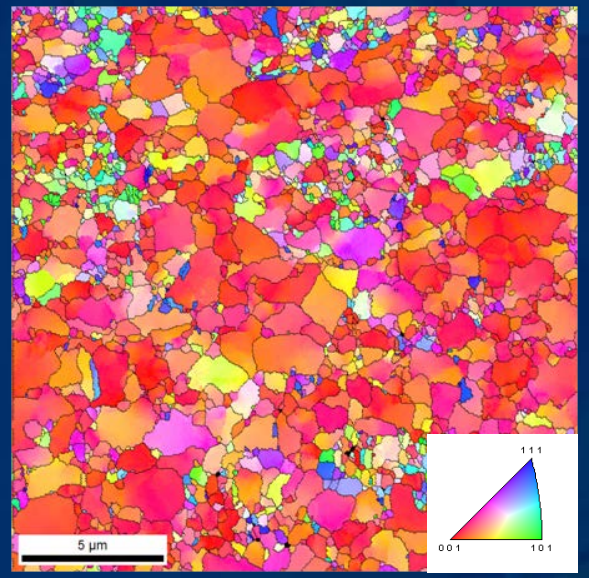
Data processing by Mesh-free method (MFM)

- **MFM is suitable for crystal-defect sensitive objective with a complex geometry (such as MEMS probes)**

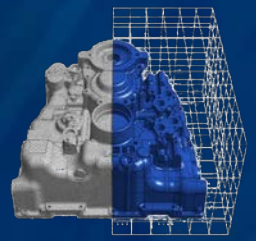
Data Acquisition

Data Processing

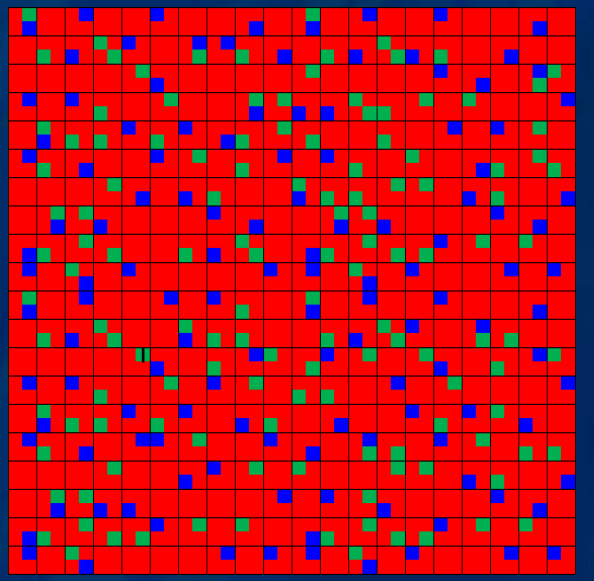
✓ **EBSD**



Sample (About 100 ea)

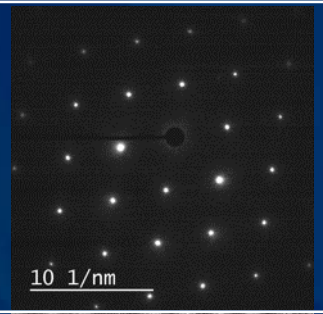
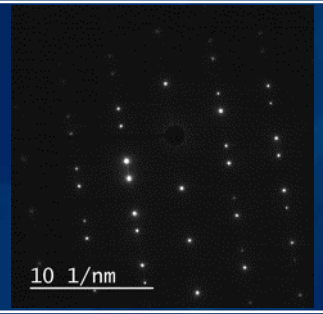
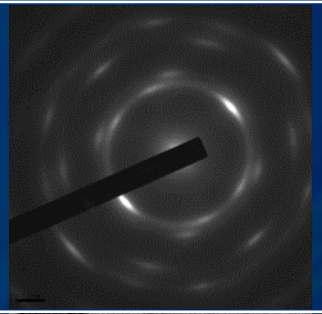
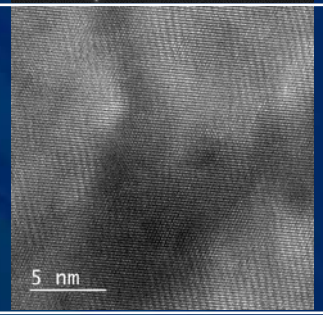
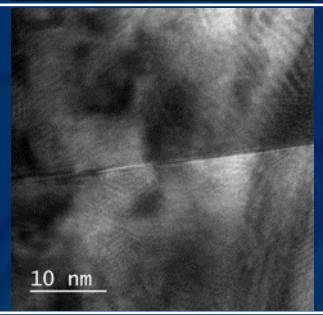
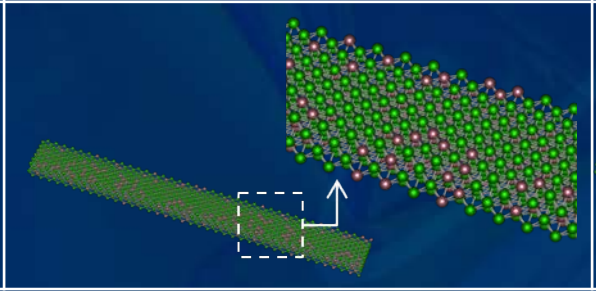
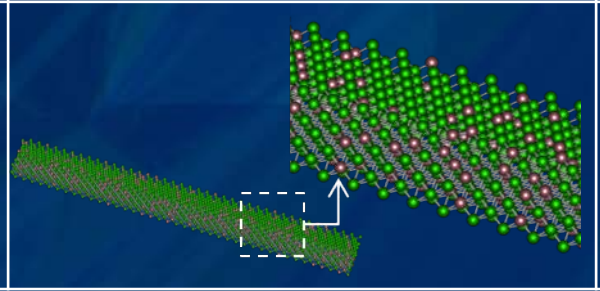
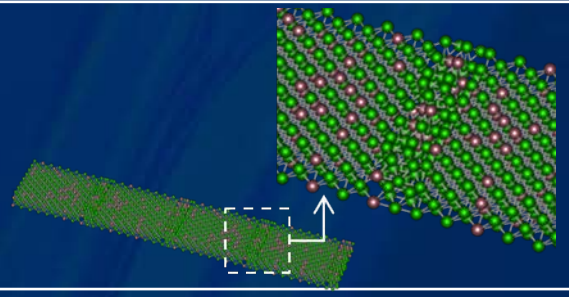


✓ **MFM**



Step II: DFT-based structural modeling

- **DFT modeling is able to accommodate a variety of crystal structures/defects**

	Single Crystal (SC)	Twin	Poly Crystal (PC)
SAED Pattern			
HR-TEM			
Structural modeling			

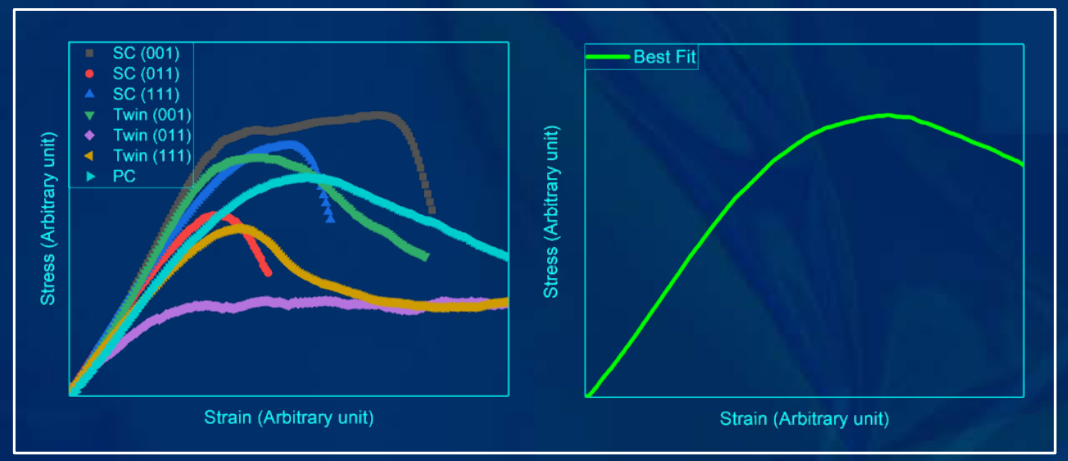
Step III : MD simulation and fitting

- **Performing stress-strain(S-S) simulations using MFM and MD**

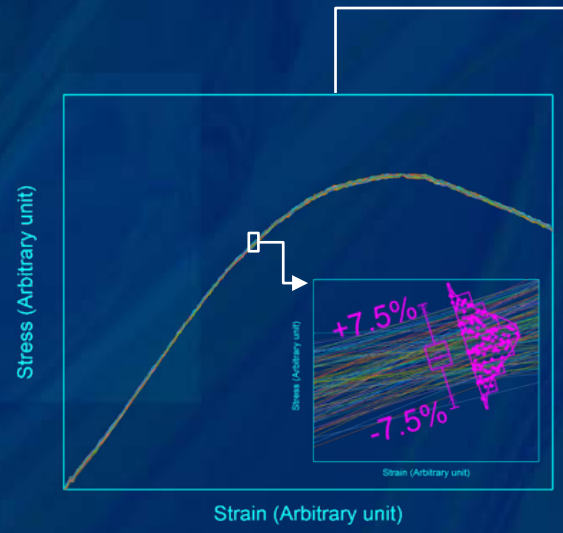
$$S\text{-}S_{simulation} = \text{Normalized Factor} \times [\ (\alpha \times \text{SC } S\text{-}S_{simulation}) + (\beta \times \text{PC } S\text{-}S_{simulation}) + (\gamma \times \text{Twin } S\text{-}S_{simulation}) + \delta(\text{Crystal defects})\ ]$$

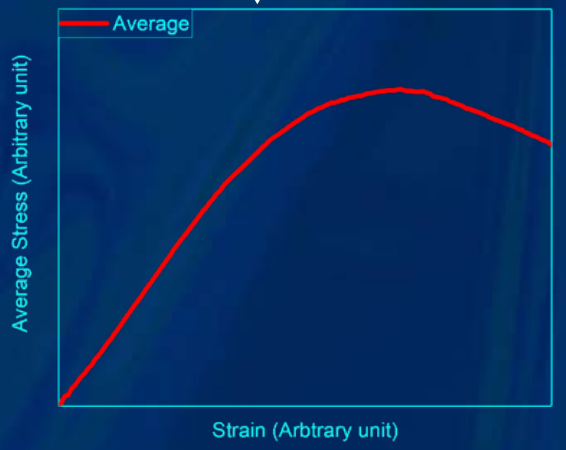
Data Processing → DFT → MD → Statistical analysis → Trend Curve Fitting

Repeat x 100 times
(A hundred samples)



x 100 times



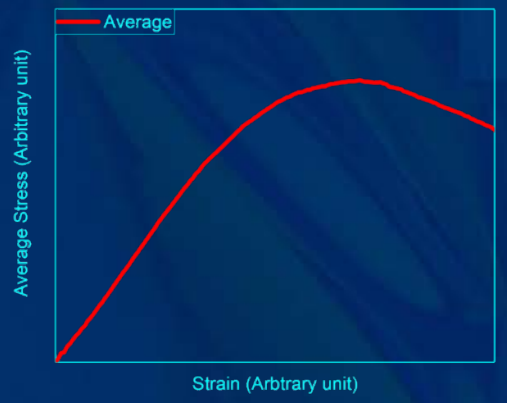


Validation of MD Simulation with a real probe

Validation of MD Simulation with a real probe

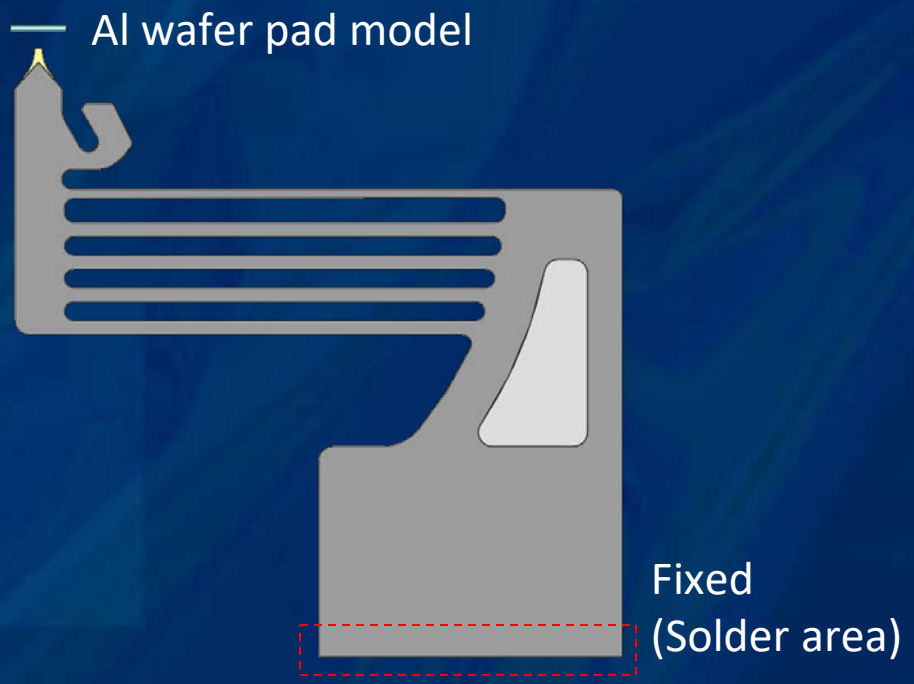
- **Start the simulation using the data from trend curve fitting**

Trend Curve Fitting



✓ Stress-Strain data from MD Simulation

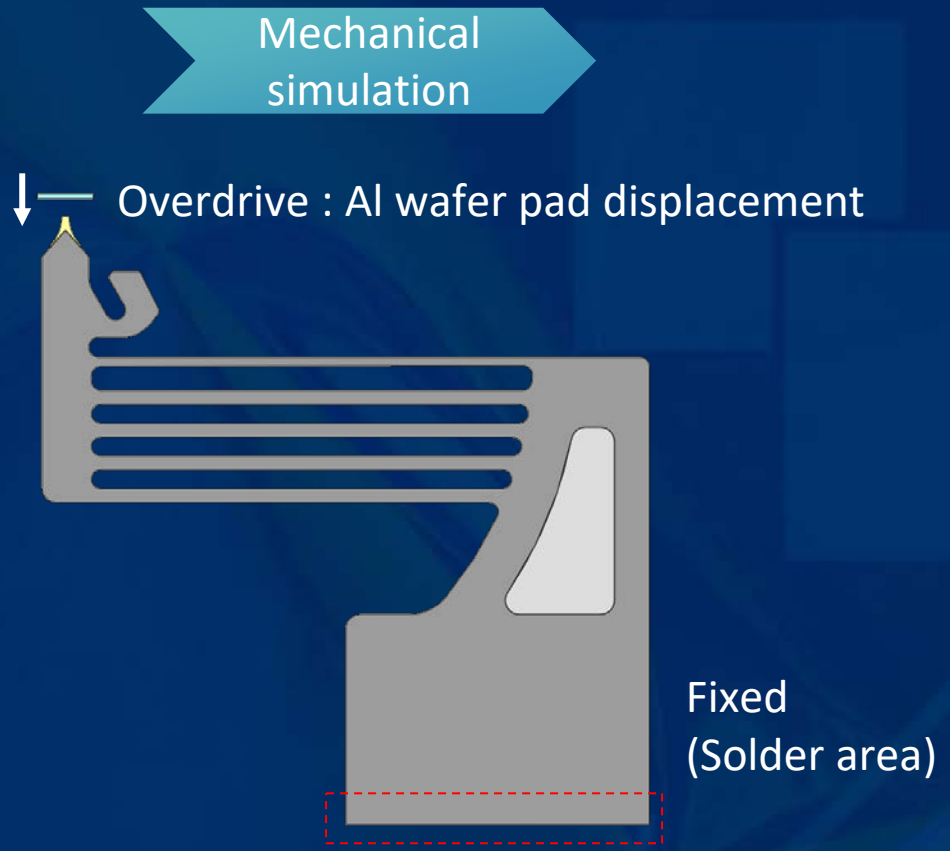
Mechanical simulation



✓ Typical probe shape (Not an actual product)

Cognitive Simulation of MEMS Probe - Mechanical Aspect

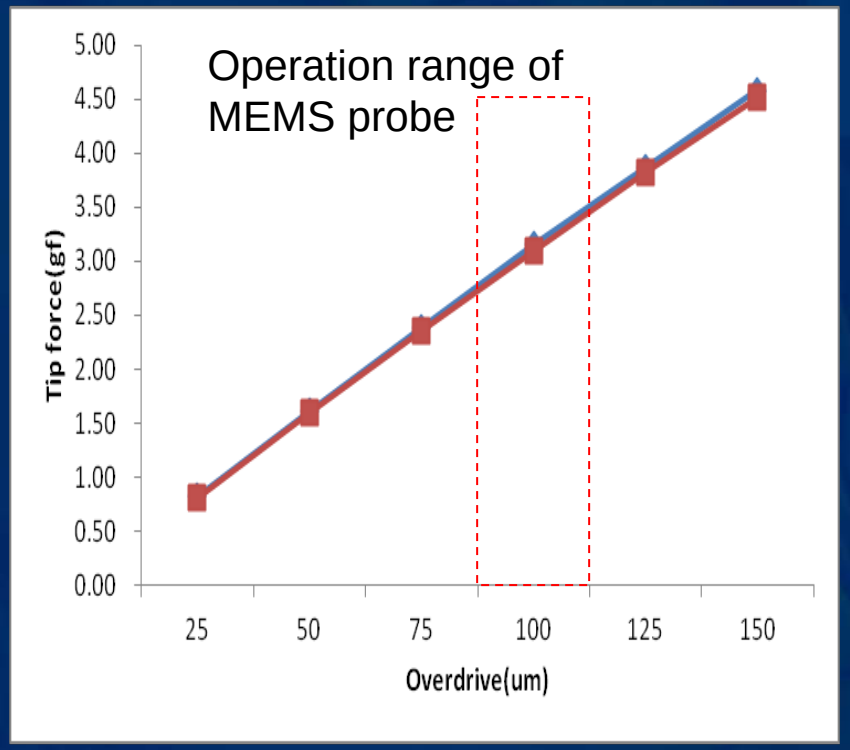
- **Preparation of simulation conditions and the necessary data set**

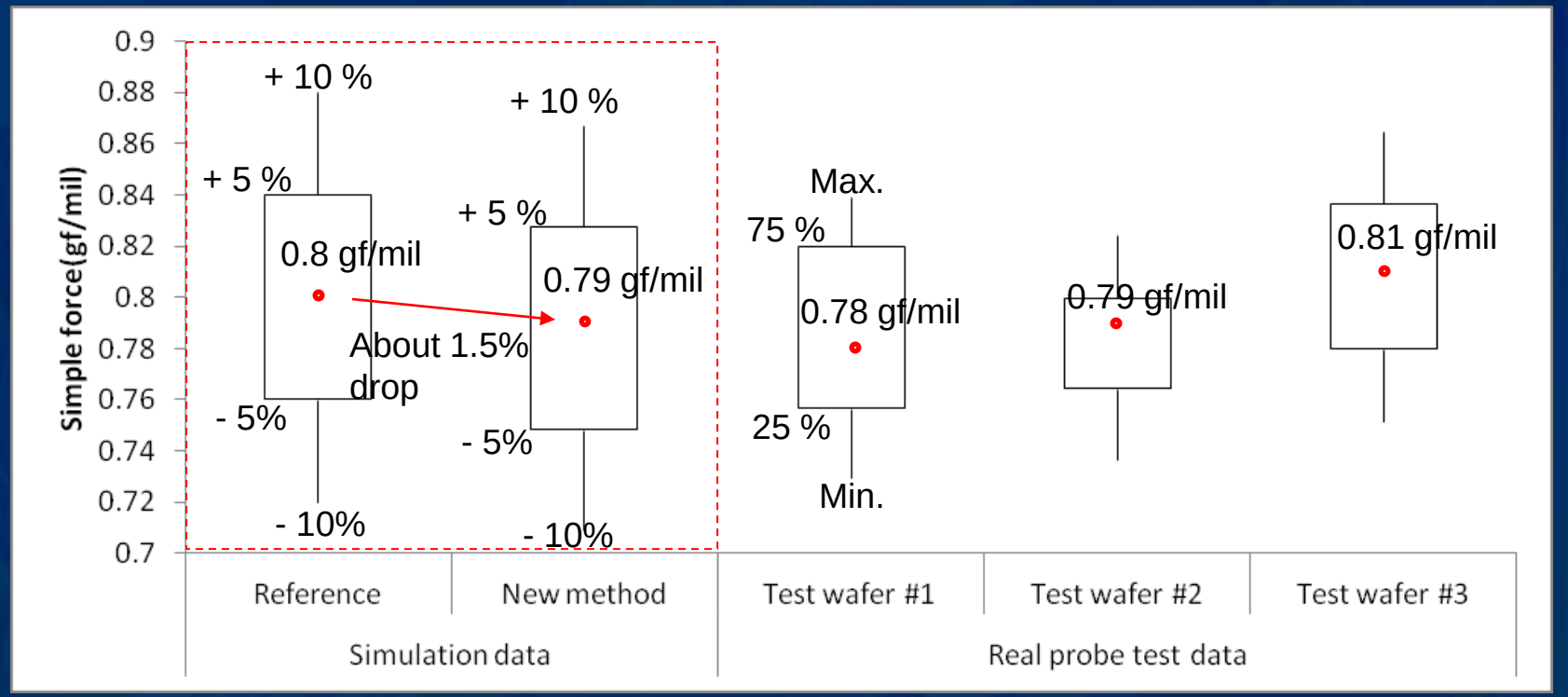


- **Mechanical simulation for tip force**
  - ✓ Non-linear simulation
  - ✓ Implicit method, dynamic method
  - ✓ Quasi-static analysis
  - ✓ Fixed : Solder area
  - ✓ Overdrive(Load) : Displacement
- **Al pad property for simulation**
  - ✓ Modulus : 68 GPa
  - ✓ Poisson's ratio : 0.36
  - ✓ Yield stress : 105 MPa
  - ✓ Density : 2.70 g/cm^3
  - ✓ Second hardening modulus : 680 MPa

Cognitive Simulation of MEMS Probe - Mechanical Data

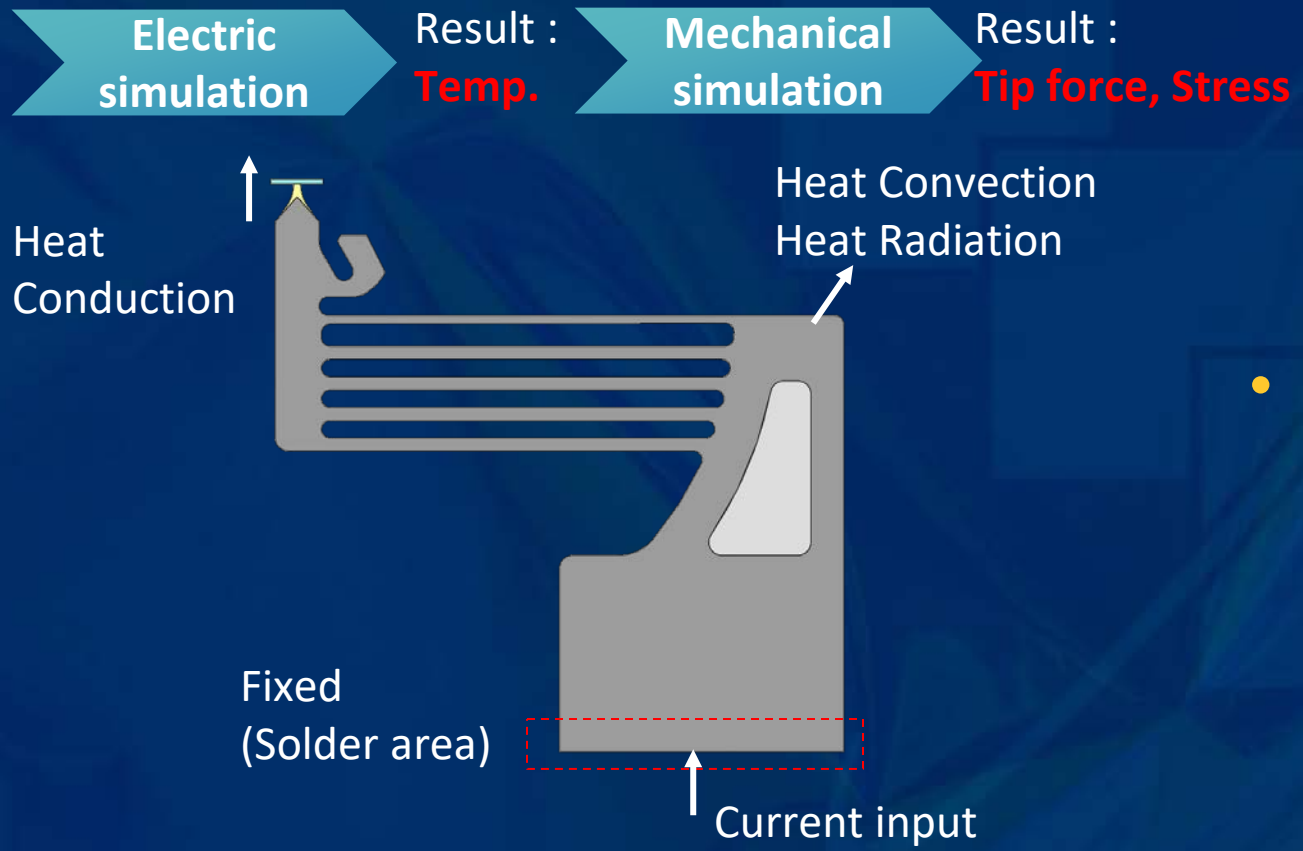
- **Prediction of Tip Force (spring const.) Results**
  - ✓ The difference between the simulation and measurement data is approximately 1.5%.
  - ✓ This is well within the manufacturing tolerance of MEMS probes.
  - ✓ The predicted properties using our method shows a high consistency.





Cognitive Simulation of MEMS Probe - Electrical Aspect

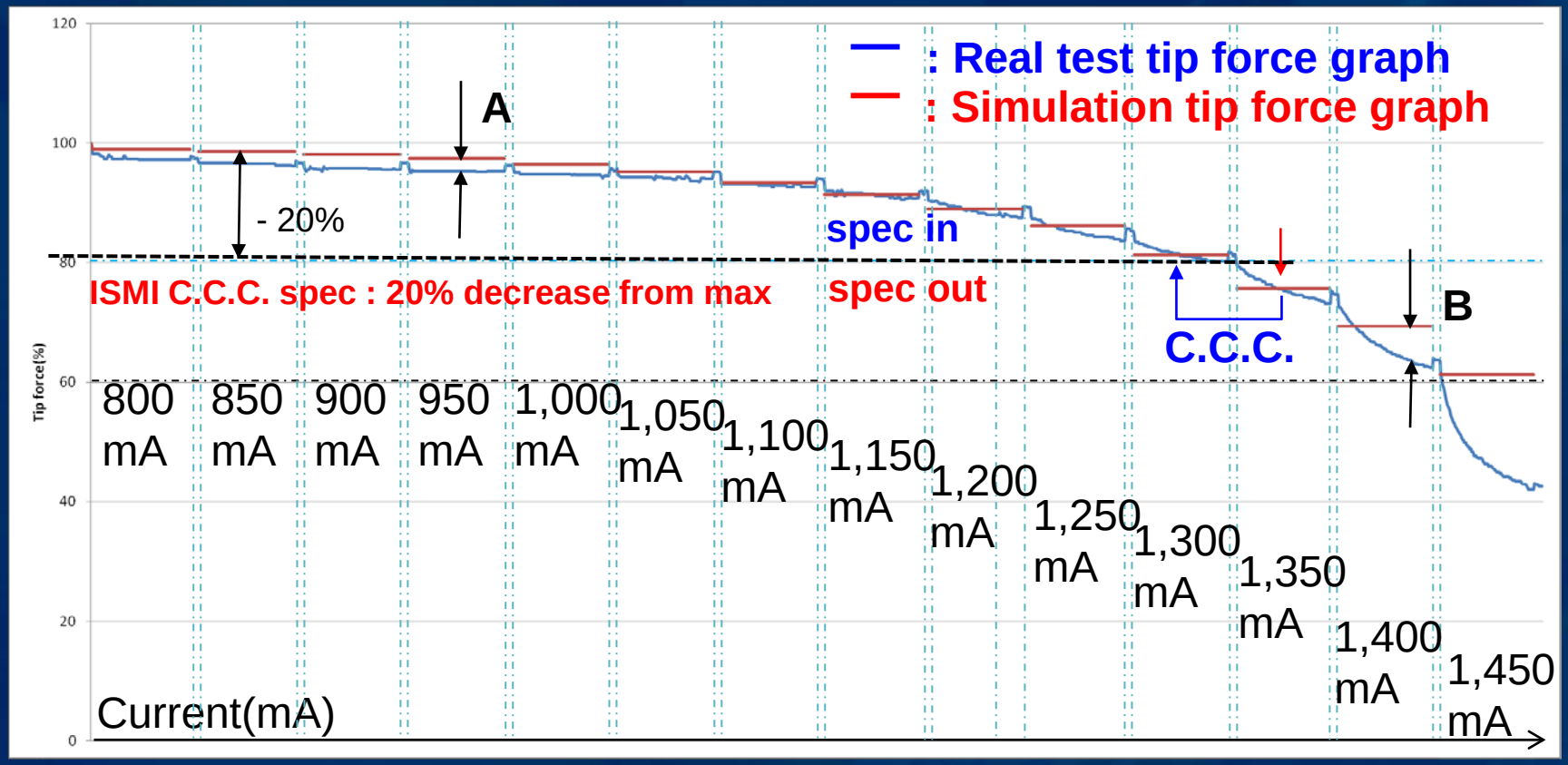
- **C.C.C.(current carrying capability) is the most important electrical property.**
  - C.C.C. is highly dependent on the mechanical and thermal properties.

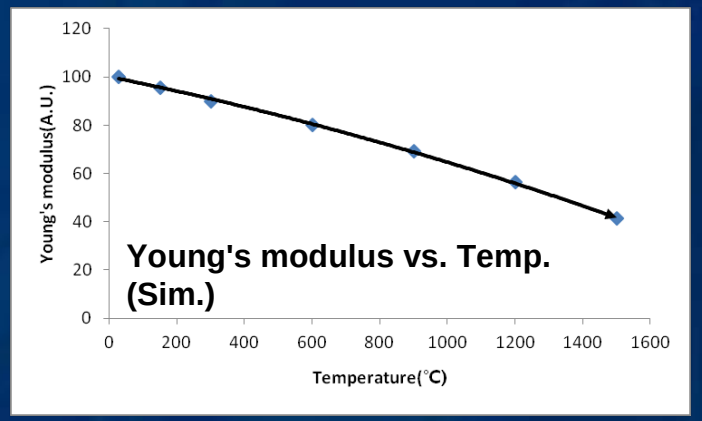


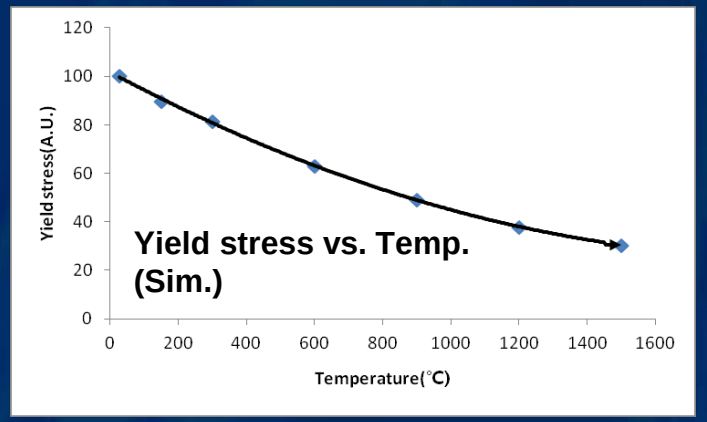
- **Electric simulation (for C.C.C.)**
  - ✓ Joule heating simulation
  - ✓ Contact resistance : Constant
  - ✓ Conduction coefficient : Constant
  - ✓ Convection coefficient : Constant
  - ✓ Radiation coefficient : Constant
- **Al pad property for simulation**
  - ✓ Non-linear simulation
  - ✓ Implicit method, dynamic method
  - ✓ Quasi-static analysis
  - ✓ Fixed : Solder area
  - ✓ Overdrive(Load) : Displacement

Cognitive Simulation of MEMS Probe - Electrical Data

- **Force drop w.r.t. current : measured data > simulated data**
  - ✓ Decreases in Young's modulus and Yield strength lead to tip force decrease.
    - Middle current region (800 -1250 mA) : relatively small gap denoted by "A"
    - High current region (> 1250 mA) : considerable gap denoted by "B"

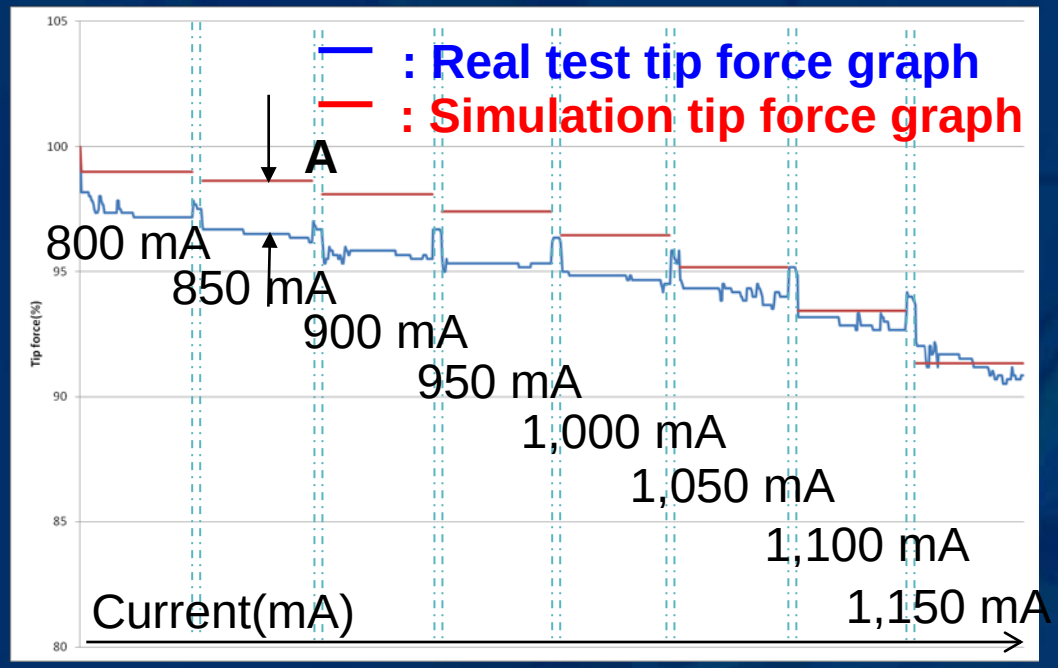


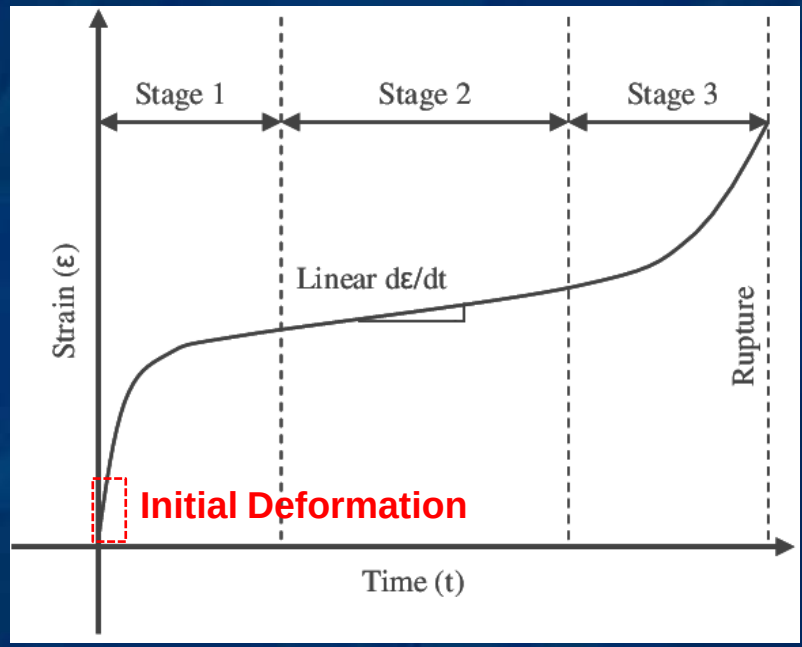




Cognitive Simulation of MEMS Probe - Gap analysis A

- **Small gap (up to 1,150mA) between measured and simulated data (A)**
  - ✓ Relatively large deformation at the very beginning of test
  - ✓ Hard to quantitatively predict due to the extrinsic factors (heat treatment etc.)





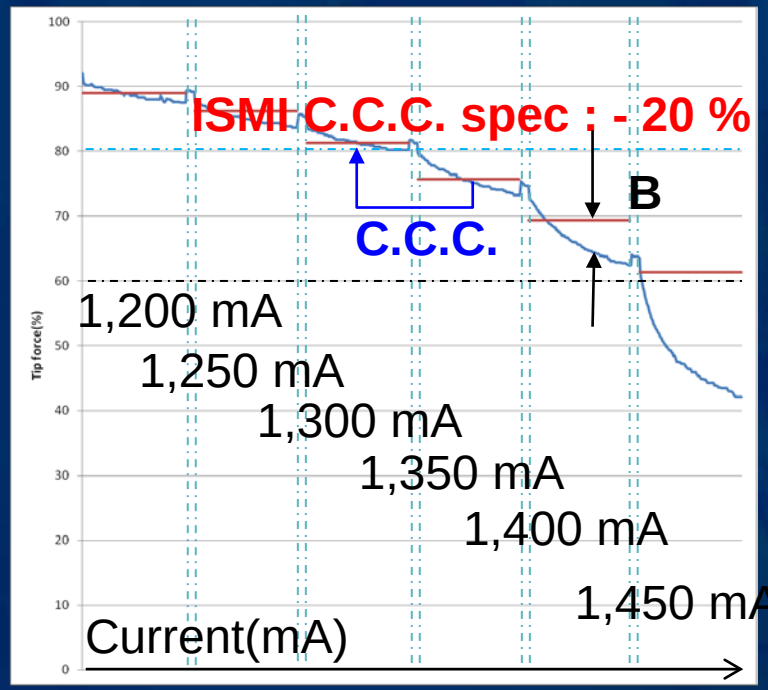
Cognitive Simulation of MEMS Probe - Gap analysis B

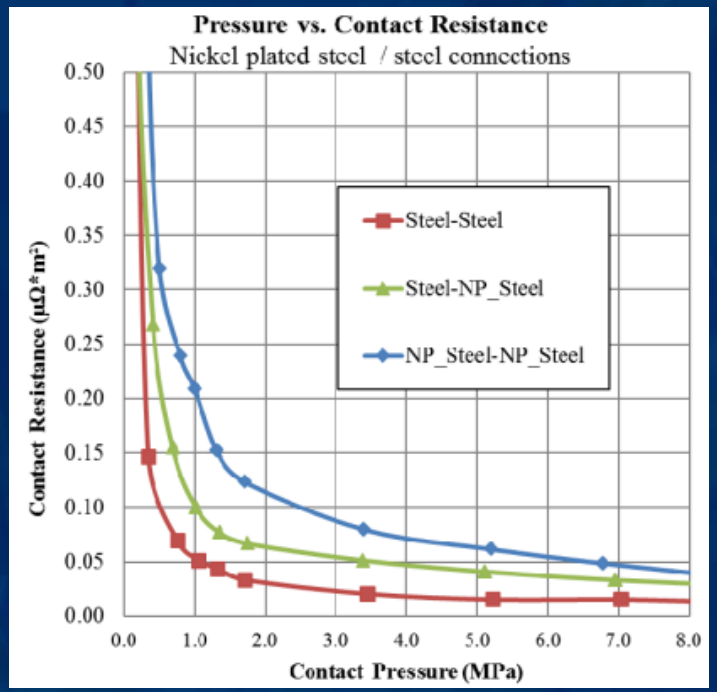
- Large gap (>1,150mA) between measured and simulated data (B)

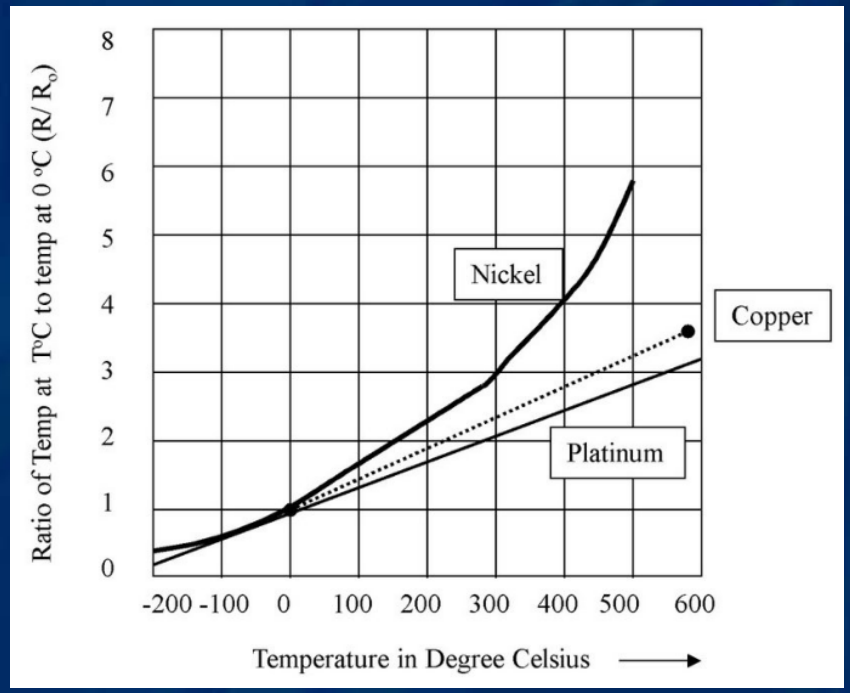
✓ High Current → Joule heating → Decrease in Young modulus → **Contact R increase**

repeat

✓ Metals show different behaviors of R-increase with temperature







" Contact Resistance versus Pressure of Electrical Connections Used in Aluminium Smelter Potlines ", W.Berends Y. J. Park et al.

" Research and Design of Snow Hydrology Sensors and Instrumentation " , Raman K. Attri

Summary

- We suggested the simulation methodology to predict and validate the properties of new materials for MEMS probe application.
  - ✓ To predict the mechanical properties of new materials, Molecular Dynamic (MD) based tool was mainly used.
  - ✓ Prior to MD simulation, we performed data processing on crystal defect/structure and simulation based on Density Function Theory (DFT).

- To verify the consistency of our simulation methodology, we simulated the mechanical properties for a known material.
  - ✓ Key mechanical properties of real probe (tip force vs. current) were predicted in comparison with measured values.
  - ✓ Although the overall trend is similar, the gap existed such that it became larger in higher current region.
  - ✓ The gap is due to initial deformation and contact resistance characteristics, where some of the materials properties can be obtained by measurement only at this point.

Future works

- Additional information for the completeness of MD Simulation
  - ✓ Material creep behavior at the very beginning stage
- Additional simulation areas that can replace experimental methods
  - ✓ Dependence of contact resistance on tip force and contact area
  - ✓ Further study on contact resistance, related to
    - -. Fretting phenomenon caused by mechanical movement and/or thermal expansion
    - -. Self-cleaning effect that typically helps to decrease the resistance
  - ✓ Fritting, a melting/softening phenomenon, occurring when the voltage reaches a critical point.

If you have any questions,
PLEASE SEND an e-mail

(E-mail address : teakongjuni@kicl.co.kr)

Cutting Cost and Resolution Enabled by Novel Photonic Technologies for Next–Generation Probe Cards Manufacturing

Dr. Ksenija Varga, Dr. Thomas Uhrmann
Business Development Management
EV Group

4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

SW Test Asia | Presentation Outline

- EV Group: Company Overview, Novel Photonic Technologies.
- Maskless Exposure Technology: Motivation for Evaluation: Objectives & Goals.
- Methods, Materials, Procedures.
- Key Data & Discussion.
- Newest EVG's Technology: NanoCleave™.
- Summary & Conclusions.

EV Group | Company Overview


EV GROUP
EVG
EV GROUP
FORSTINGER

EV Group | Novel Photonic Technologies

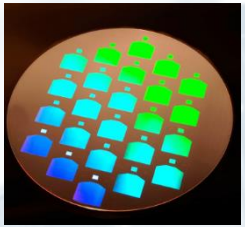
Leading supplier of wafer processing equipment for the MEMS, nanotechnology & semiconductors markets.

Founded in 1980 by DI Erich and Aya Maria Thallner. More than 1300 employees worldwide.

Headquarters in Austria, with fully owned subsidiaries in the USA, Japan, South Korea, China, Taiwan & Malaysia.

Advanced Resist Processing EVG®150 Series

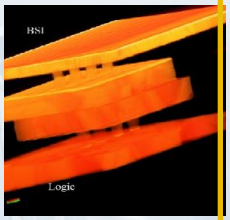
Maskless Exposure Technology LITHOSCALE®



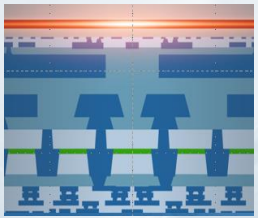
Nanoimprint & S&R Mastering HERCULES®

Wafer Level Optics & Photonics Packaging EVG®7300

METROLOGY



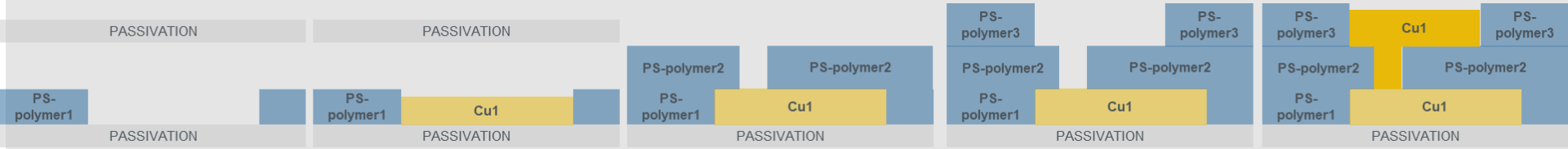
3D Integration & Hybrid Bonding



NanoCleave™ IR Laser Release

INTRODUCTION / BACKGROUND

- Fine pitch probe cards interconnect formation: several lithographic patterning steps.
- Process is connected to high CoO.



PATTERNING PROCESS
METAL1

- **VIA**

1. Coating
2. Expose VIA
3. Development
4. UV-cure
5. Post UV cure bake

- **METAL2**

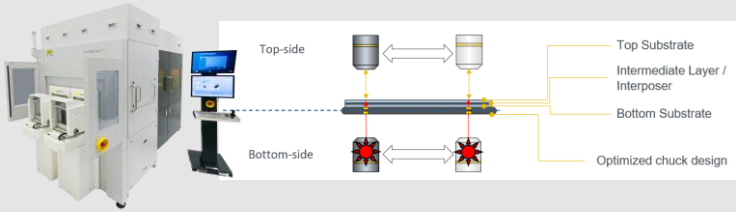
1. Coating
2. Expose METAL2
3. Development
4. UV–cure
5. Post UV cure bake
6. Oven cure as normal
7. Descum

Development of cost–efficient processes.

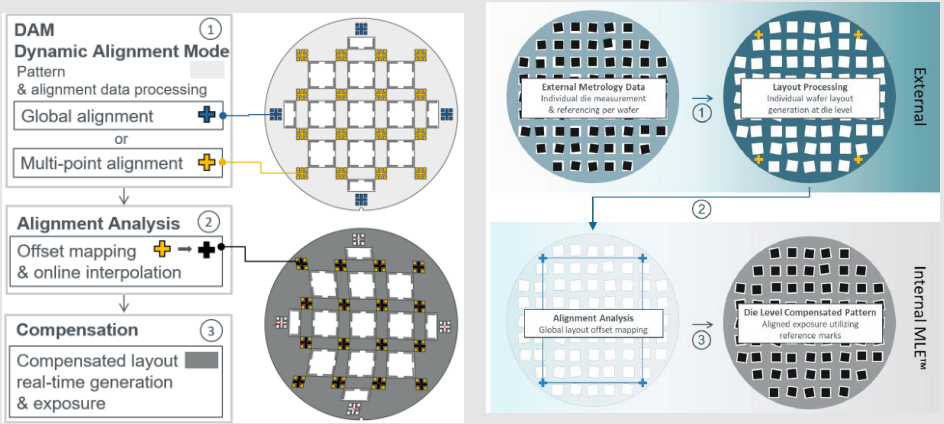
Cutting costs by reduction of the lithographic steps.

EQUIPEMENT

- VIS top–side alignment & backside alignment.
- Advanced Distortion Function: crucial for advanced packaging.
- High autofocus ±50 µm, high dept of focus ±12 µm.
- Die annotation feature.



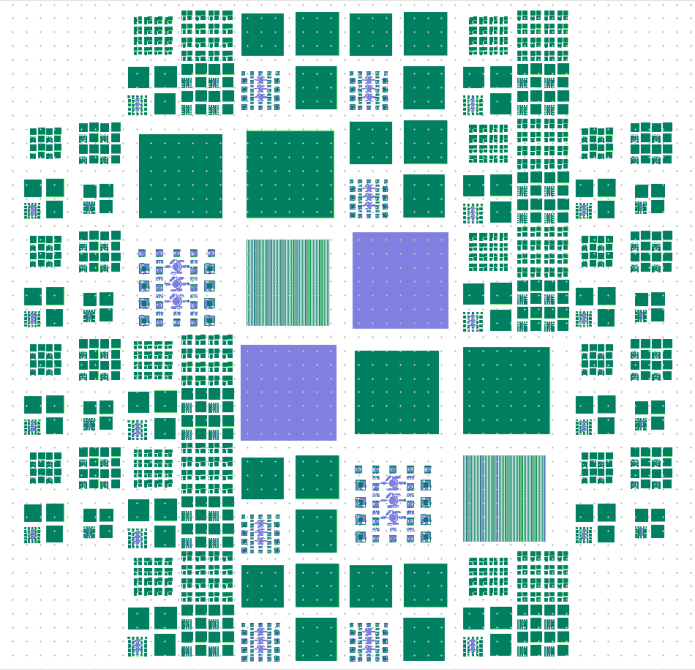
PARAMETER	SPECIFICATION
Exposure Source	HP UV – Laser Diode (LD)
Exposure Spectrum [nm]	375, 405 and every mix
CD L/S [µm]	< 2
Substrate Sizes [inch]	6“ – 12“
Wafer Layout [format]	GDS II (standard) Gerber, OASIS, ODB++ (optional)



Die-level compensation schematic process flow

TEST LAYOUT

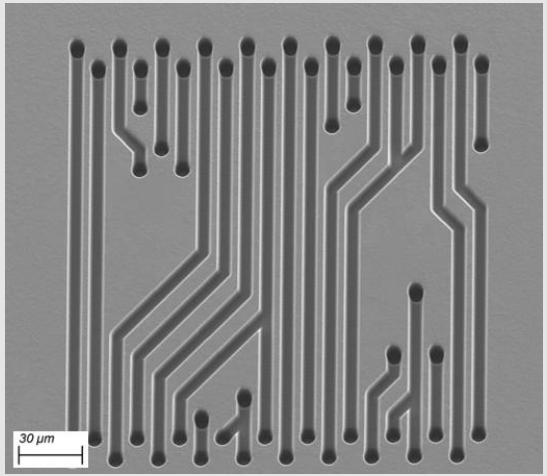
- Containing various test fields scaled up/down to different sizes written on 1 wafer.

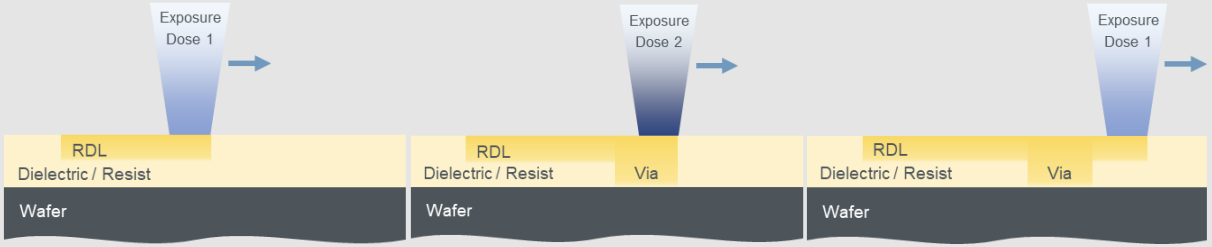


EFFICIENT PROCESS EVALUATION & OPTIMIZATION!

EXPERIMENTAL SETUP

- Evaluated dose range: 10–450 mJ/cm^2.
- TOK resist, positive tone.

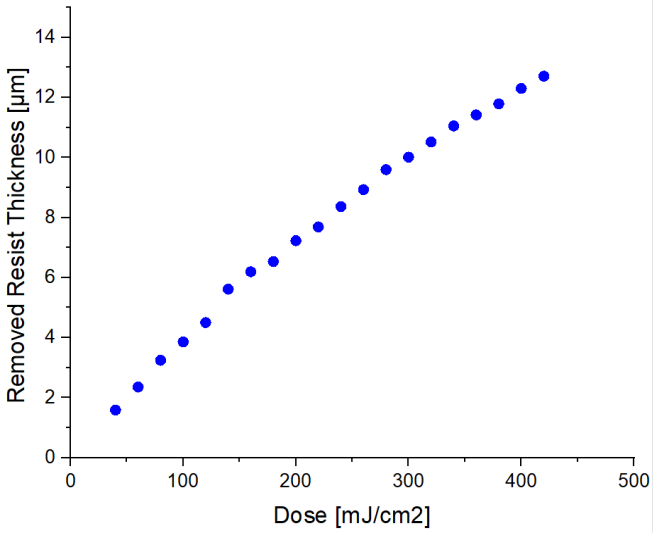




Design layout with dense RDL and VIAs connections

CONTRST CURVE

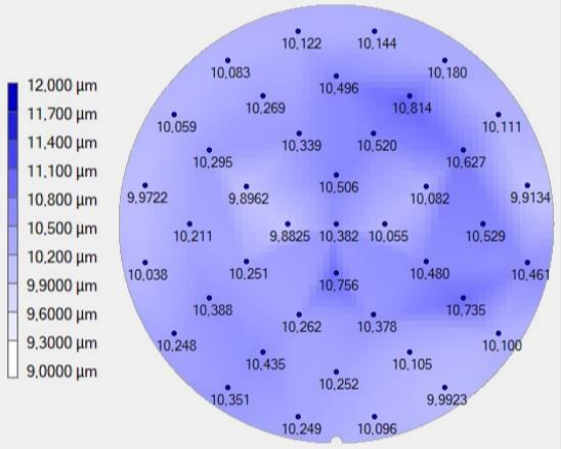
- To optimize the multi–level exposure an understanding of dose dependency on the penetration depth is required.
- Matrix where dose/wavelength/focus can be adjusted via recipe.



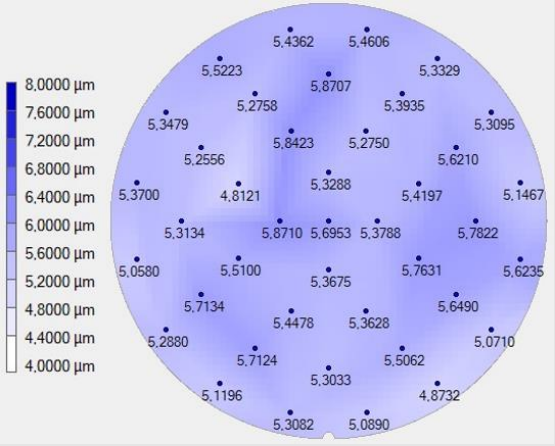
- Minimum exposure dose required to initiate reaction.
- Linear behavior at higher exposure dose

SPECTRAL REFLECTANCE IMAGES

- Estimation of the FT nonuniformity.



Nonuniformity measurement after spin–coating process.

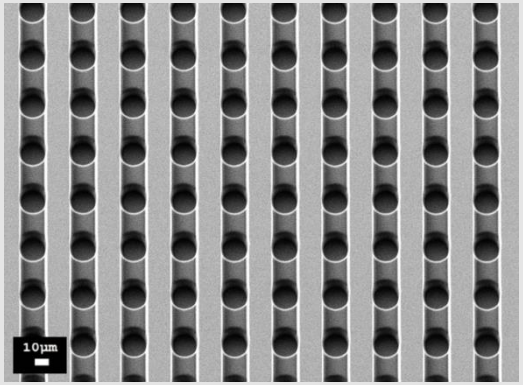


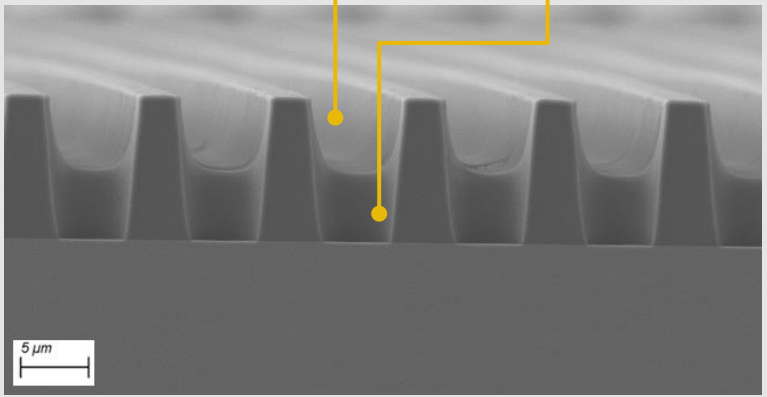
Nonuniformity measurement after exposure with a defined penetration depth & resist development.

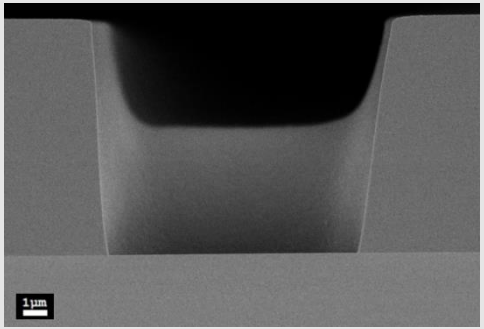
Resist surfaces generated via multi–level exposure is not significantly deviating from the original spin–coated surface.

SEM IMAGES of DUAL–LAYERS

- High dept–of–focus allows good control of sidewall profile and resolution throughout the resist layer thickness.



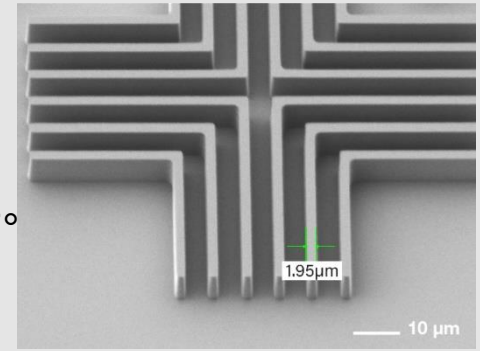


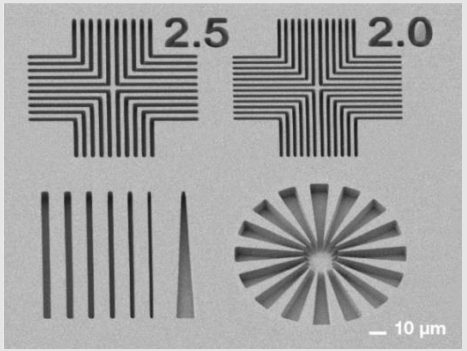


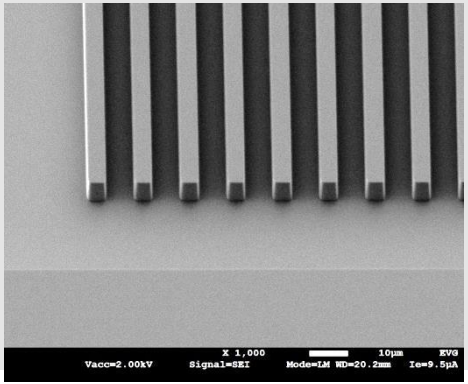
- RDL traces with vias (width: 5 µm, gap: 3 µm)

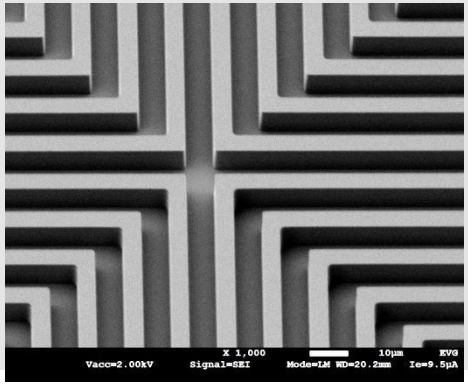
SEM IMAGES

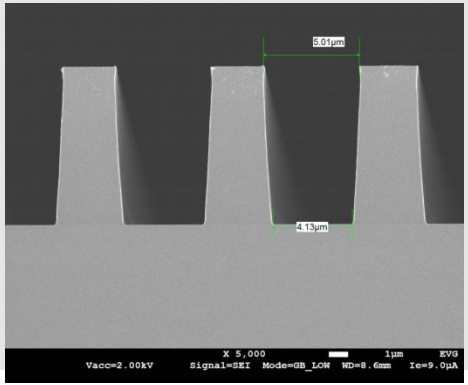
- Baseline evaluation of line–space variation patterning performance.
- Pos. TOK P–W1000T
- Layer thickness: 8 µm
- Aspect ratio 4:1, sidewall angle up to 87°

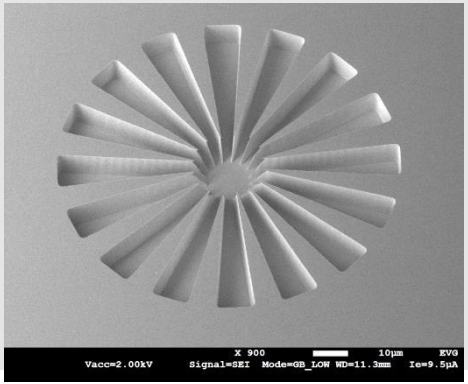






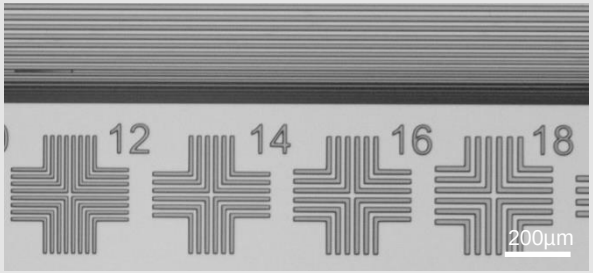


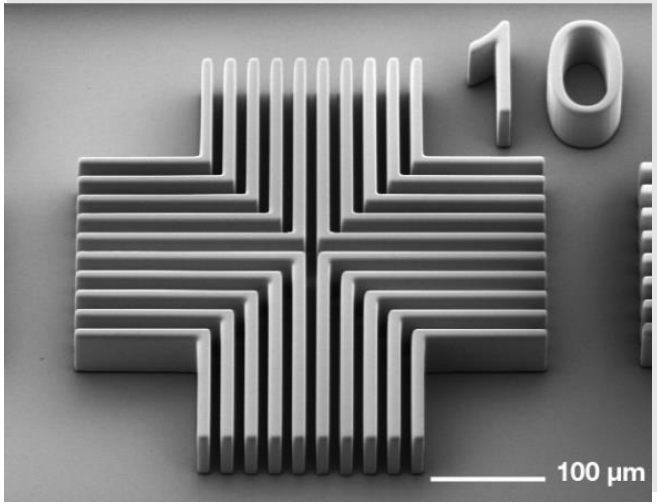


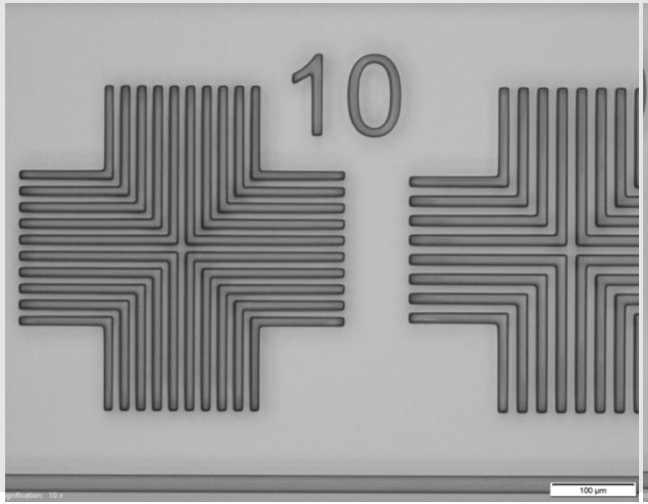


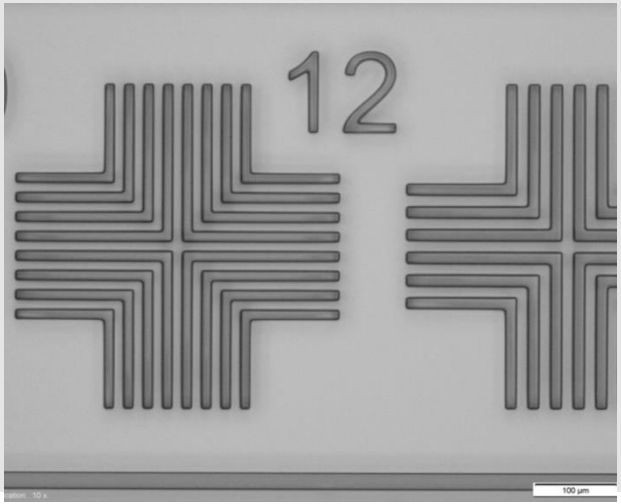
SEM IMAGES

- Thick resist applications.
- JSR THB 151N, negative tone.
- Layer thickness: 50 µm, AR 5:1





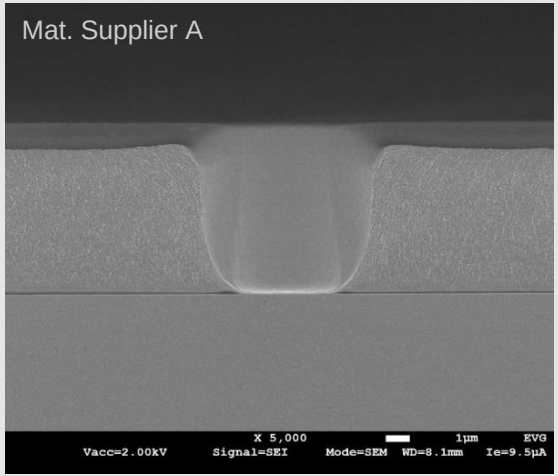




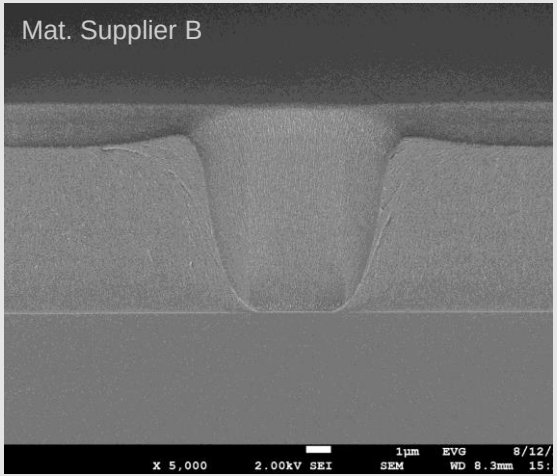
SEM IMAGES

- NEW DEVELOPMENT: negative tone dielectrics for fine pitch probe cards RDL patterning.
- Layer Thickness: 7 – 8 µm (after soft bake), AR: > 2:1

FUJIFILM Value from Innovation



3.5 µm via resolved in ~7 µm LT



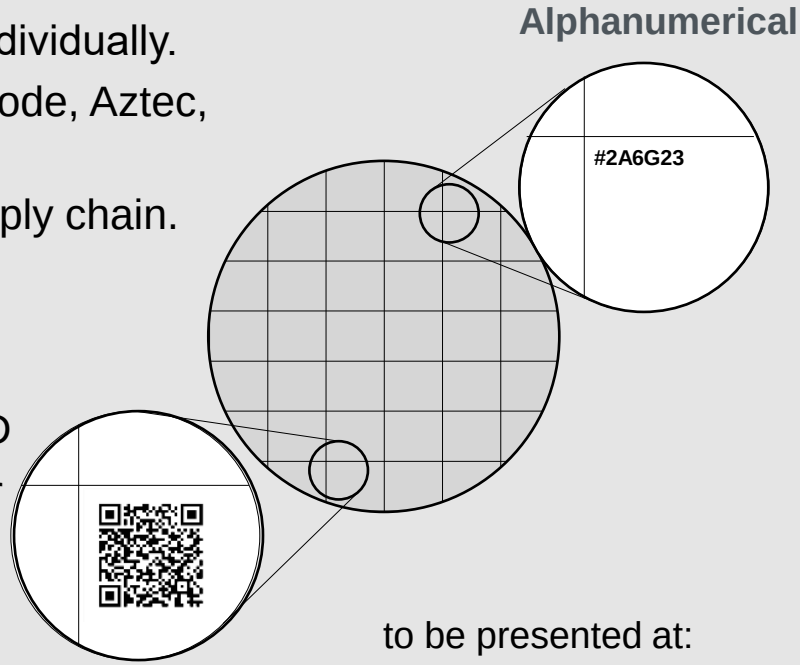
3 µm via resolved in ~8.5 µm LT

DIE ANNOTATION FEATURE

- Data generation “on–the–fly” for each wafer individually.
- Available Annotation Types: DataMatrix, QR Code, Aztec, PDF417 etc.
- Important for traceability in semiconductor supply chain.

VARIABLES USED

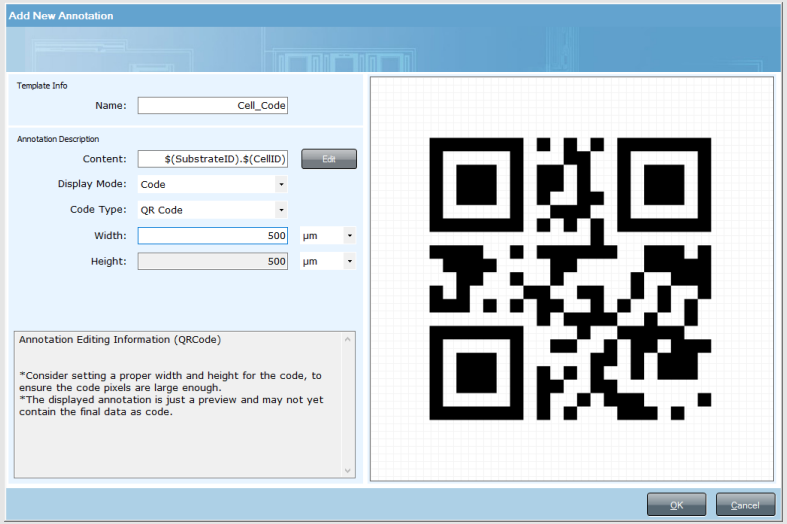
- LotID, SubstrateID, SubstrateAquiredID, CellID
- EquipmentName, ModuleName, SerialNumber
- RecipeName, RecipeNamespace
- ProcessJobID, ControllJobID



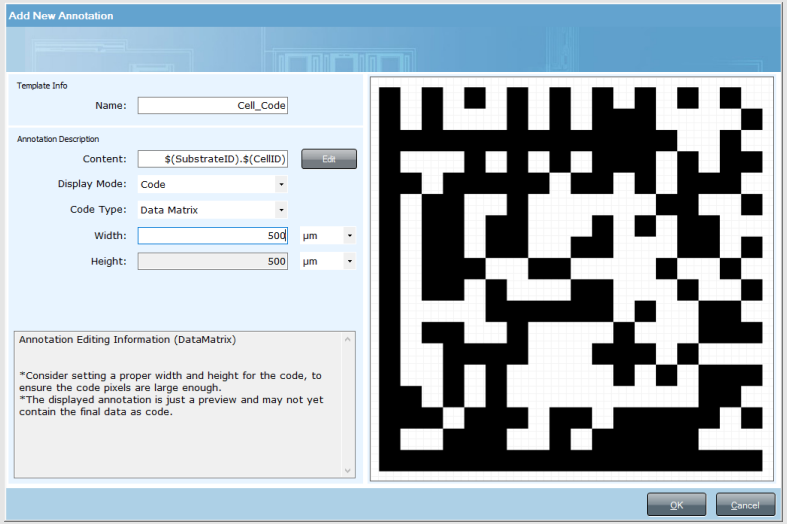
to be presented at:

EPTC 2023
25th Electronics Packaging Technology Conference

- Annotations are created as templates on LITHOSCALE® and can be used in various recipes.



QR CODE

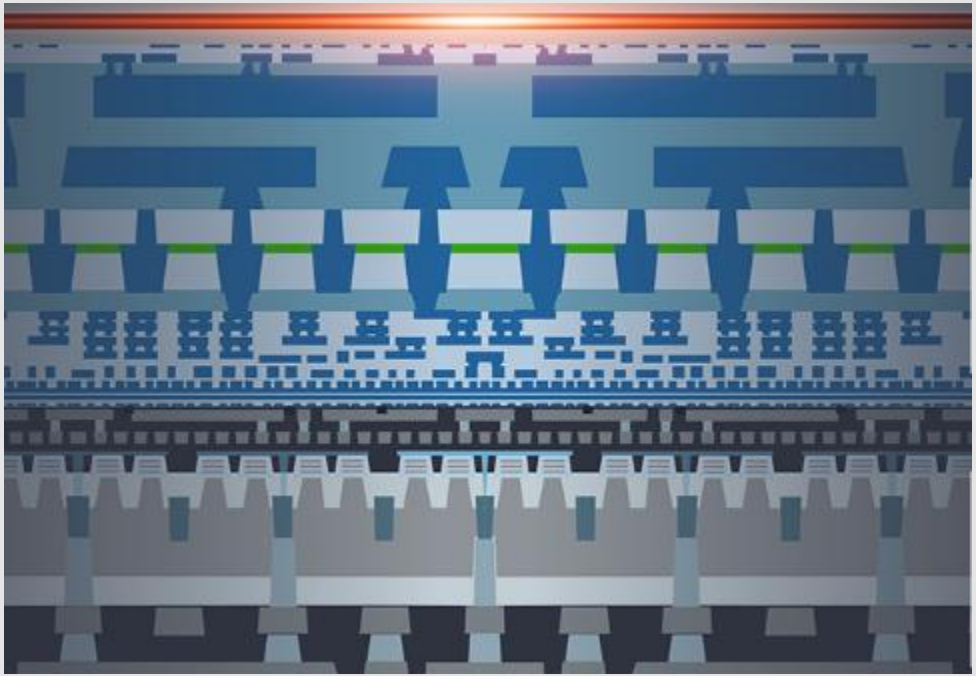


DATA MATRIX

NanoCleave™ | IR Laser Release

IR laser–initiated release of any ultra–thin film or layer from silicon carriers with nanometer precision.

Revolutionizing 3D & heterogenous integration as well as material transfer.

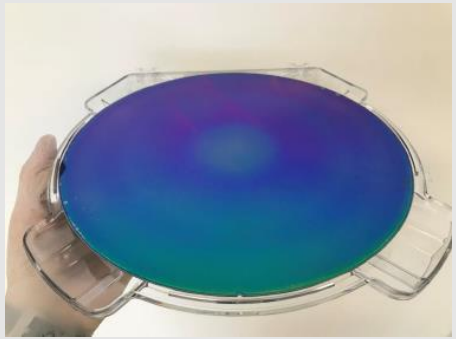


Front–end compatible carrier technology for further integration of fusion and hybrid bonding processes.

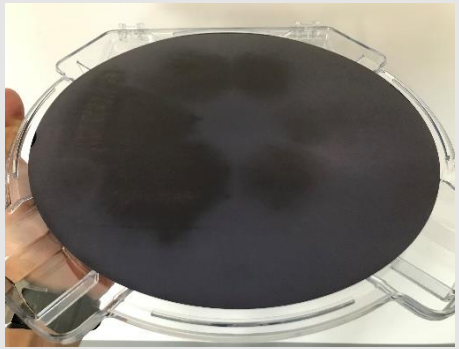
Enabling silicon carrier wafers in advance packaging processes such as FoWLP & 3D SIC.

INTRODUCTION

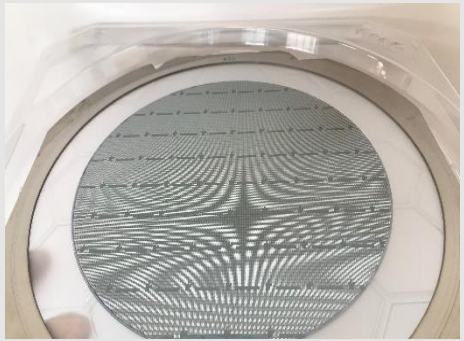
- Technology utilizes IR laser & inorganic release materials to enable laser debonding on Si.
- This eliminates the need for glass substrates in advanced packaging.
- Temperature & glass carrier compatibility issues are avoided.
- Ability to transfer ultra–thin layers via carriers in front–end processing is enabled.



300 mm fusion bonded wafers release



300 mm molded wafer release



200 mm temporary bonded thin device wafer release

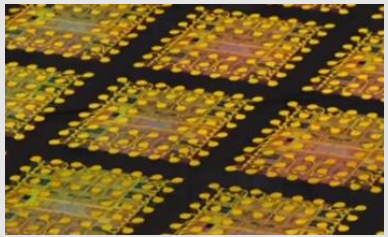
NanoCleave™ | IR Laser Release

INTRODUCTION

- The nanometer–precision of new process supports advanced semiconductor device roadmaps calling for thinner device layers & packages.

APPLICATION in FO WLP

- Release for “RDL first”.
- Temporary bonding for warpage control for “chip first” enables thinning & backside processing.



Source: Brewer Science

MASKLESS MANUFACTURING ACCOMPLISHES:

TECHNOLOGY SCALING for FINE PITCH PROBE CARDS
- High resolution patterning achieving <2 µm L/S

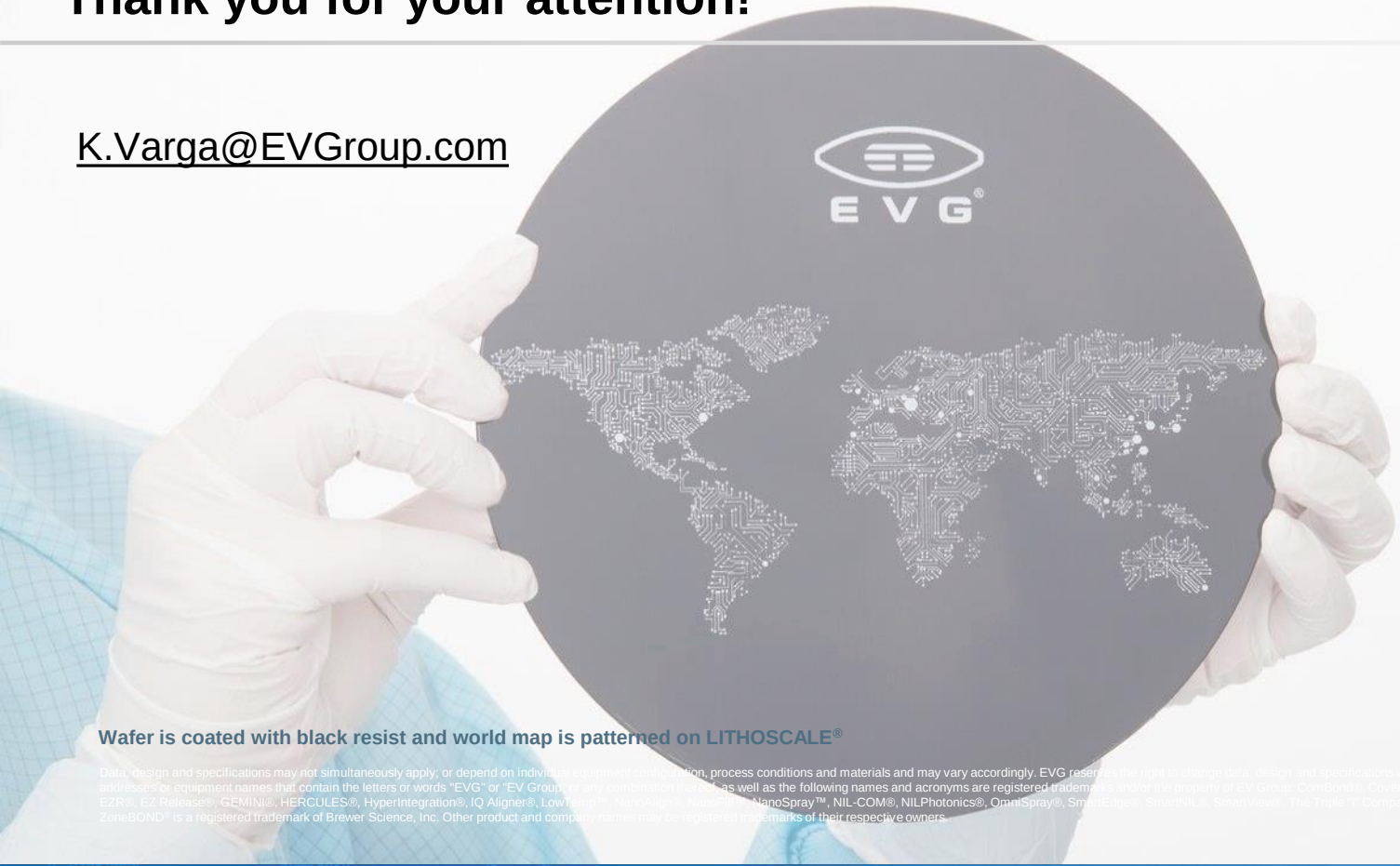
DESIGN FLEXIBILITY
- Layout independent from chip size
- Multi–die architectures, die–level patterning

MARKET LEADERSHIP
- Fast tape–out
- Adaptation to customer needs

- MASKLESS MANUFACTURING ACCOMPLISHES:
  - ECONOMICAL BENEFITS
    - By dual–layer exposure of resists by cutting the lithographic steps.
  - SUSTAINABLE INDUSTRY
    - Short supply chain contributes to low ecological footprint
- Recently launched IR Laser Release Technology
  - Enables cutting the costs through thin layer transfer & elimination of needed glass substrates.

Thank you for your attention!

K.Varga@EVGroup.com



Wafer is coated with black resist and world map is patterned on LITHOSCALE®

Application of Contact Resistance in Parametric Testing

Micron | Intelligence Accelerated™

Iwan Putra Kurniawan
Micron Semiconductor Asia, Singapore

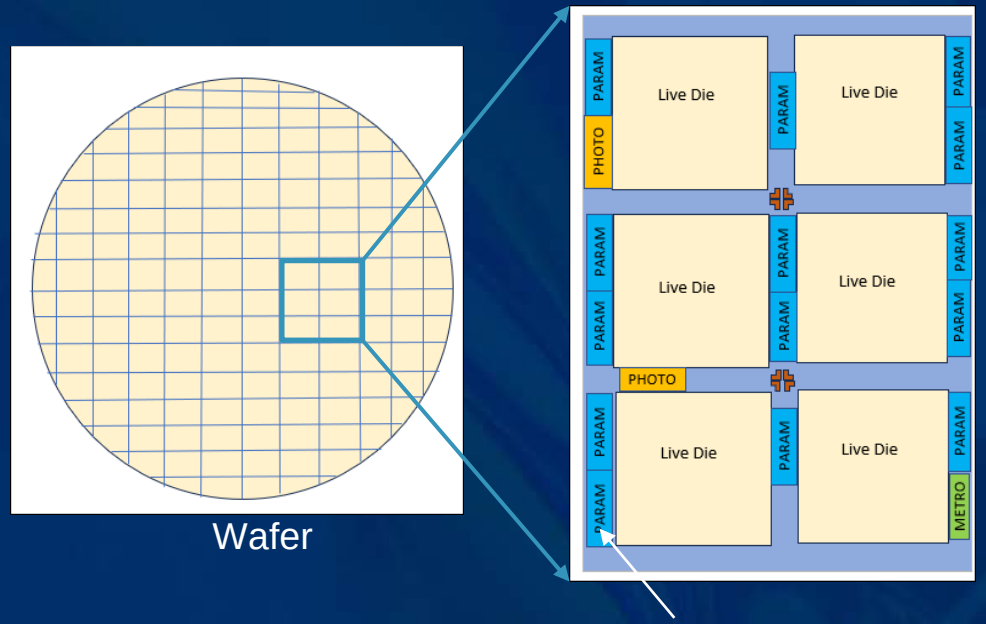
4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

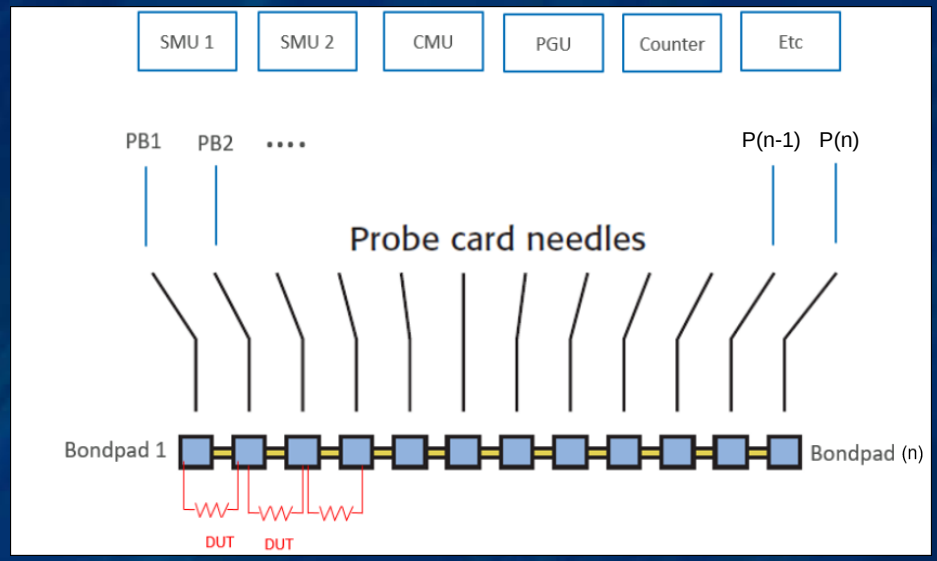
Overview

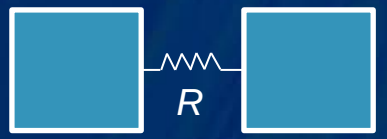
- Parametric Testing in NAND
- 3D NAND Evolution
- Testing 3D NAND Parametric with Multiplexer Module
- Challenges in Troubleshooting MUX Test Fails
- Contact Resistance (CRES) Test as option
- Limitation of CRES and hardware diagnostic
- Summary

Parametric Testing in NAND

- **Functional test is electrical test to check good or bad die.**
- **Parametric test is electrical test to check internal structures.**

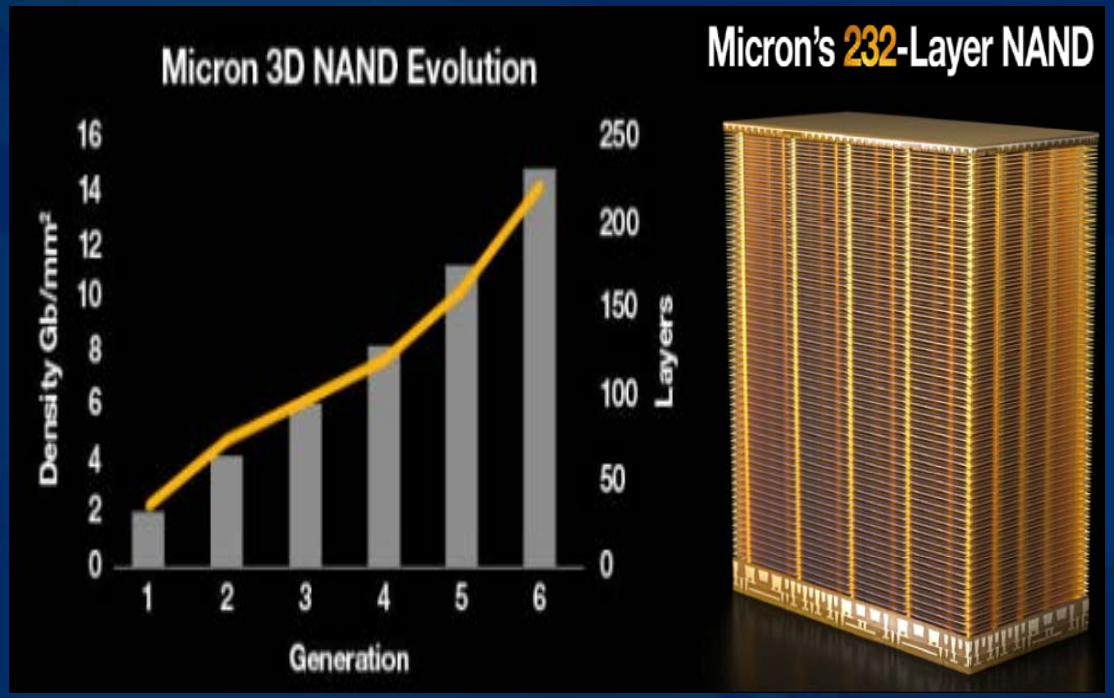




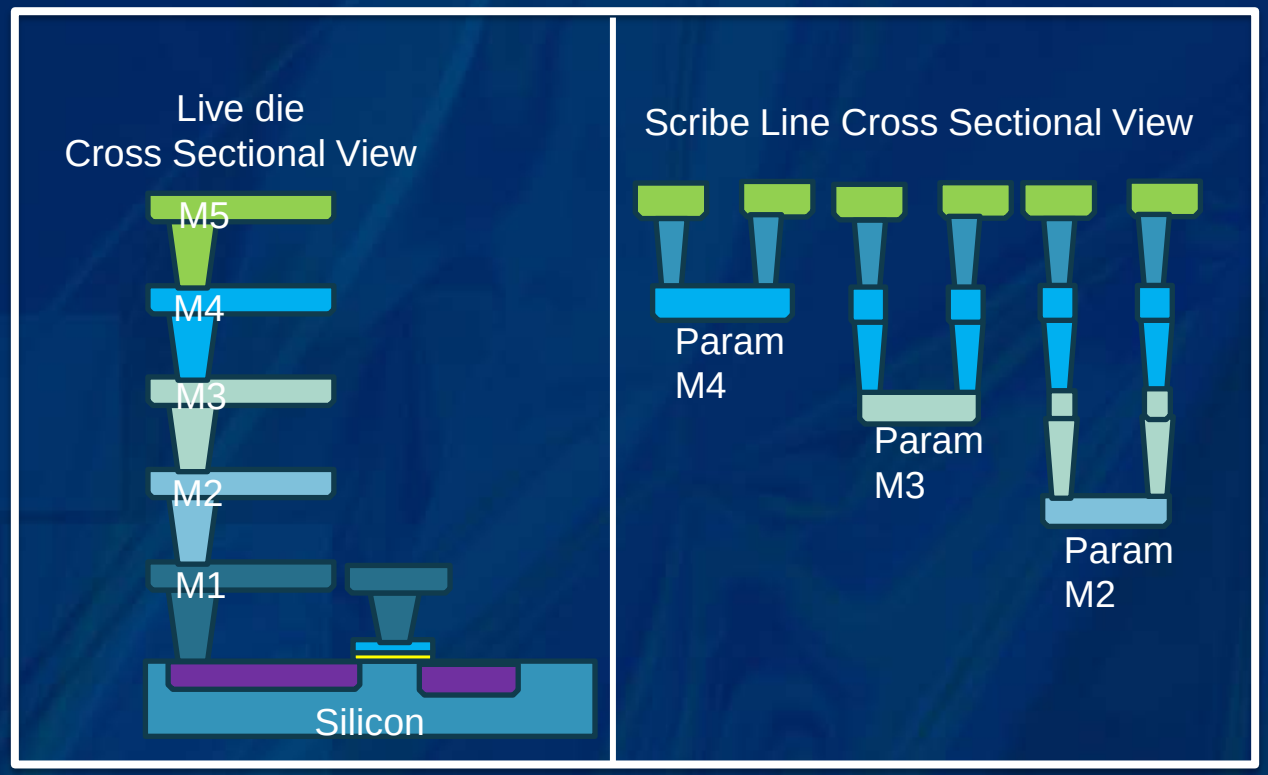


Parametric Test structure

3D NAND Evolution



Micron's 3D NAND Evolution: 232-Layer NAND



Hypothetical diagram, does not represent Micron design.

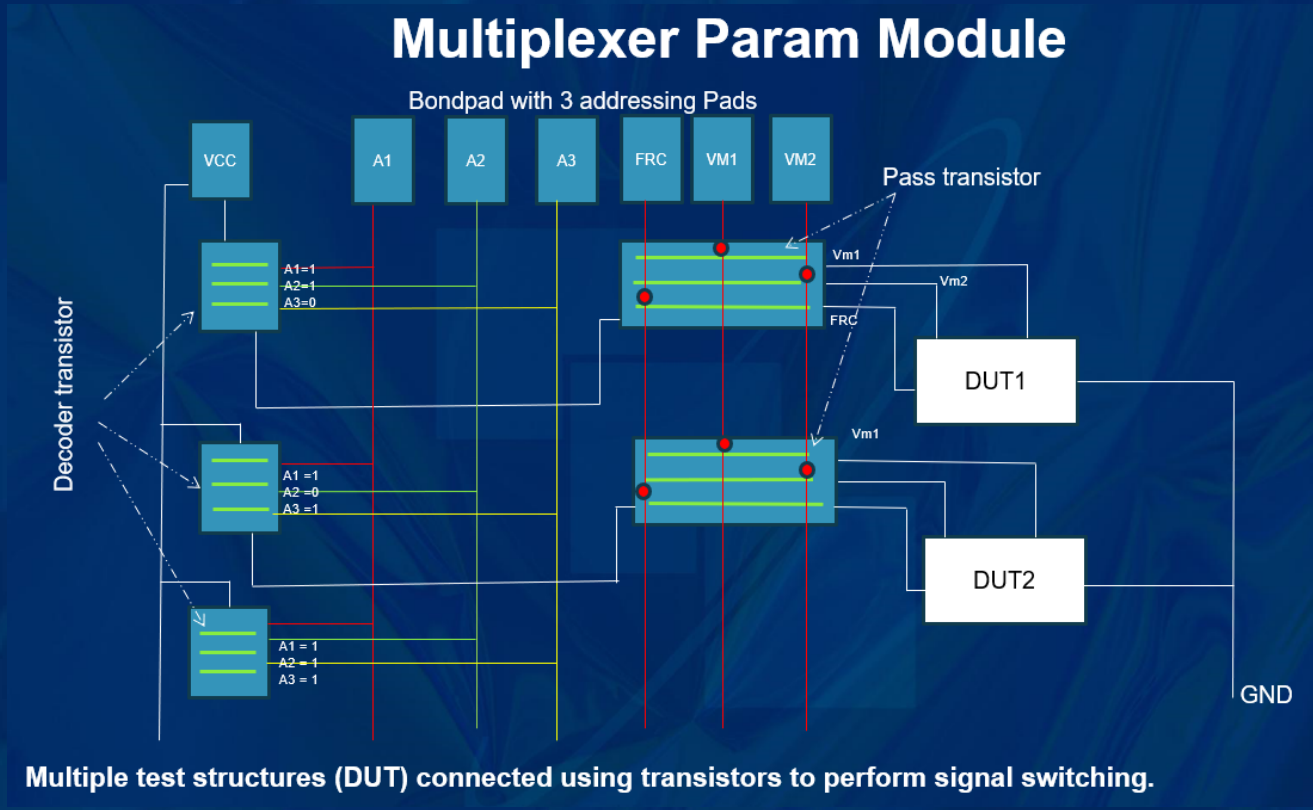
Testing 3D NAND Parametric with Multiplexer Module

- **Param Multiplexer (MUX) module could pack 10X~20X components vs standard module.**

Typical Param MUX Module Test Structure Connection Table

	Address	VM1	VM2	FRC	GND	VCC	Vbb/Vpp	Address High	Address Low
Test Structure 1	11110011	01	02	03	04	05	6&7	8&9&10&11	12 & .. (n-1)&(n)
Test Structure 2	01001001	01	02	03	04	05	6&7	11&13	8&9&10&..(n-1) & (n)
Test Structure 3	00010010	01	02	03	04	05	6&7	10&13 & ..(n-1) & (n)	7&8&9&11&12
Test Structure 4	10110011	01	02	03	04	05	6&7	9&10&12	8&11&13&..(n-1)&(n)
Test Structure 5	10010011	01	02	03	04	05	6&7	10&11&12	8&9&11&13&..(n-1)& (n)

Measurement pads | MUX logic | Addresses



Multiple test structures (DUT) connected using transistors to perform signal switching.

Problem Statement

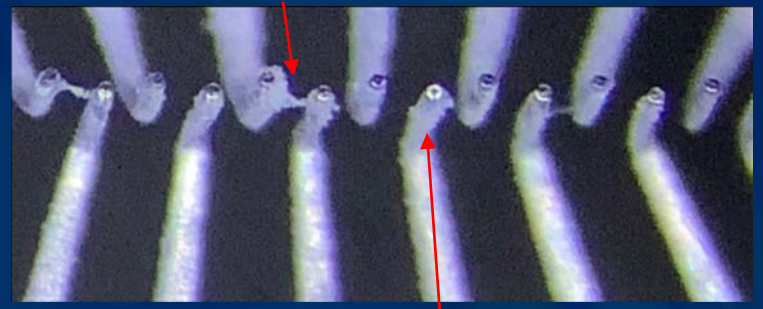
- **Param Multiplexer module poses challenge in diagnosing hardware issues.**
  - It is not straight forward to isolate faulty hardware.
  - Common issues are highlighted and a technique to isolate is illustrated in this presentation.

- **Why couldn’t the hardware self diagnose itself?**

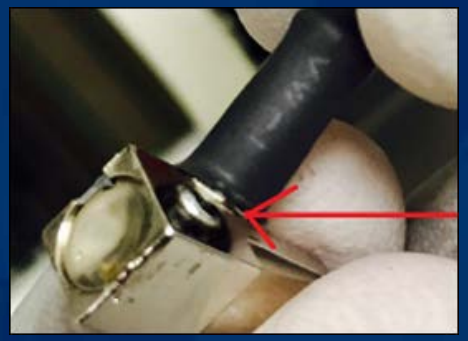
Common Hardware Issues

Probe marks misaligned/ out of bond pads

Dirty

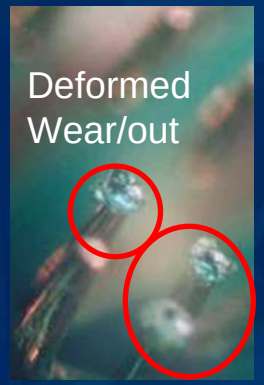


Tip chip off



Loose connector

Bent tip



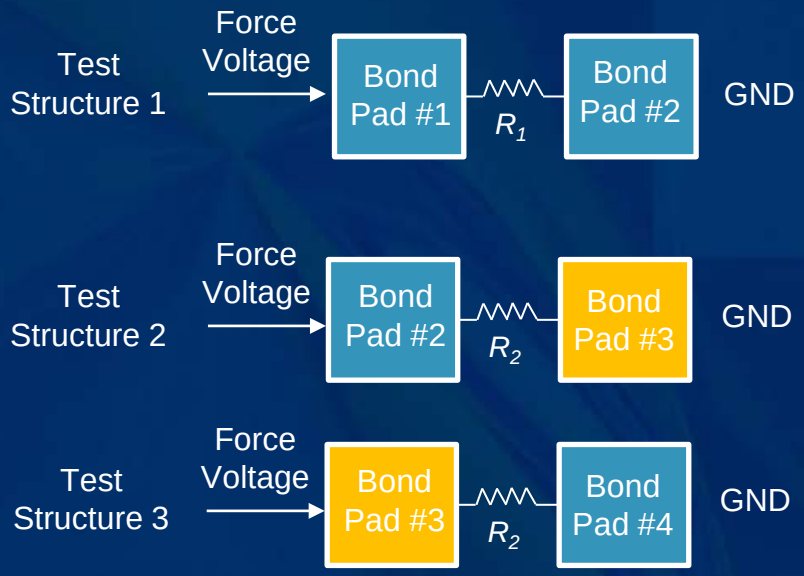
Faulty Equipment / Probecard

- **Mechanical Contact:**
  - Probe marks misalign/out of pad
  - Bent/burnt/deformed tips
- **Electrical Contact:**
  - Tester Board faulty
  - Loose / damaged connector

Pictures do not necessarily represent Micron's production condition

Challenges in Troubleshooting MUX Test Fails

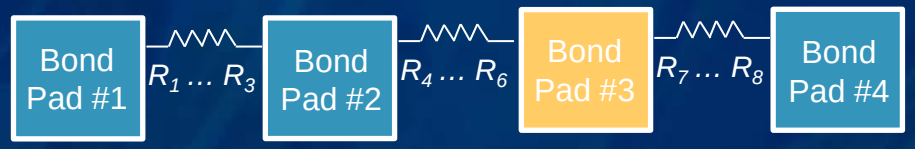
Single Component Module



- **Commonality leads to Pin #3**

Multiplexer MUX Module

Top View



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Test Structure 3	00010010	01	02	03	04	05	6&7	10&13 & ..(n-1) & (n)	7&8&9&11&12

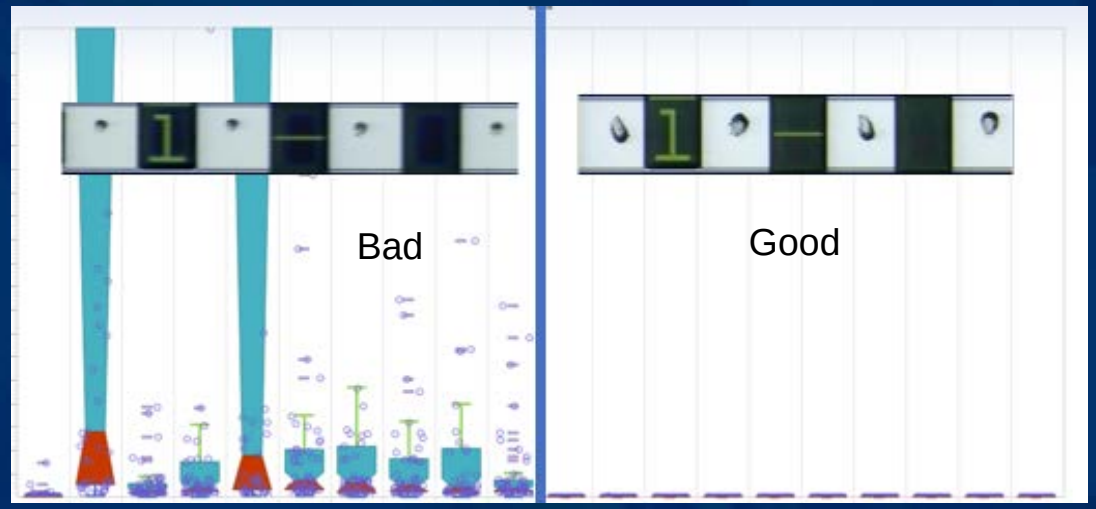
- **Unable to trace which Pin failing.**

Contact Resistance Test as option

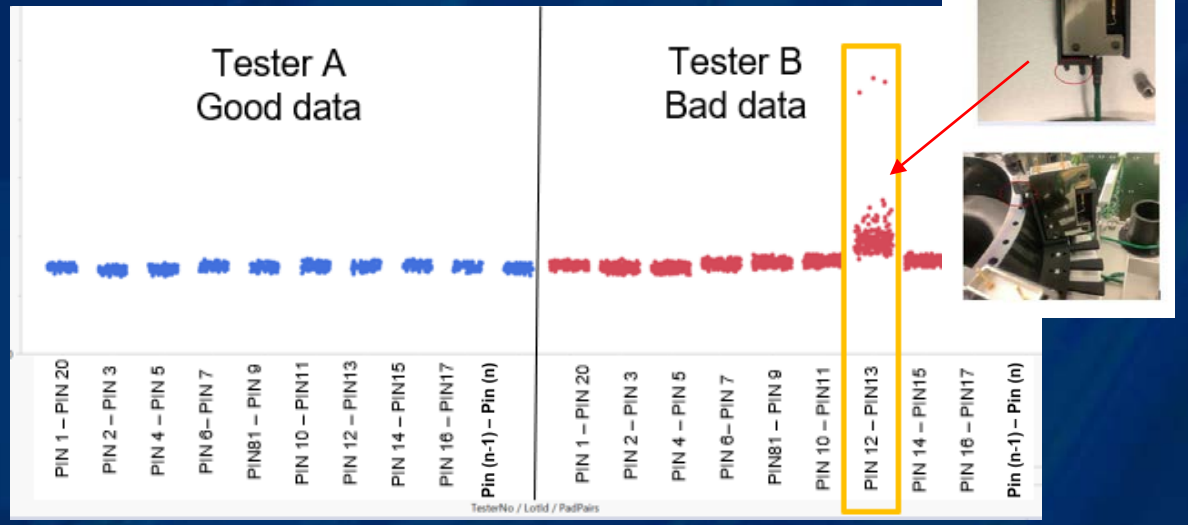
- **One way is to use Contact Resistance (CRES).**
- **What is CRES?**
  - Interface resistance between probecard lead tip and bondpad.
- **Why CRES?**
  - Most Issues are contact related.
  - Direct signal path measurement.
- **How can it help us?**

Example of CRES Application

DETECTION



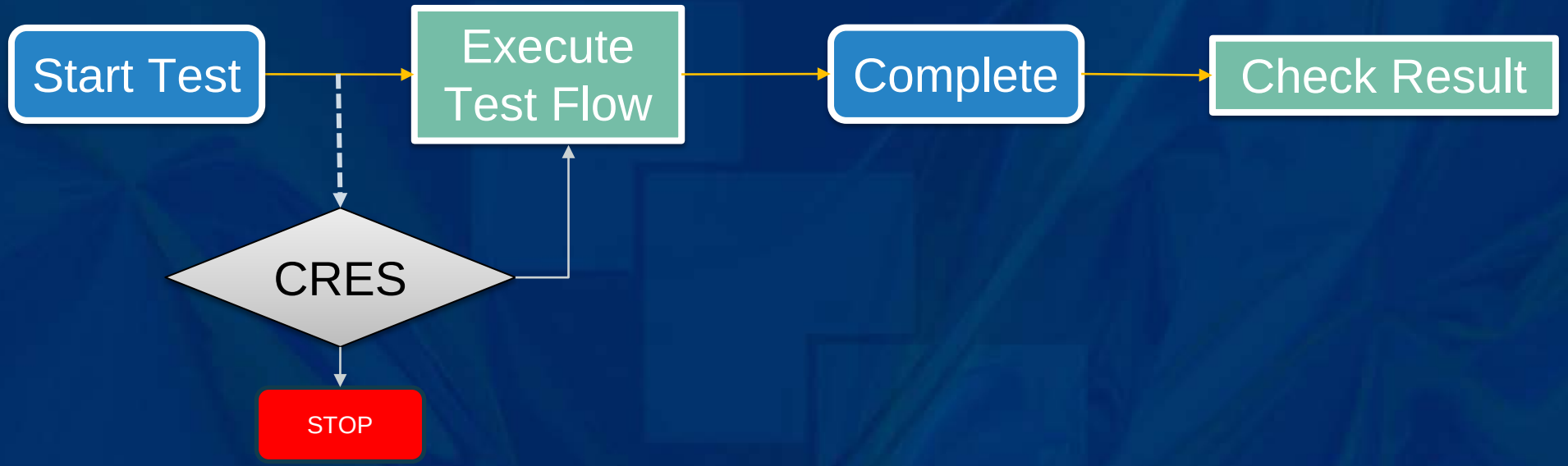
ISOLATION



Pin Board
guide pin bent

- **Examples of Hardware Failure with CRES**

Shift Left CRES



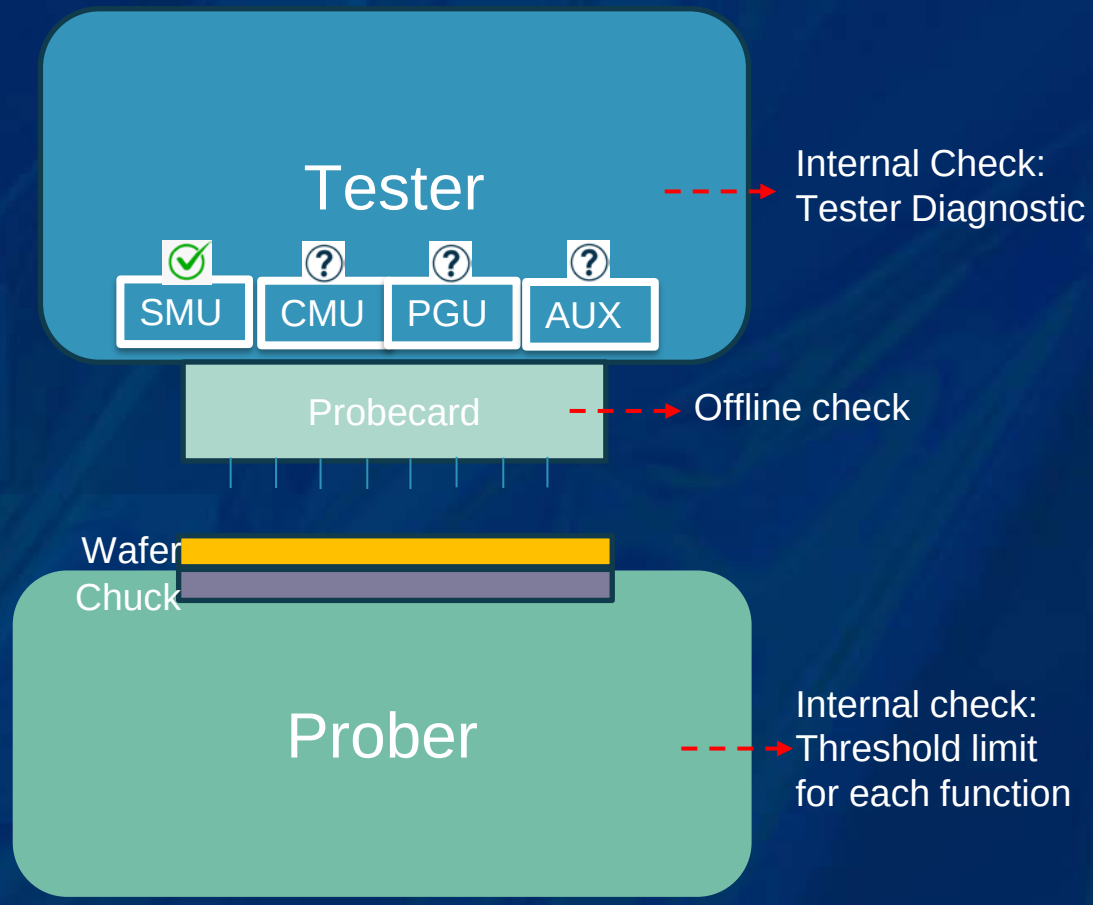
- **Shift Left / Preventive mindset at every run.**
- **Saving capacity and avoiding bad data generation.**

Limitation to CRES and Current Hardware Diagnostic

1. **CRES is not covering all tester resources and requires wafer.**

2. **Tester and Prober performed its own individual self-check, not as one single entity.**

Need new capability from Industry:
Test Cell Integrated Self-Check



Summary

- Multiplexing param test structures helped overcome scribe line real estate constraints.
- Inadvertently caused challenges in Parametric hardware troubleshooting.
- CRES is viable option but not the perfect solution.
- Future Test Cell need to be integrated, smart to self-diagnostic, always good when needed.

THANK YOU!

- **Credits & Acknowledgement:**
  Micron Technology : Dave Peterson, Randy Cleverly, Gary Southern, Salil Mujumdar, Low Kar Loong, Thiam Seng Yip.

SiC, GaN and more: Probing Technologies for HV-HC Power Devices

Dr. Rainer Gaggl
T.I.P.S. Messtechnik GmbH

4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

Overview

- Intro: power devices
- Probing challenges: High Voltage, High Current
- Arcing suppression: LuPo pressure chamber technology
- High Current – contact technologies
- Overcurrent and "burn" protection: SmartClamp
- Single-site vs. multi-site wafer test
- Known Good >>POWER<< Die (KGD)
- Summary and Outlook

Power Devices


photo courtesy: Wolfspeed

- **Where are these used ?**
  - Electric Vehicles (EVs): cars, trains, ships, (future)aircraft...
  - Renewable Energies – solar, wind, hydrogen
  - Efficcient power supplies: computing, chargers, mobile...

- **Types**
  - discretes: MOSFETs, IGBTs, Diodes,
  - ICs: gate drivers, switching power supplies

- **Why SiC, GaN?**
  - very fast switching with little power loss, allows for
  - much smaller and energy efficient circuits

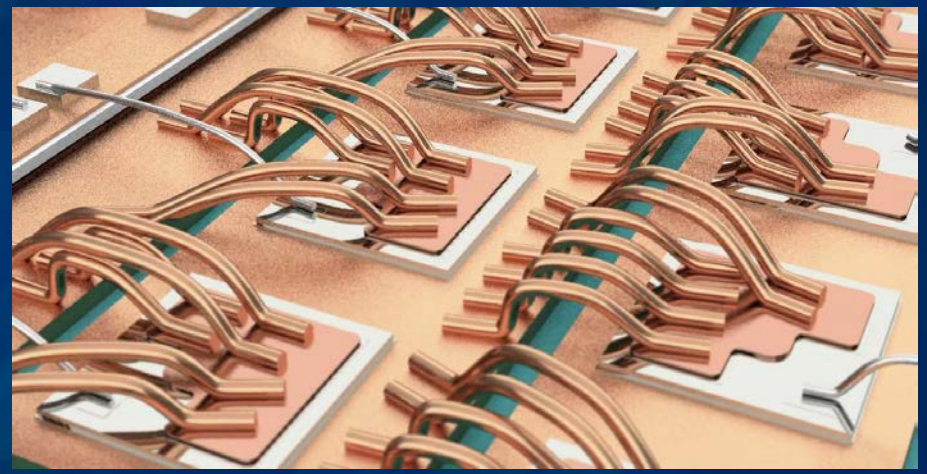
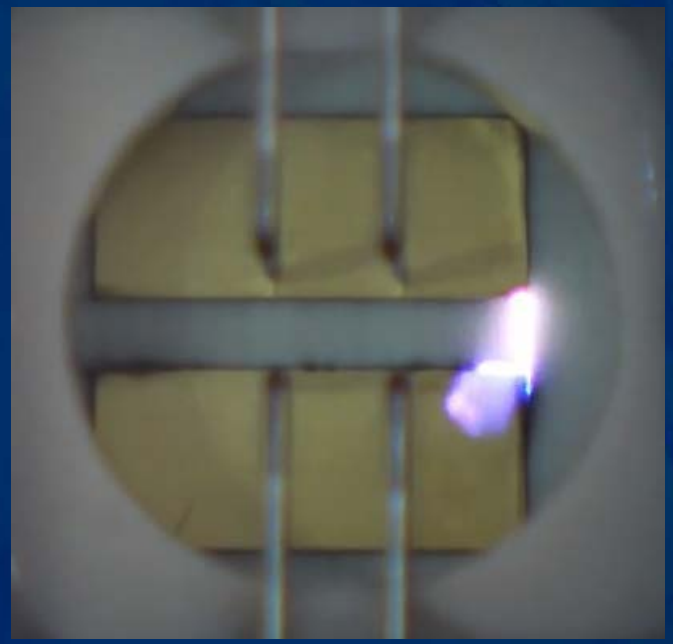


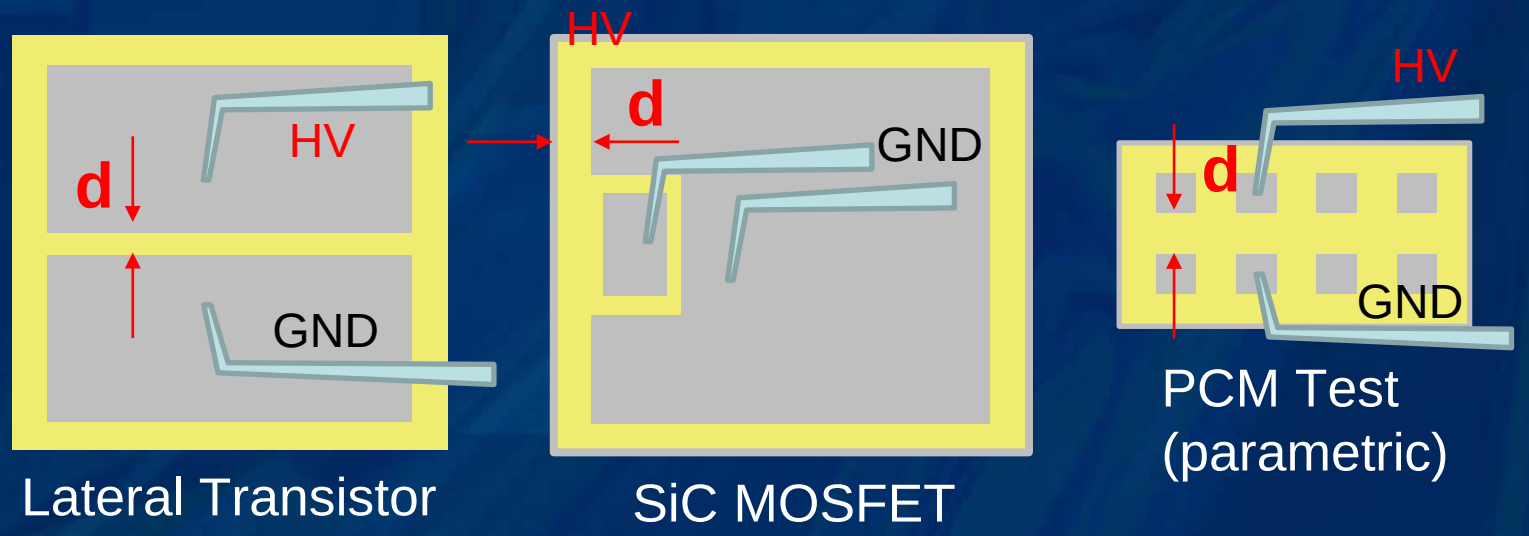
photo courtesy: ABB

- **Why still Si?**
  - extremely robust and well proven: IGBTs, Diodes for automotive and industrial drive trains

Probing Challenges: High Voltage

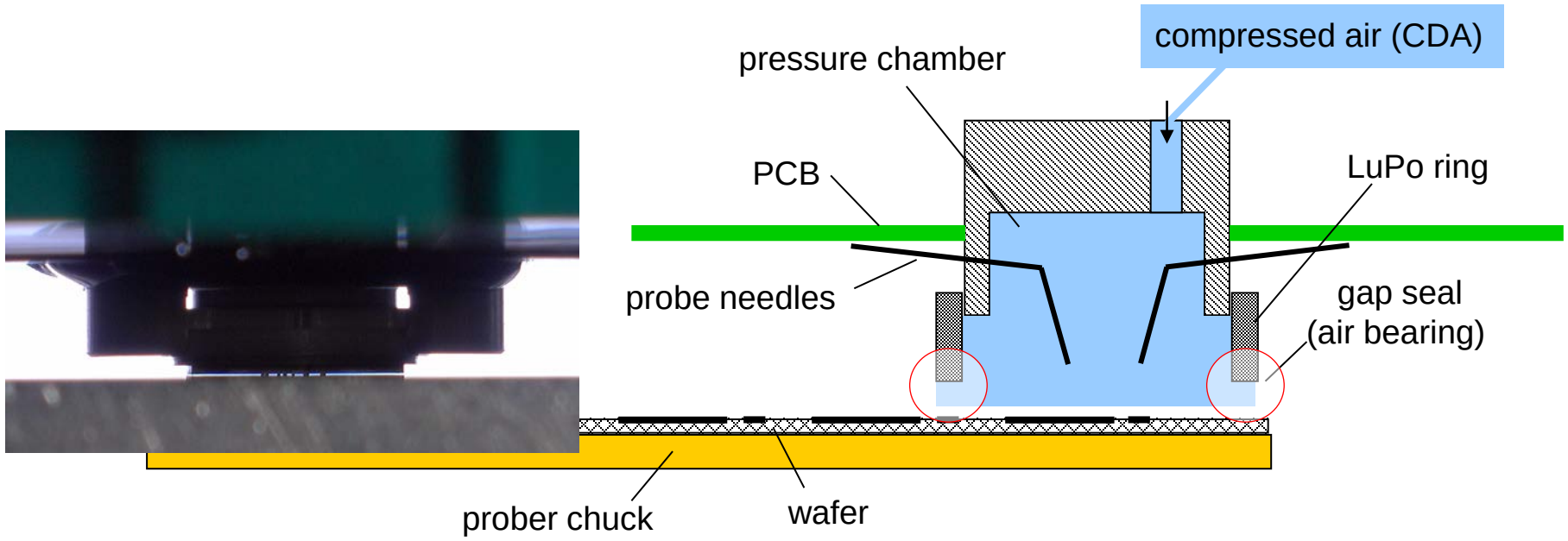
- **High Voltage Arcing**
  - test voltages: several 100 V to several kV
  - SiC and GaN: "wide bandgap" semiconductor material allows for narrow HV structures (distance **d**) compared to traditional Si devices
    -> high arcing risk at wafer probing or at KGD test





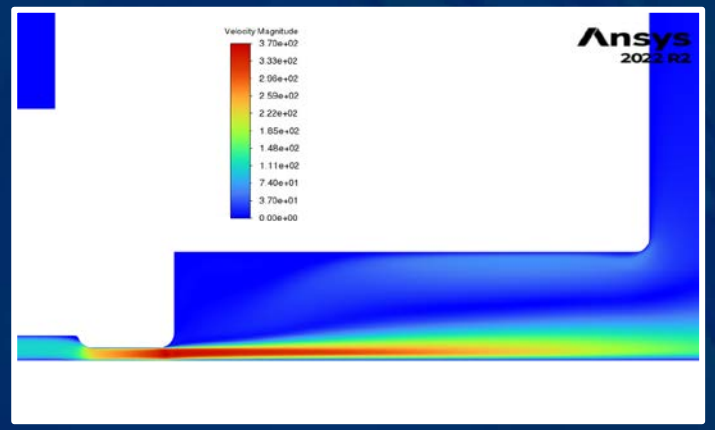
Arcing Suppression: LuPo technology

- **"Applied Paschen": chip-scale pressure chamber**
  - uses compressed air (CDA) to suppress arcing
  - environmentally "green"
  - low operating cost



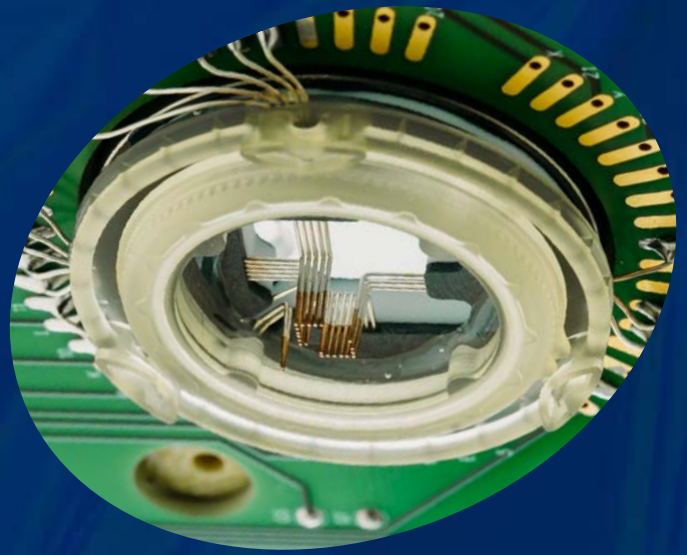
LuPo Technology – Insights...

- **Air-Bearing-Seal (LuPo-ABS)**
  - LuPo floats on air cushion – NO TOUCH of wafer surface
  - Auto-z align, insensitive to overtravel setting and probe tip wear
  - Latest version "Gen.4" - applied CFD simulation and 3D printing technology: optimized floating and pressure buildup, low noise and CDA consumption, insensitive to wafer-born particle contamination



CFD simulation for the LuPo air bearing structure

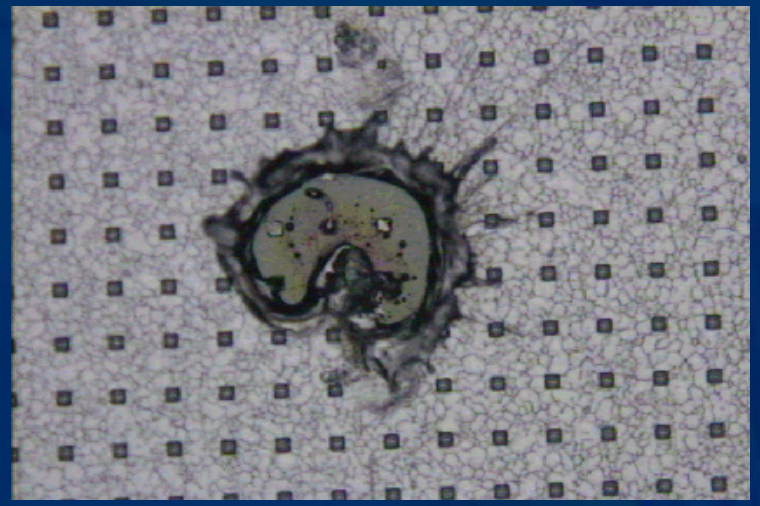
NO TOUCH: LuPo contacting motion



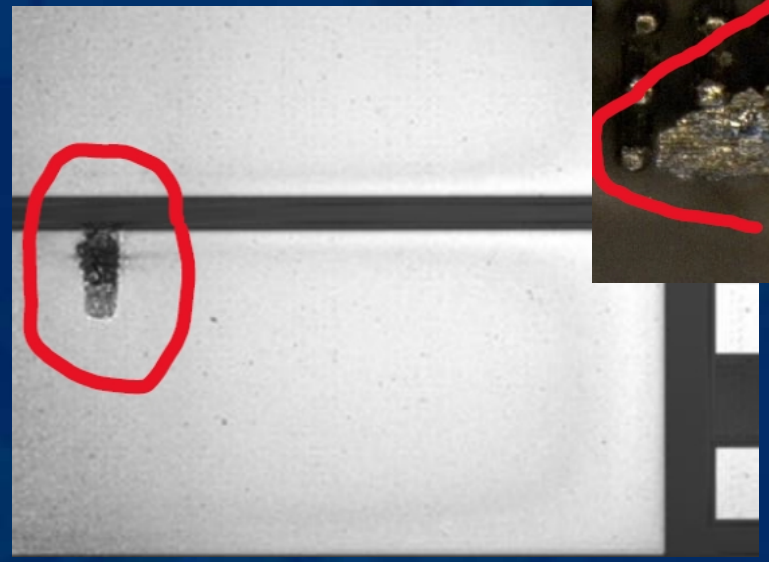
LuPo "Gen.4"

Probing Challenges: High Current

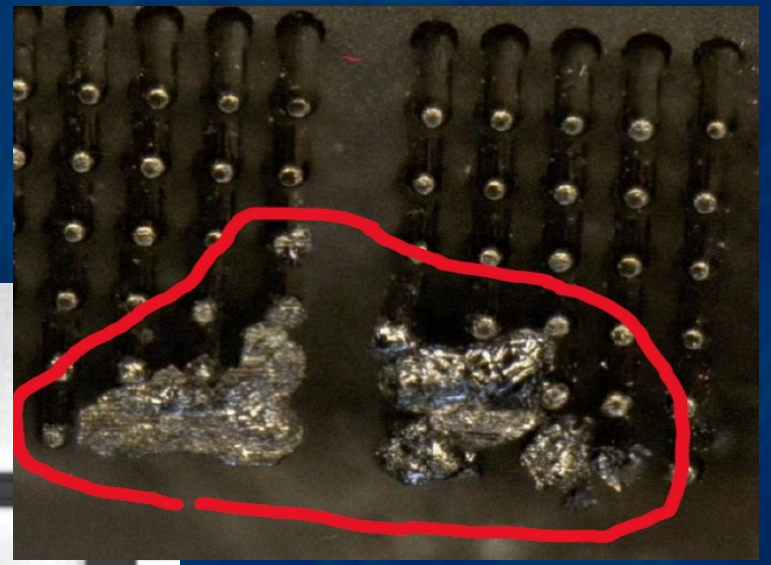
- **"Chip burn", probes damage**
  - test currents: a few A to 3000+ Amps!



molten chip pad on IGBT (wafer test, cantilever probes)



"chip burn" (KGD test)

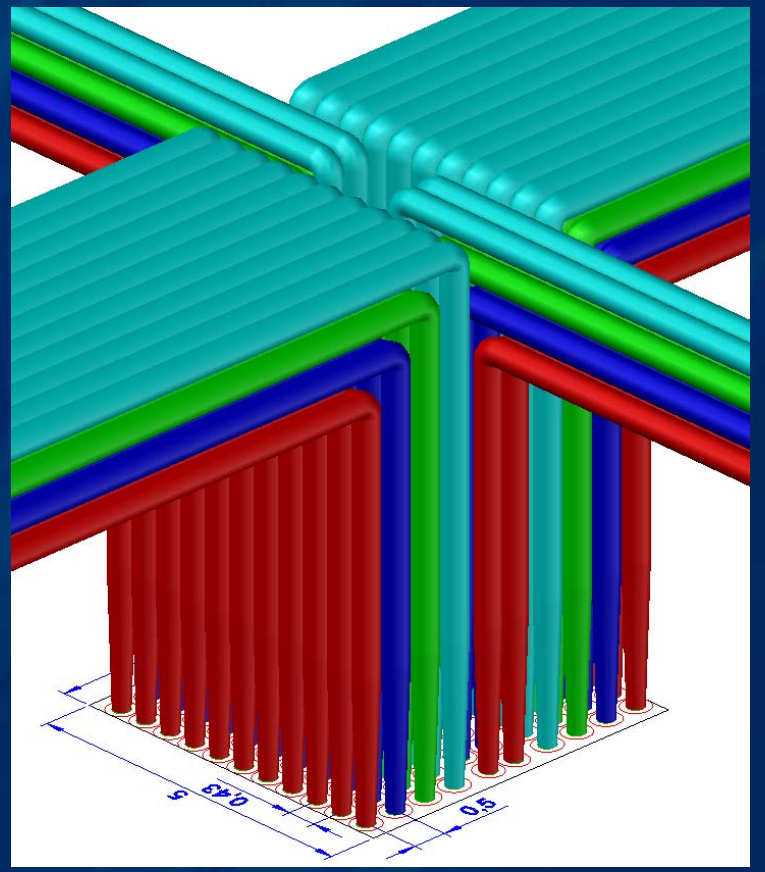


chip metal fused to HC vertical probes (KGD test)

High Current – Cantilever vs. Vertical (1)

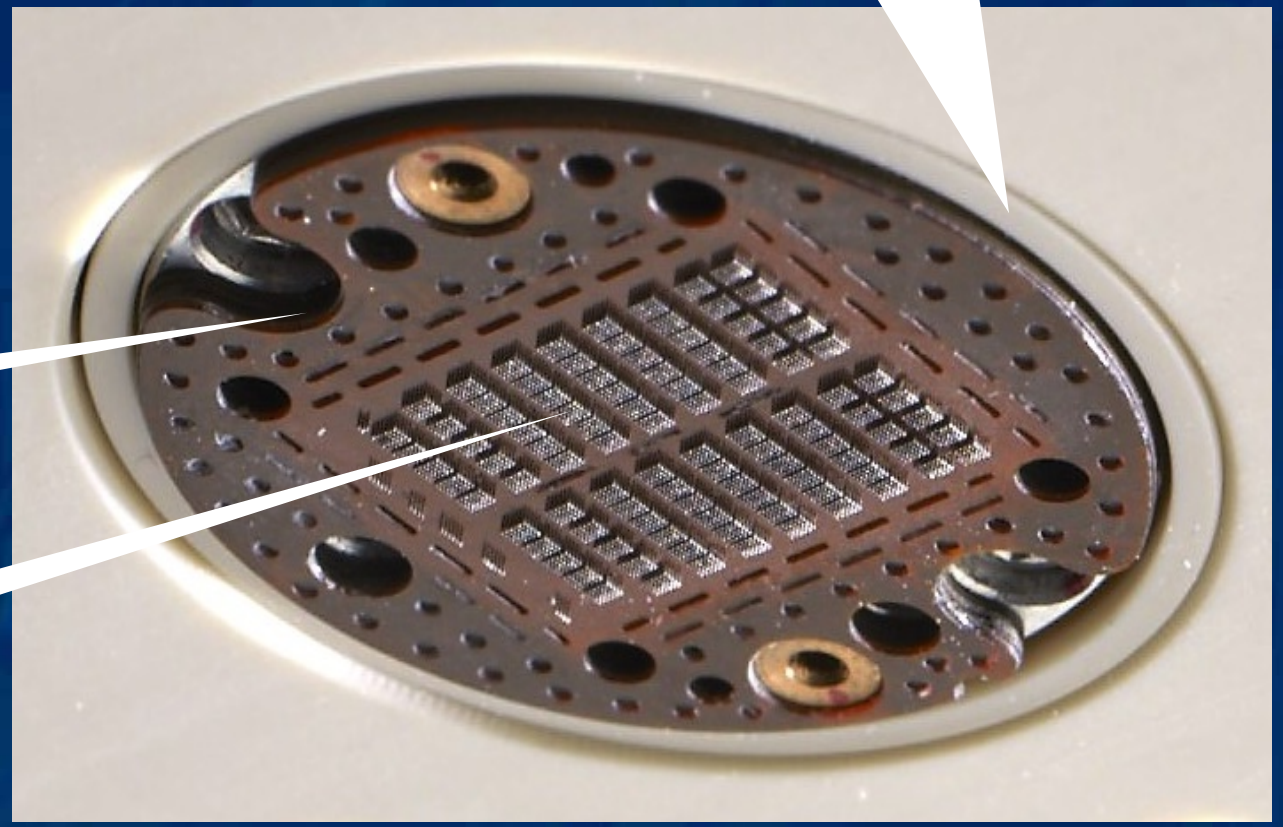
- **Cantilever probes technology: the robust "workhorse"**
  - limited max. current density ~ 40 A/mm^2 might be too low for SiC power devices
  - good choice for Si-IGBTs, diodes
  - comparably low cost

1600 A Cantilever probe card for IGBT



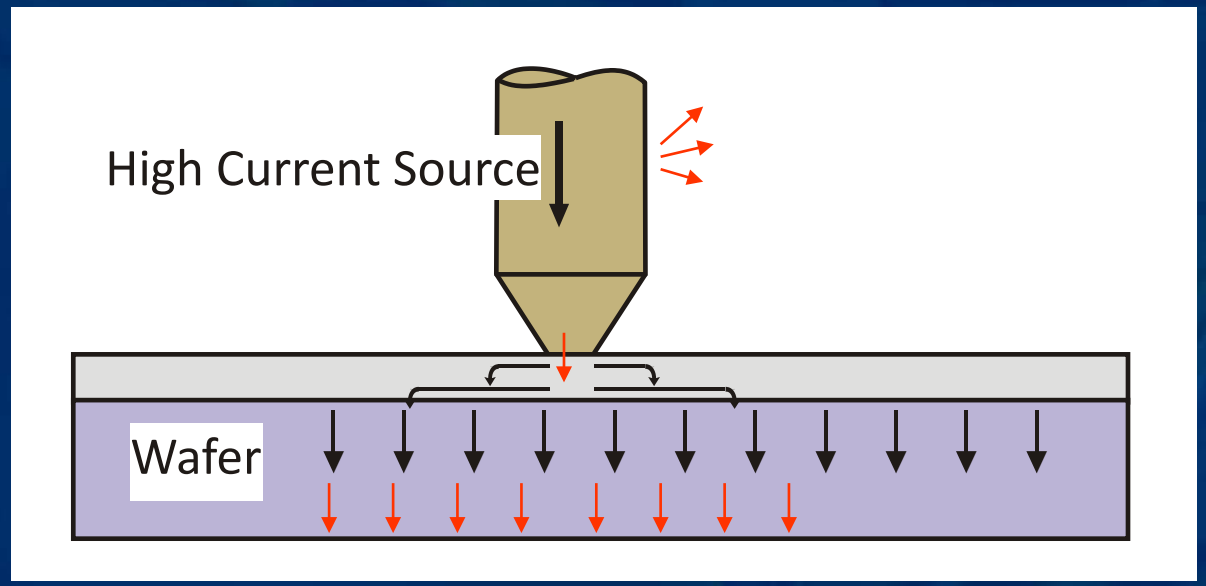
High Current – Cantilever vs. Vertical

- **Vertical probes technology: highest current densities**
  - highest current density: 80+ A/mm^2: SiC, AC tests for KGD
  - very homogeneous current distribution over chip surface
  - small and shallow probe marks
  - well proven "buckling beams"
  - allows for small pad sizes (SiC, GaN based ICs, PCM...)

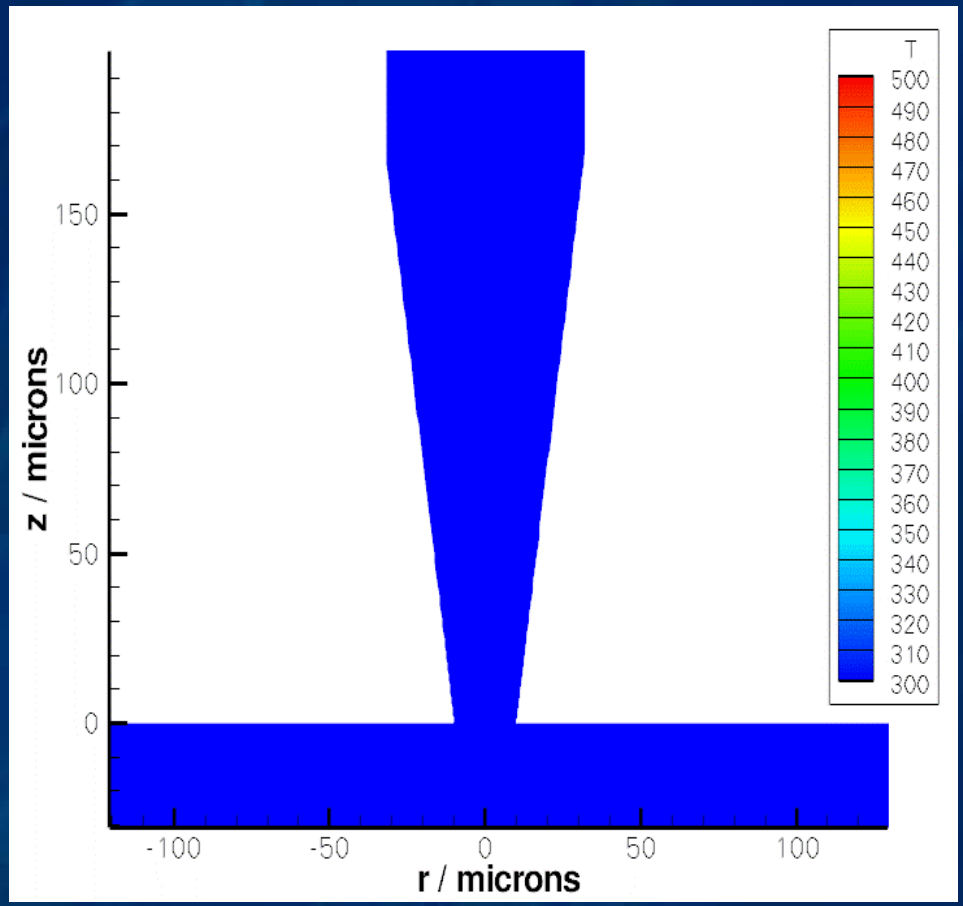


High Current – "Burn Protection"

- **First steps: knowing what's going on...**
  - electro-thermal simulation of probe-wafer
  - for short high current pulses
  - include contact resistance model (Cres)
  - lab verification

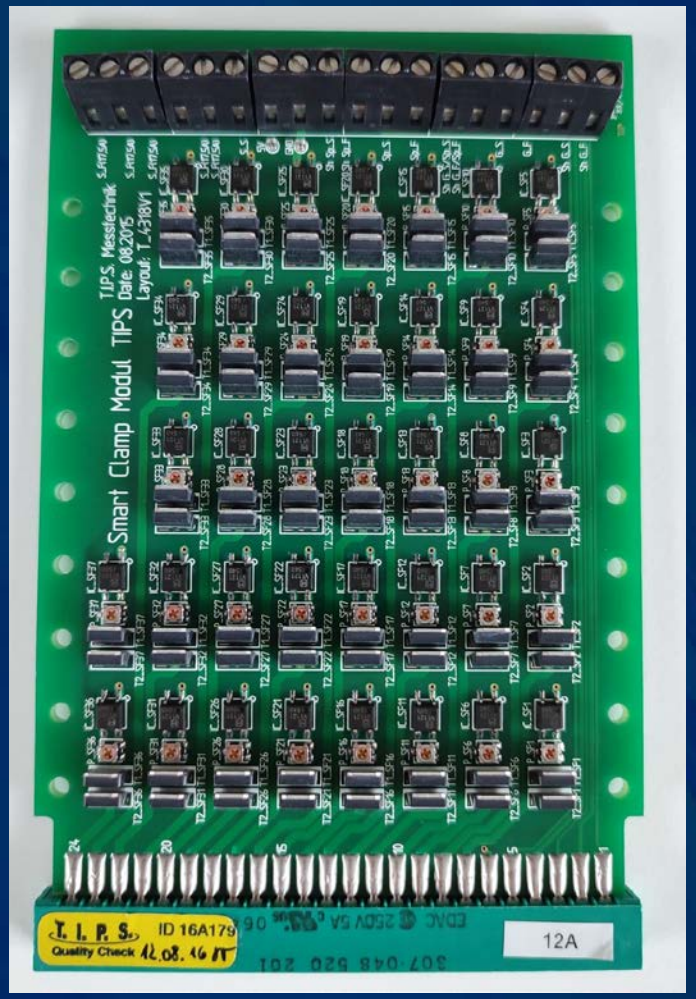


electro-thermal modeling of probe-wafer system



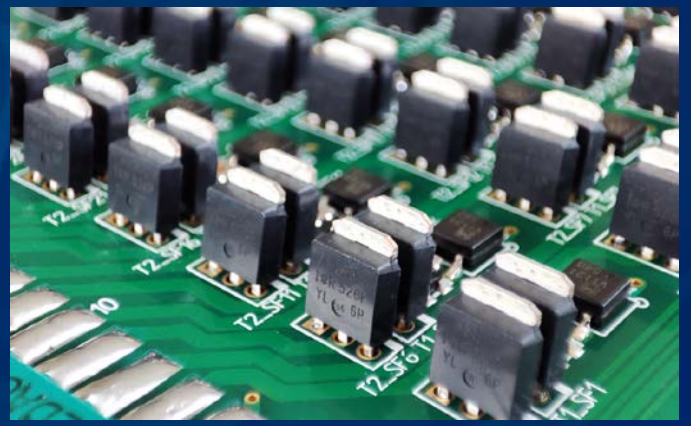
FEM simulation: (vertical beam) probe tip and pad heating high current pulse train 10x 3 ms / 2A

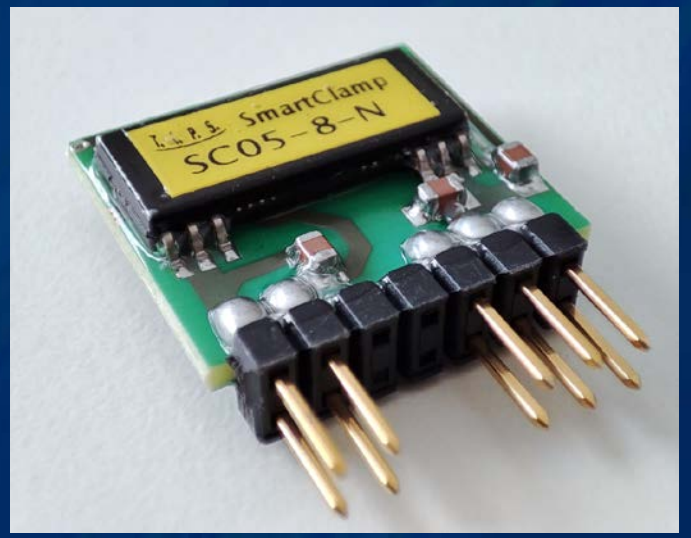
SmartClamp – Overcurrent Protection



370 A SmartClamp Module

- Probe protection circuitry for TIPS High Current probe cards.
- protects each probe (or groups of probes)
- prevents probe / pad contact current overload caused by imbalanced probe currents or tester overshoot
- Active current balancing
- bi-directional current protection

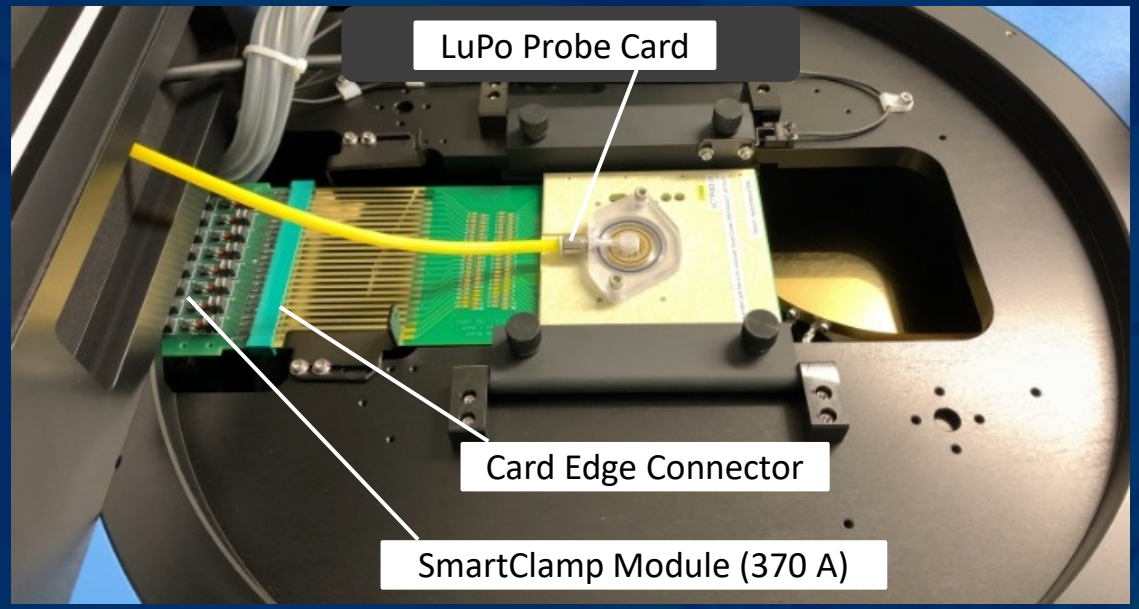




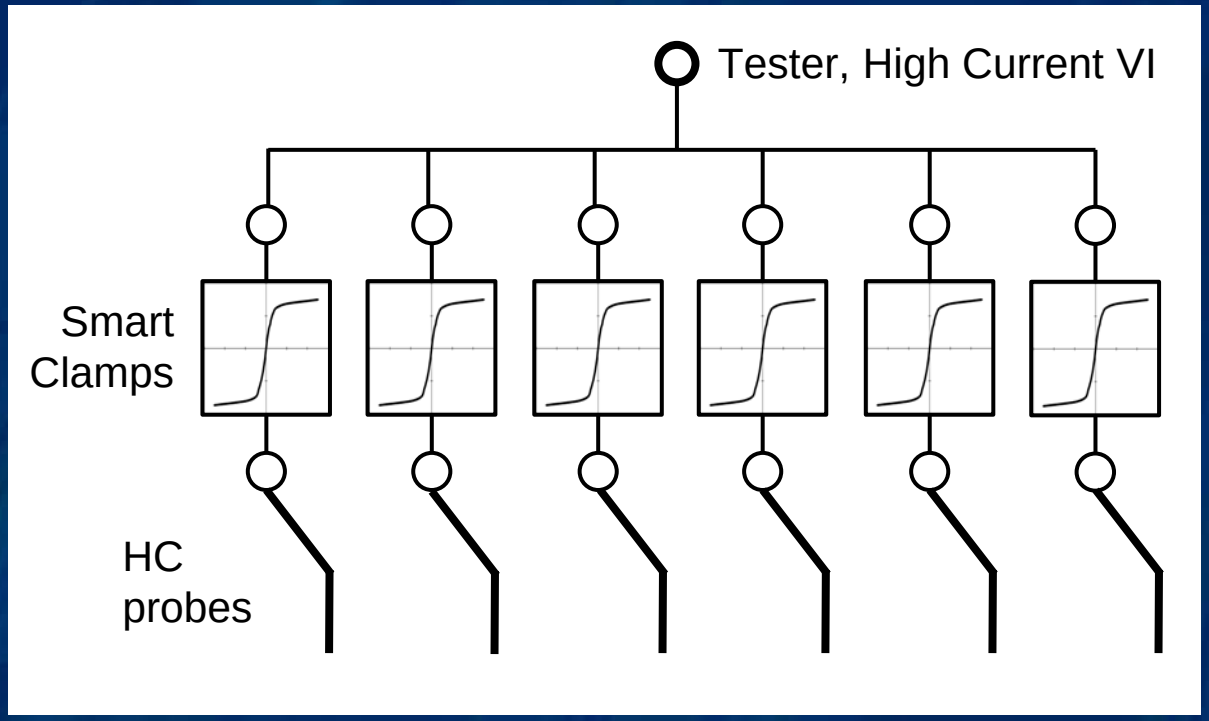
SmartClamp for Load Boards

SmartClamp – Implementation

- **Probes Protection**
  - connected in series to each probe (Cantilever) or cluster of probes (Vertical)



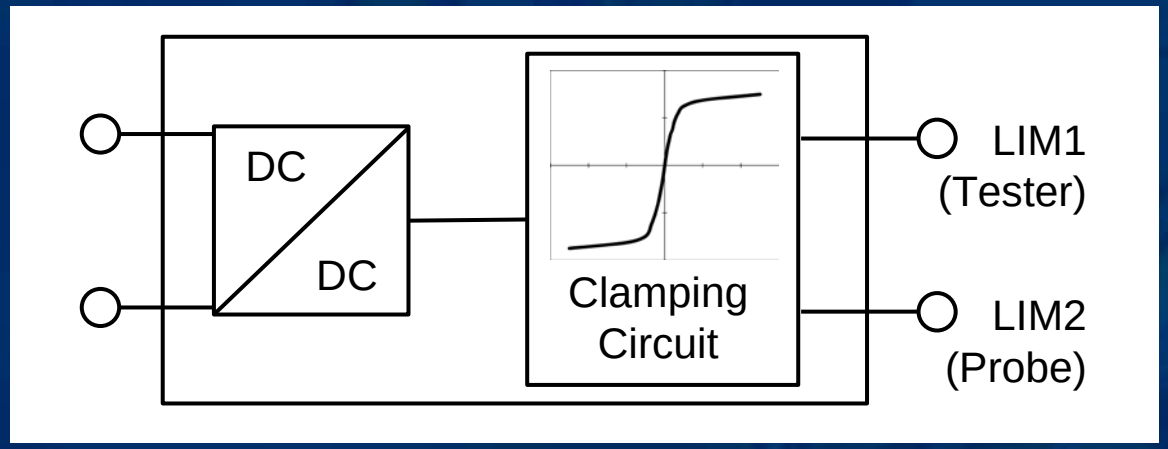
SmartClamp Module 370 A
setup with probe card on Accretech UF2000 prober



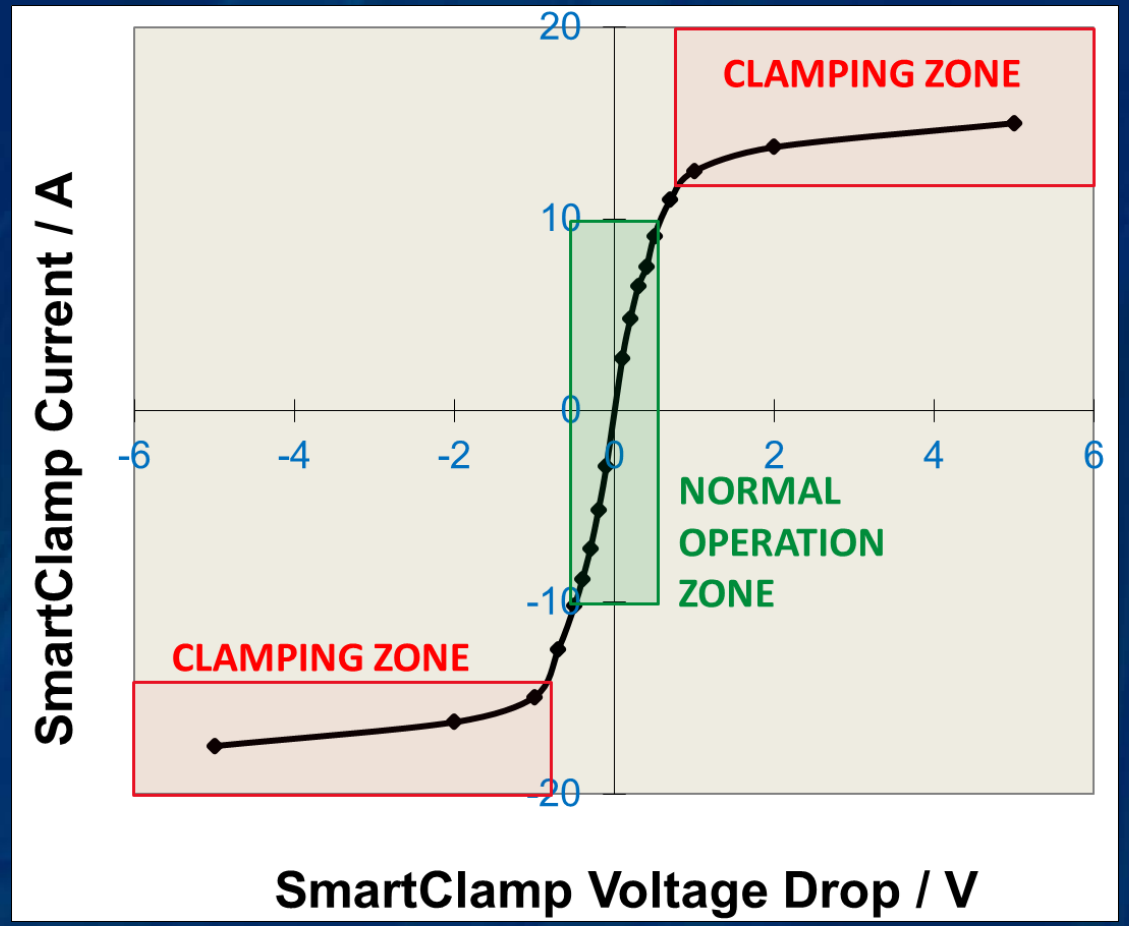
SmartClamp – implementation into test setup

SmartClamp Technology – Insights...

- **Basic Functionality**
  - low-resistive within safe probe currents
  - limits max. probe current to prevent burn
  - insulated from supply power:
    easy to integrate into tester setups



SmartClamp – functional schematics



SmartClamp – electrical characteristics

High Power...Going Multisite

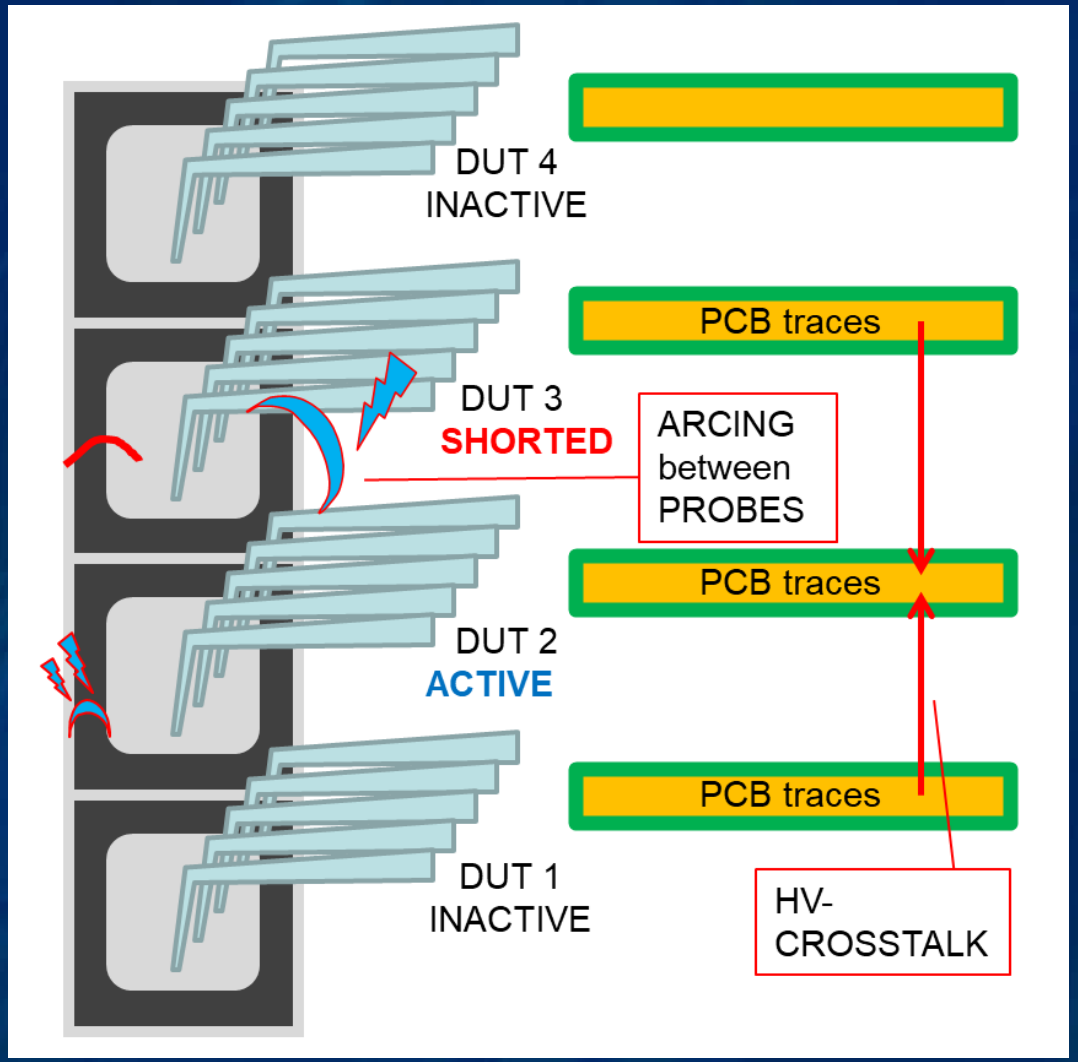
- **Example: HV Power Diode – 4x MULTI**

Considerations

- Additional arcing path between probes / sites !
- HV crosstalk from adjacent sites
- Safety aspects: traces present on probe card PCB might get connected to HV

-> Can be avoided / minimized by

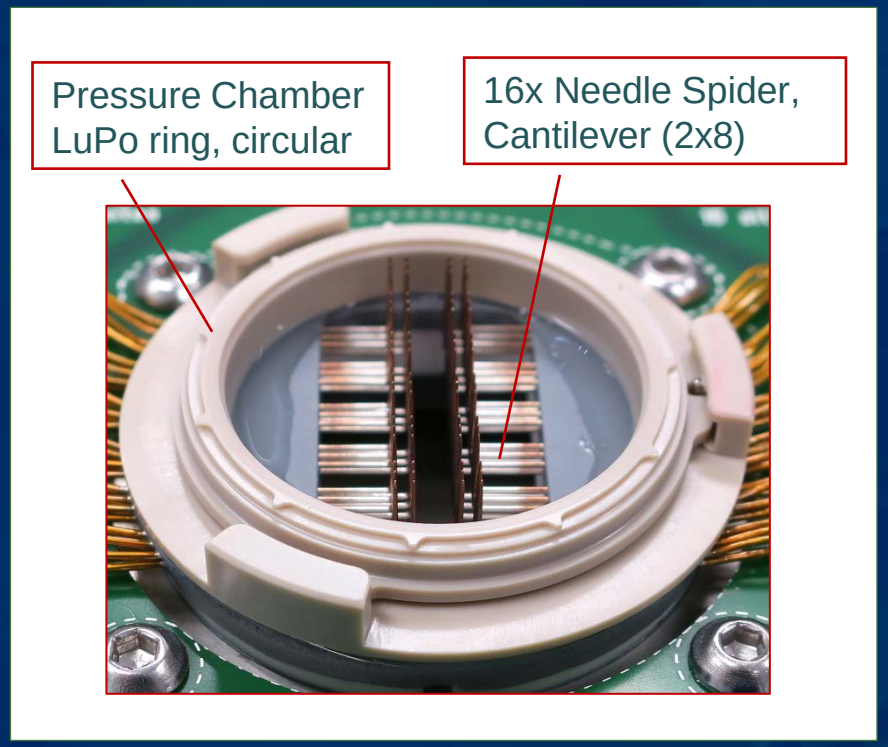
- proper probes layout using HV design rules
- appropriate PCB design techniques
- HV safety enclosure for prober / tester setup



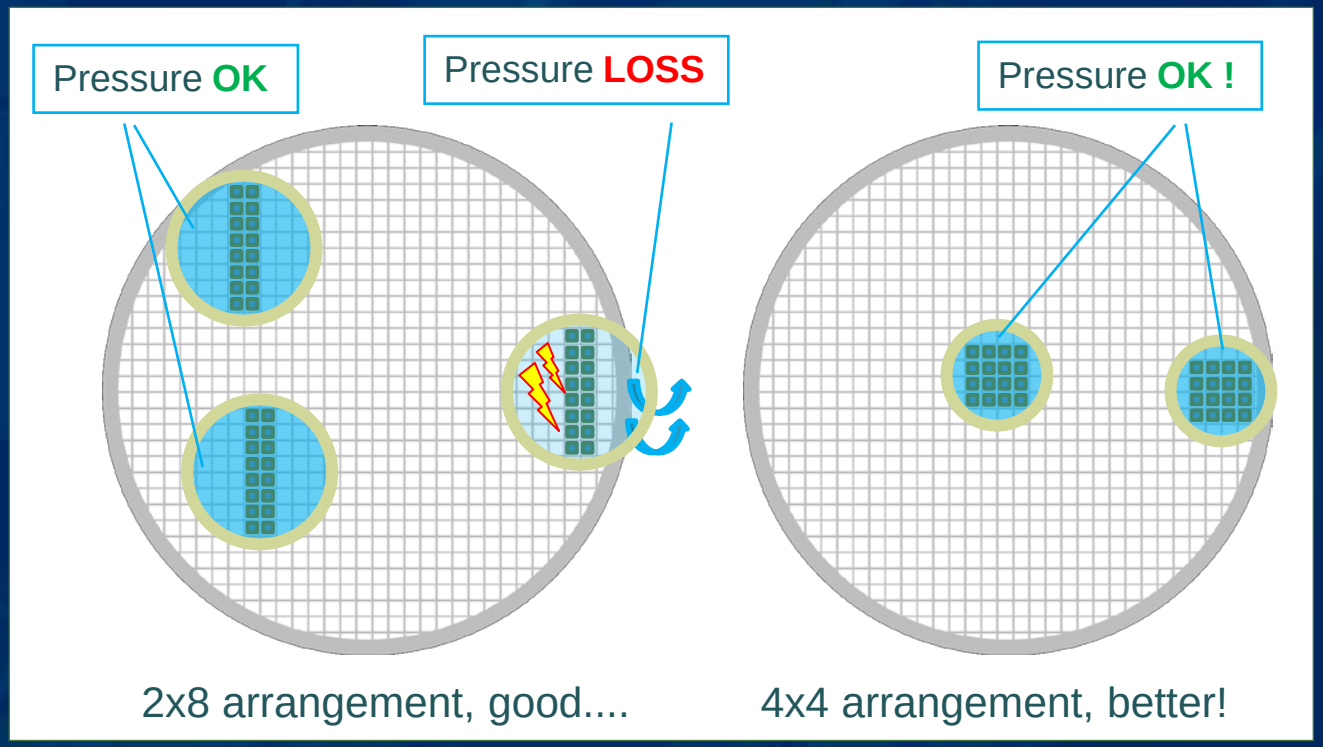
*) For details see conference proceedings SWTest 2023, San Diego

Multisite Test Coverage ... Design Aspects

- Depending on multi-site DUT arrangement there might be a certain "overhang" of the pressure chamber w.r.t. DUT arrangement - compromising LuPo pressure build-up
- This might lead to non-testable chips near the wafer edge



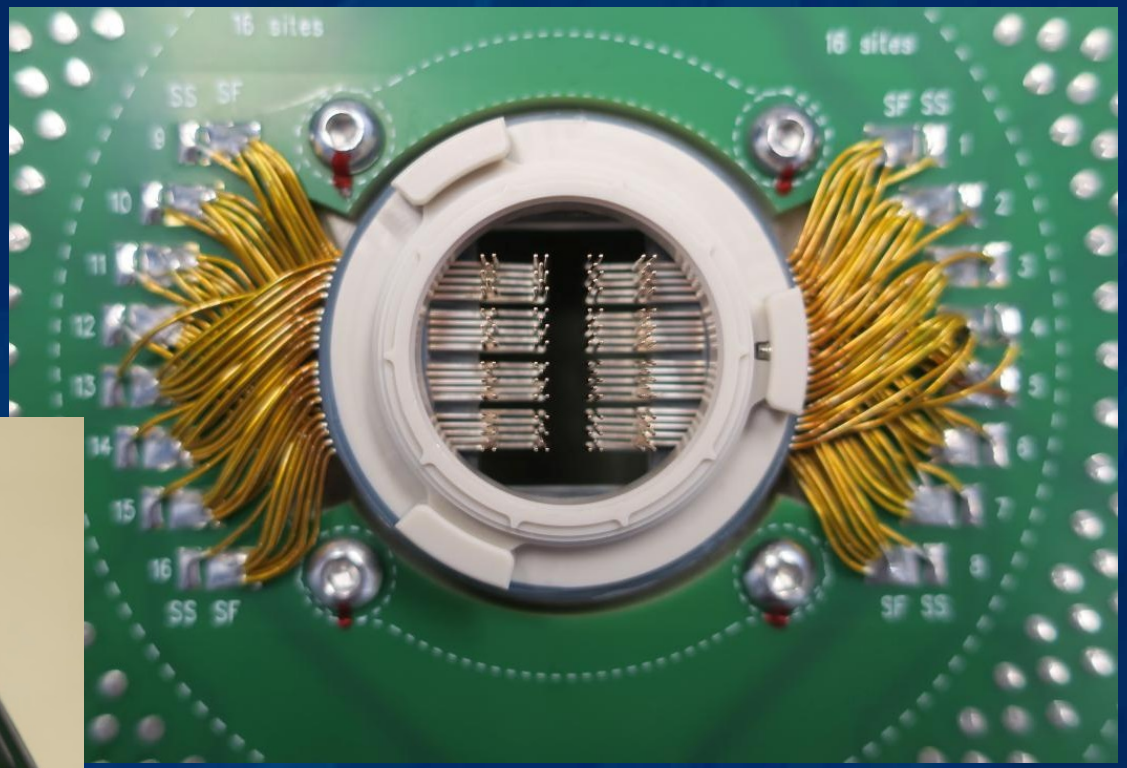
16x LuPo probe card, Cantilever probes

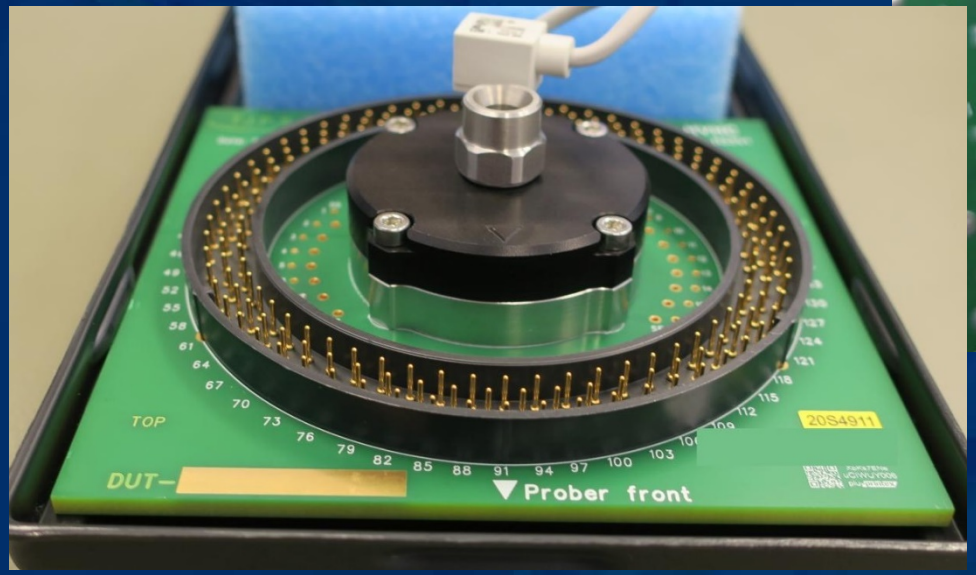


wafer edge contacting and LuPo pressure buildup

Multisite Probe Cards – Cantilever 16x

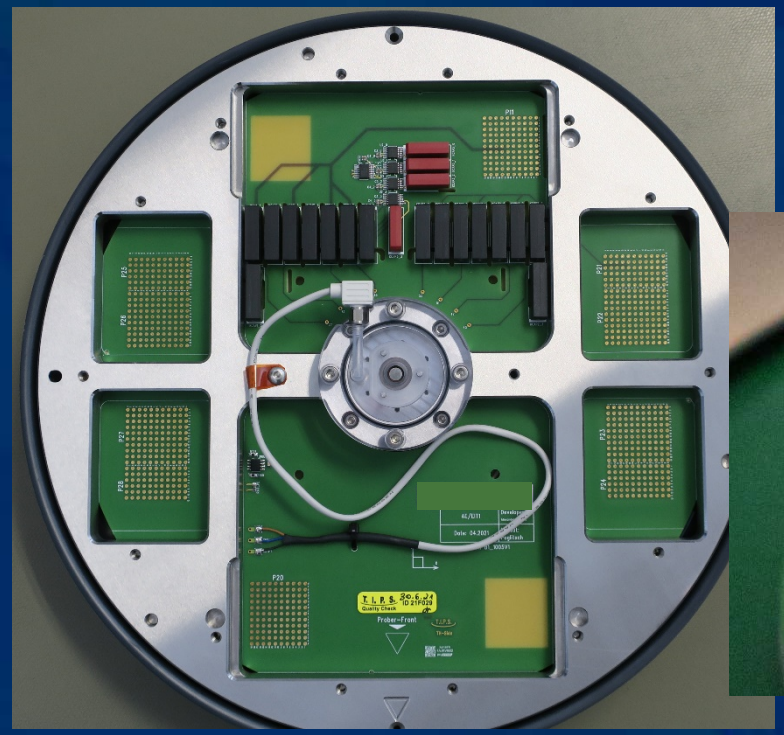
- **SiC diode, 1.6 kV, 45 A**
  - 4x4 arrangement
  - chamber pressure: 2.6 bar
  - auto compressed air docking
  - chamber pressure monitor



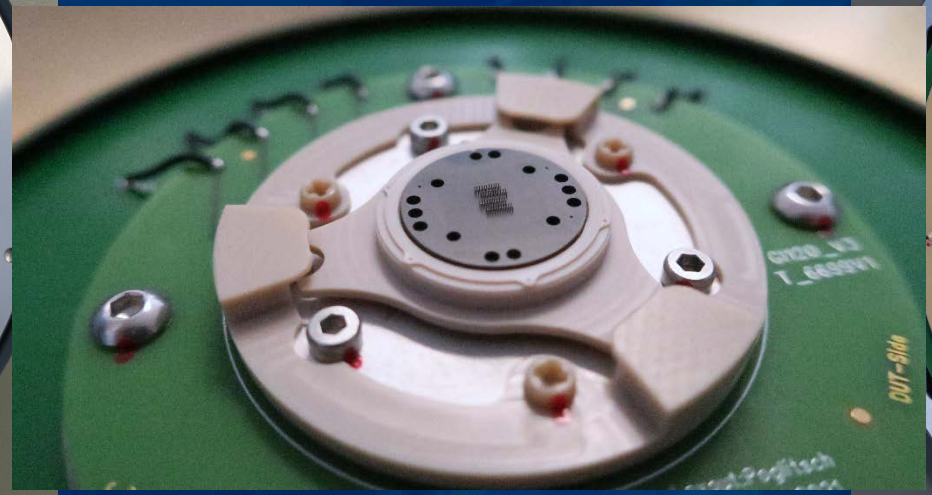


Multisite Probe Cards – Vertical 4x

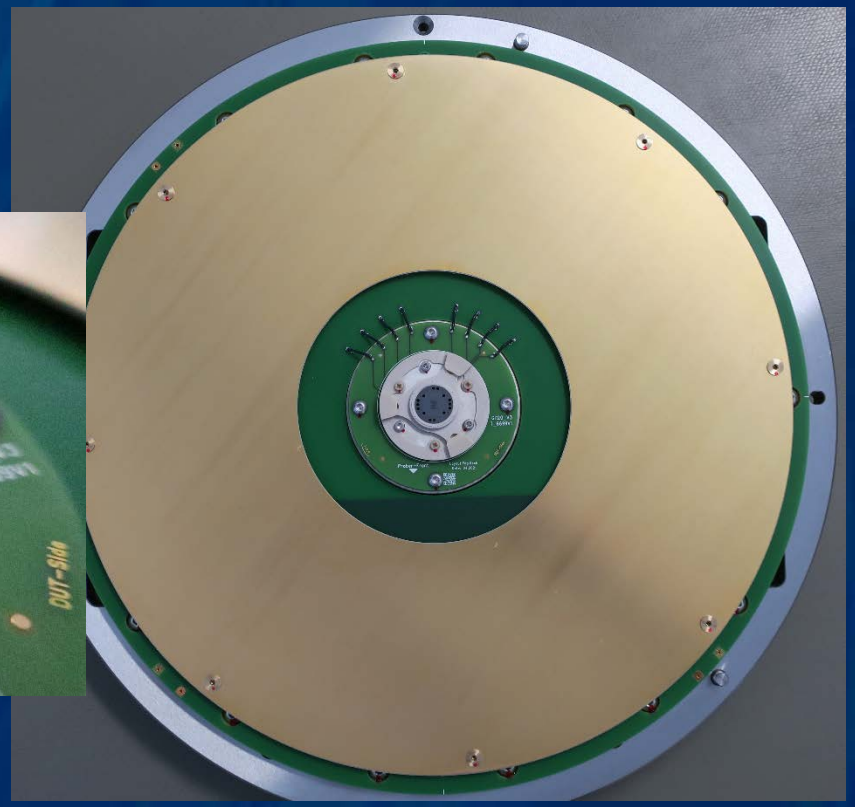
- HV capacitor array, 2.2 kV
- 1x4 arrangement
- chamber pressure: 5 bar
- chamber pressure monitor



4x Vertical LuPo probe card
top side



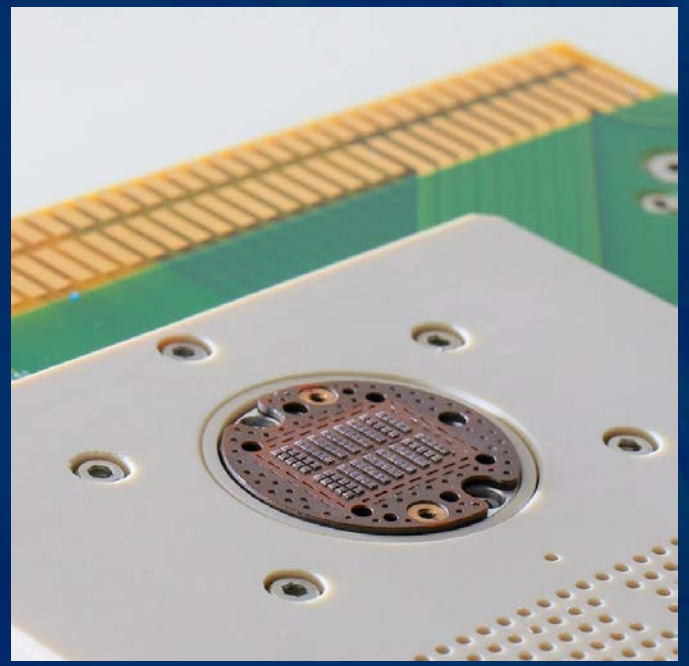
Vertical LuPo probe head
buckling beam technology

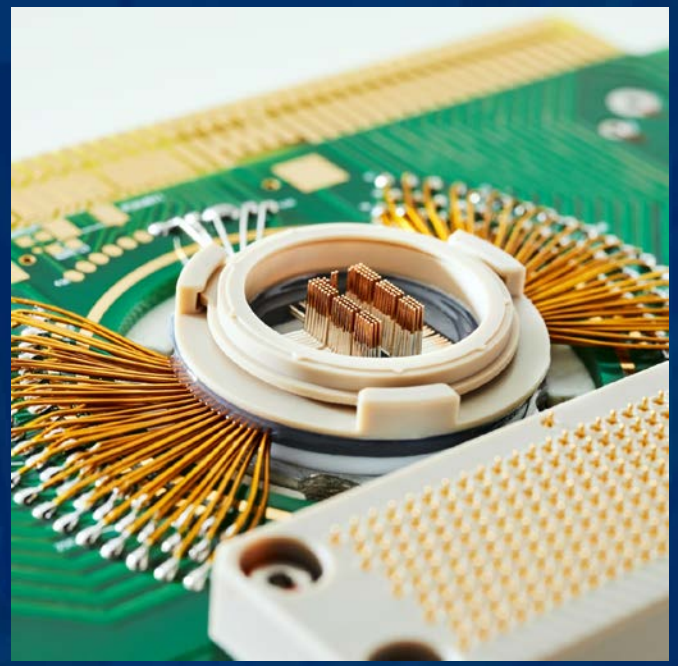


4x Vertical LuPo probe card
top side

Known Good >>POWER<< Die (KGD)

- **Application of wafer test contact technologies to bare chip testing**
  - highest test currents up to 3000A
  - ultra-fast switching: lowest parasitic inductance
  - AC test: both HV and HC present at the same time
  - test on chip handler (instead of wafer prober)





Summary and Outlook

- various technologies (LuPo, SmartClamp...) developed for arc-free and burn-free power device chip testing
- enhanced for SiC, GaN requirements
- successfully introduced into R&D and high volume production test
- from single-site to multi-site probing for mass production
- highest power densities achieved in KGD test

- **An outlook...**
  - **Gen.4 LuPo** using CFM based design and 3D print technology
  - "**RzBeam Vertica**l": new wire superalloy for High Current Vertical probes !!!

...stay tuned!

References:

SWTest conference proceedings :
2002: Probing 10 kV and 100A
2011: Aspects of High Power Probing
2017: Known Good >>POWER<< Die
2022: High Power goes Vertical
2023: High Voltage Probing goes Multi-Site
see www.swtest.org/archive
www.tips.co.at/downloads

www.tips.co.at

Acknowledgements

Diana Damian
Dietmar Einetter
Magdalena Frank
Georg Franz
Sebastian Salbrechter
The TIPS Team
Unnamed customers probing at the "leading edge"

Thanks for your Attention !

Questions please...

Maximizing CCC and the March to an Unburnable Probe

Dr. Hadi Najar
FormFactor

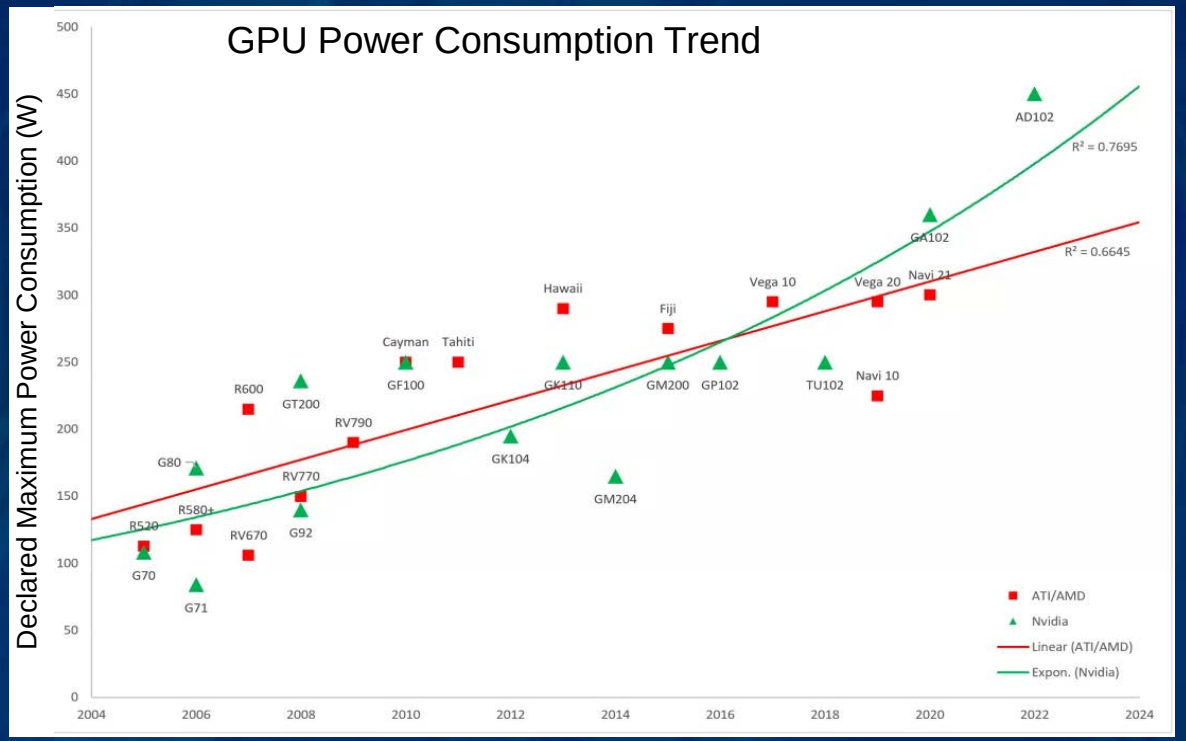
4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

Agenda

- Why Does CCC matter?
- Hybrid Probe Review
- Next Generation Probe Review
- Metallized Guide Plate Review
- Maximized CCC Conclusion

Industry Trends

- **High Performance Compute and GPU applications are marching to 1kW devices (1,000A at 1V)**
  - Shipping 400A devices today (400W at 1V)
  - Newest HPC devices have >50 Billion Transistors
- **New nodes and technology advancements are creating downward pressure on yield**
  - Yield drop with each node transition
  - Transitions to more complex digital coms (PAM4) decrease yield
  - Larger die for HPC and GPU applications are lowering wafer yield
- **As yields decrease and as device power increases Probe Card capability and CCC must increase**



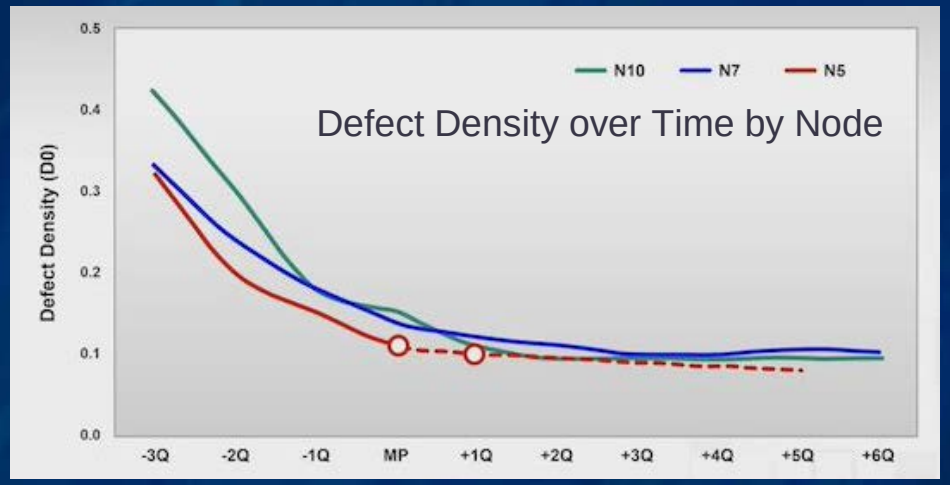
https://www.techspot.com/article/2540-rise-of-power/

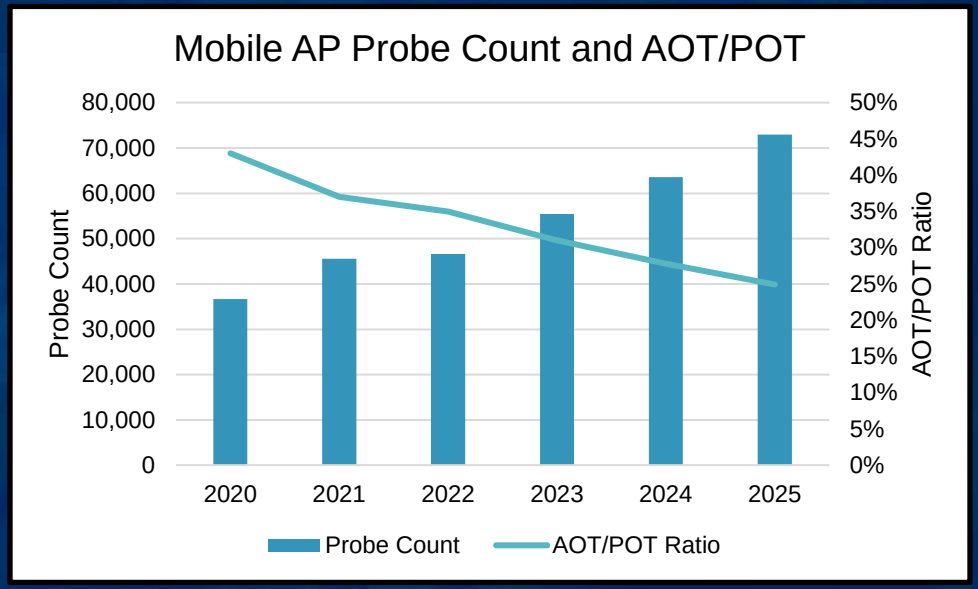
CCC Terminology

- **Current Carrying Capability**
  - The amount of current that a probe or spring can withstand before burning or damage occurs
- **ISMI CCC**
  - Current applied where a 20% lower force is observed in a probe (spring)
- **MAC (Maximum Allowable Current)**
  - Current applied where a change in probe force or planarity is first observed
- **ECCC (Effective Current Carrying Capability)**
  - An averaging of total current that a group of probes can withstand before burning occurs

Why Does CCC Matter?

- **Probe Current Carrying Capability prevents probe burning when something goes wrong during wafer testing**
  - Shorts in the DUT
  - Unstable contact between the DUT and Probe card
- **High CCC Probes improves uptime and MTBF as the probe card becomes more robust and resistant to probe burning**





Methods for Improving CCC

Hybrid Probes

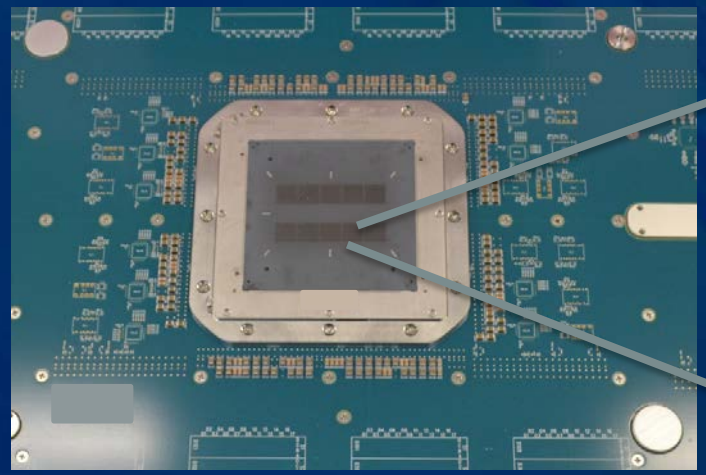
Next Generation Probes

Metallized Guide Plates

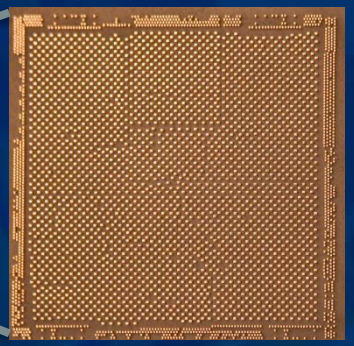
Hybrid Architecture

- **SOCs have PWR/GND in the middle of the Device and I/O in the periphery of the Device**
  - PWR/GND typically at ≥150um pitch
    - Can use wider, high CCC probes
  - I/O typically at ≤90um pitch
    - Can use smaller, lower CCC probes
- **By combining probe types in the Probe Card the Effective CCC is increased**

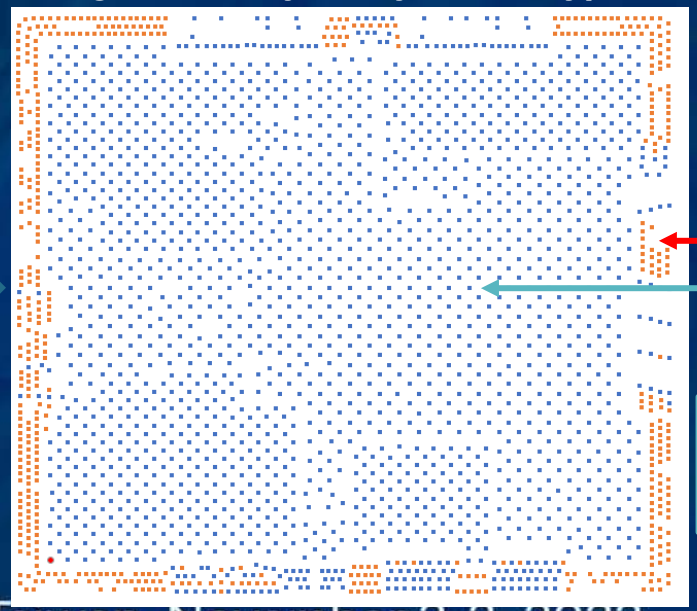
Hybrid Spring Head Probe Card – V93K DD



DUT Zoomed In



Single DUT Layout by Probe Type



Tighter Pitch Probes with lower CCC

Wider Pitch Probes with Higher CCC

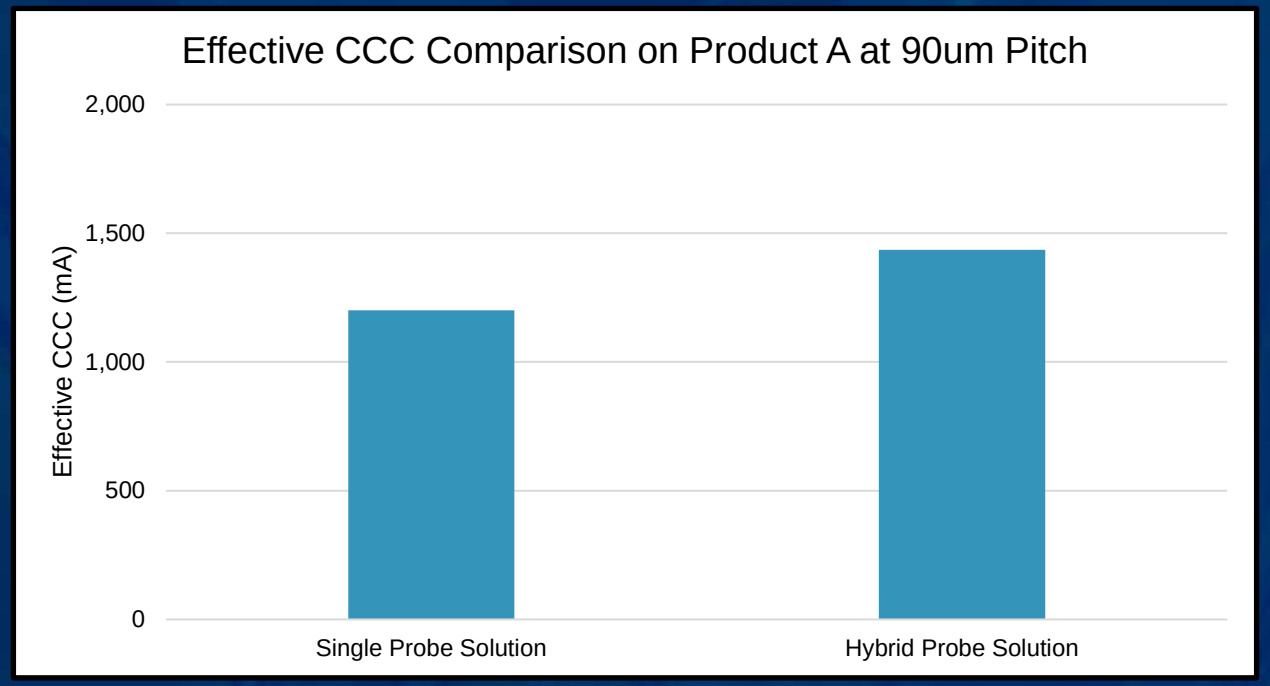
Hybrid Increasing Available CCC

- **FFI Hybrid probe technology increases probe card available CCC**
  - combining tight pitch low CCC probes and wide pitch High CCC probes in the same design
- **Product A as a test case**
  - Min Pitch = 90um
  - Requires MF100F for 90um pitch with CCC of 1,200 mA
  - If hybrid is used available CCC can be improved by 20% to 1,435 mA when using MF130/MF100

Product A x8 Hybrid Available CCC Example		
Hybrid Probe Type	**MF100F**	**MF130F**
CCC (mA)	1,200	1,500
Probe Count	4,216	15,248
Total CCC (mA)	5,059,200	22,872,000
Total Probe Card Available CCC (mA)	**1,435**	
% Improvement over Single Probe (MF100)	**20%**	

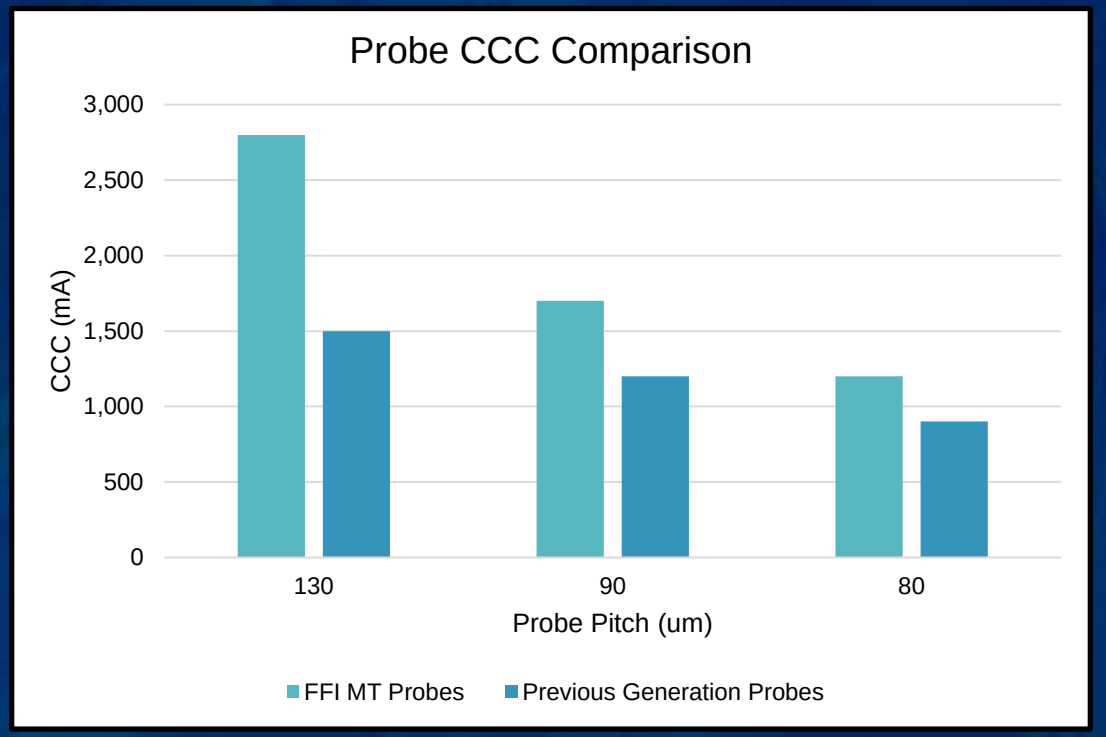
Maximizing Effective CCC

- **Hybrid probes provide 20% higher effective CCC relative to single probe solutions**



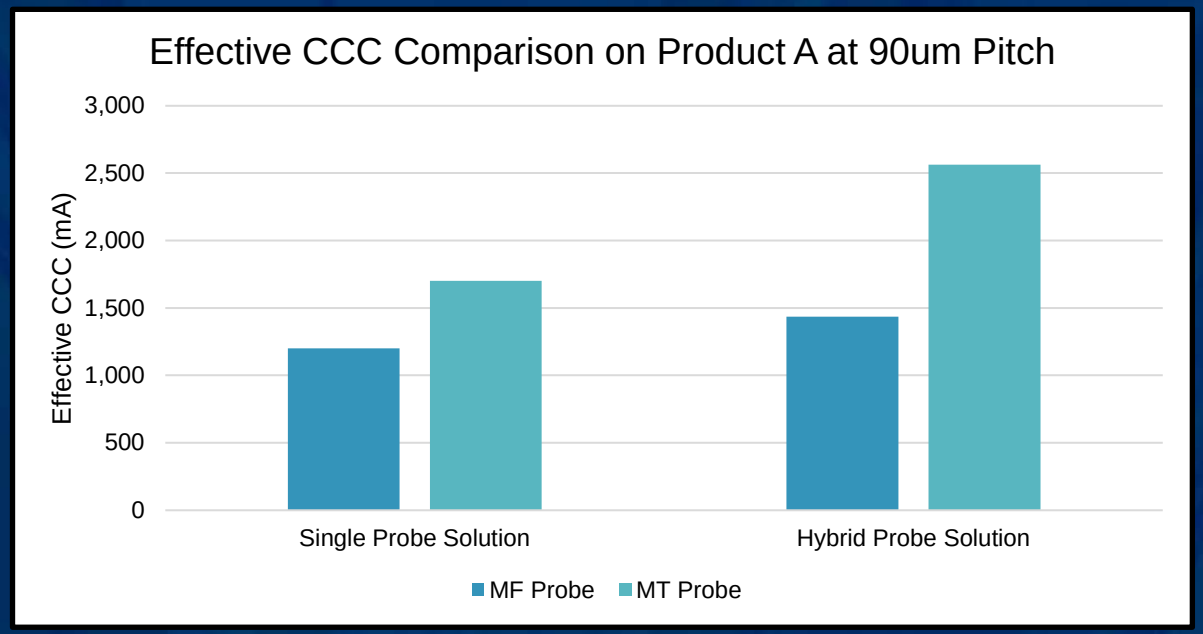
FormFactor MT Probe

- MT next generation probes provide >50% improved CCC over current gen. MEMS probes
- Higher speed performance with shorter probe length.
- Hybrid compatible MT probe family to further enhance CCC and high-speed capability.
- Metallized Guide Plate can further increase effective CCC to >3A

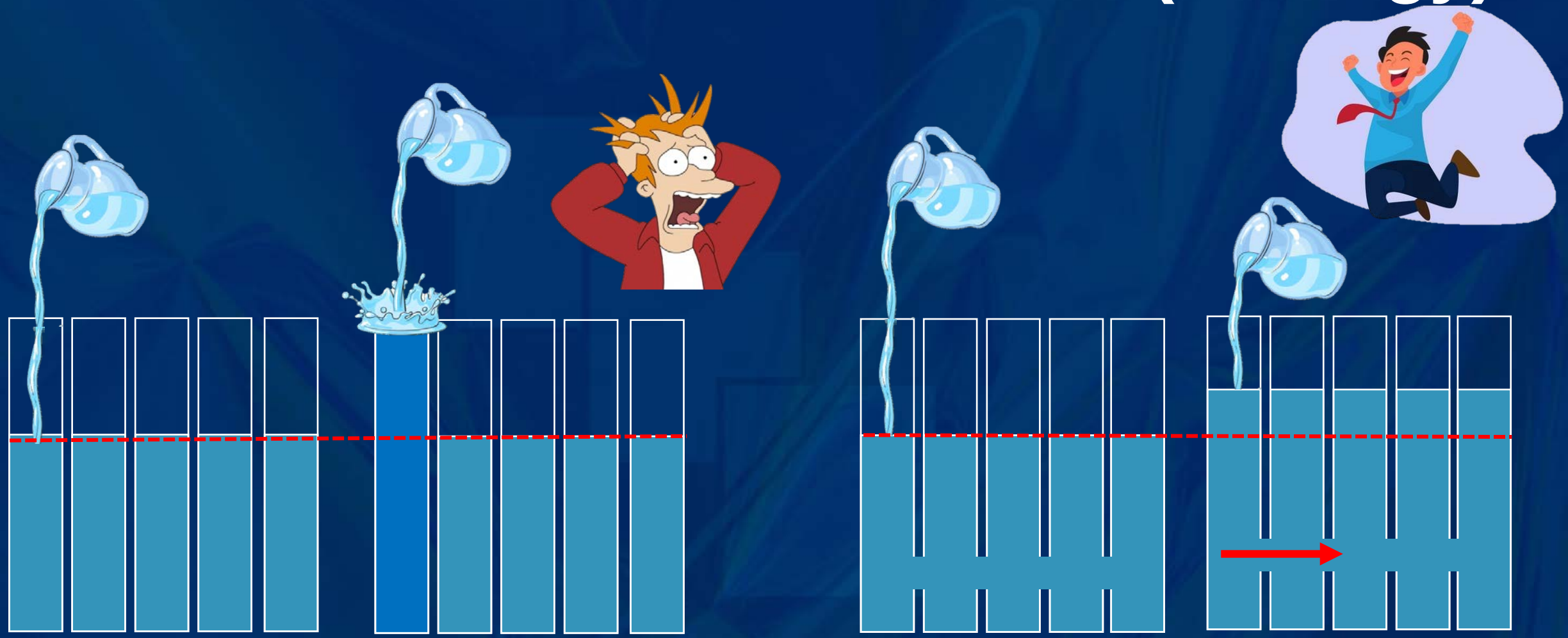


Maximizing Effective CCC

- **Hybrid probes provide 20% higher effective CCC relative to single probe solutions**
- **MT Probes provide 42% higher CCC relative to last generation probes**
  - 78% improvement when combined with Hybrid



What is Metallized Guide Plate? (Analogy)



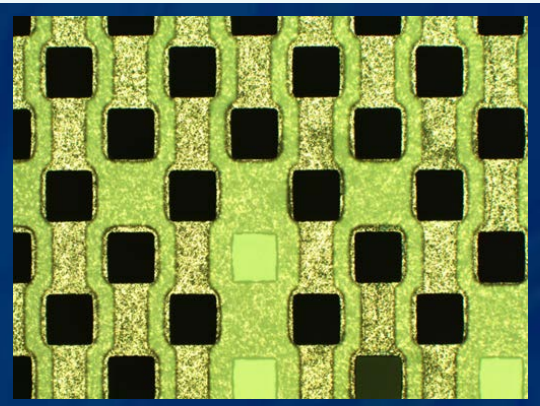
OVERFLOW!!
(No MeGP)

Distributed
(MeGP)

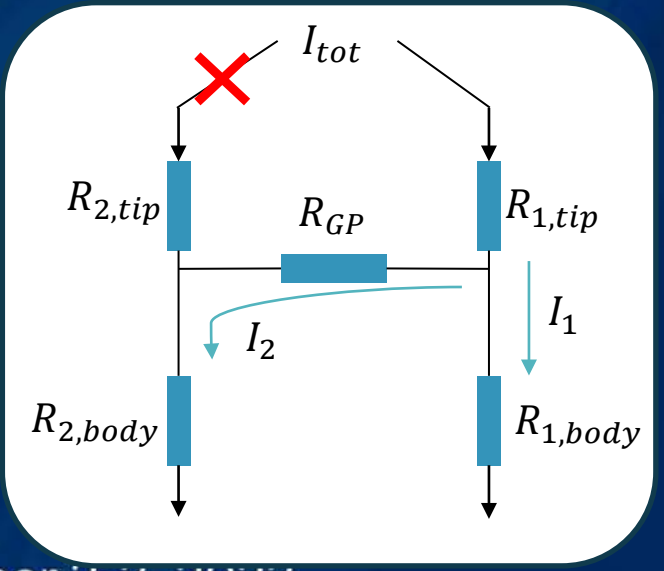
What is Metallized Guide Plate?

- **Metallized Guide Plates (MeGP) connect VDD and GND nets together through metal patterns on the Guide Plate**
  - Provides alternative current path when overcurrent events occur
  - Enables Improved Contact with the DUT through alternative current paths

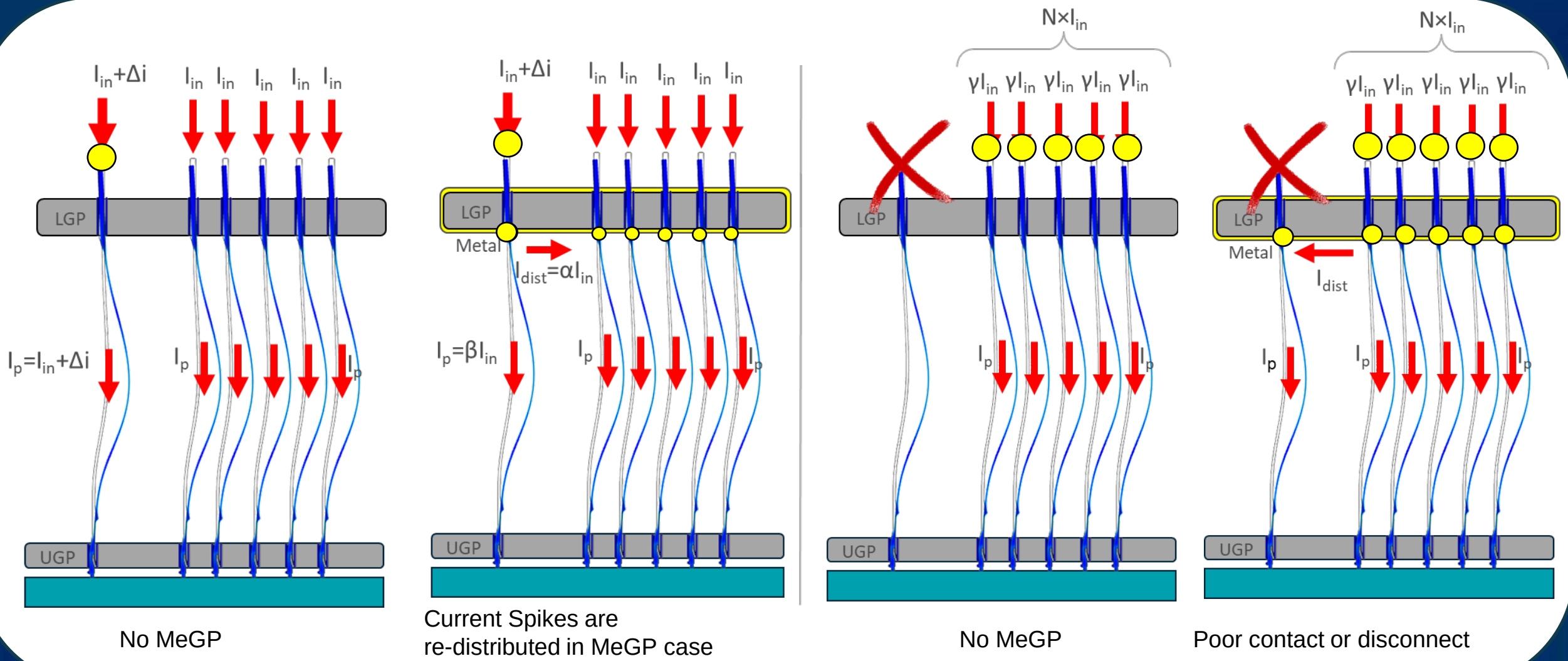
Metallization High Magnification



Metallization 2-Probe Circuit



Examples of how MeGP can help



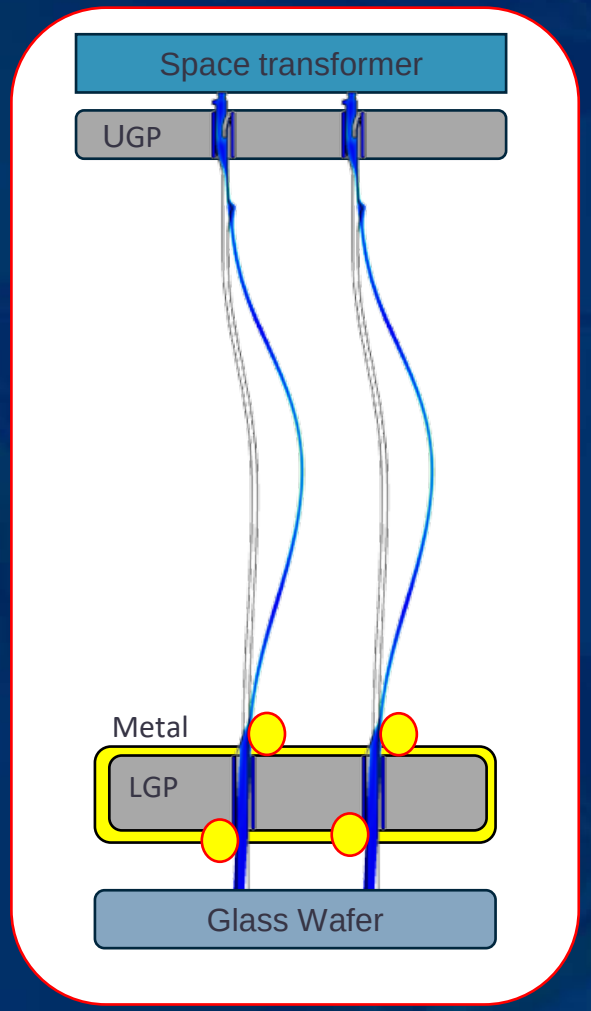
No MeGP

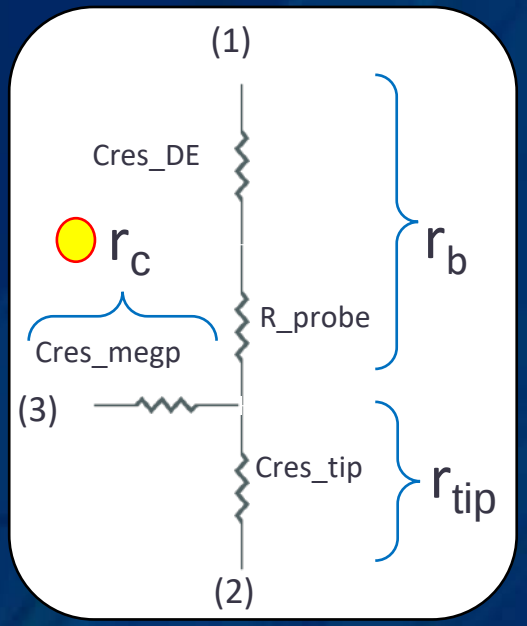
Current Spikes are re-distributed in MeGP case

No MeGP

Poor contact or disconnect

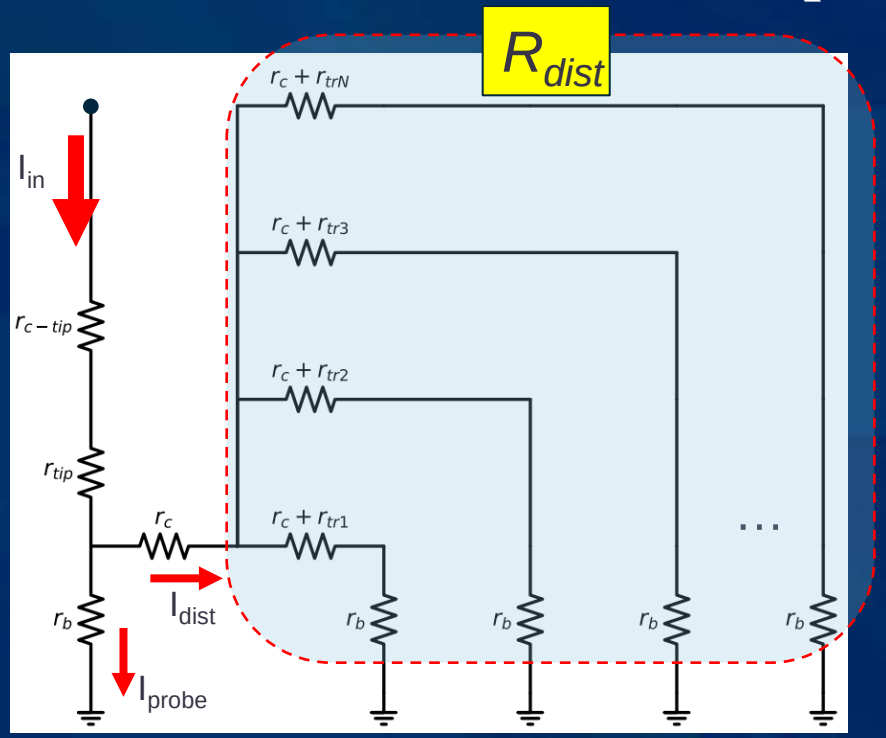
MeGP Technical Terminology





- r_b: Probe body + DE Cres
- r_c : Tip-MeGP Contact resistance
- r_{tr}: Trace resistance

Generalized MeGP Effective CCC model (building block)

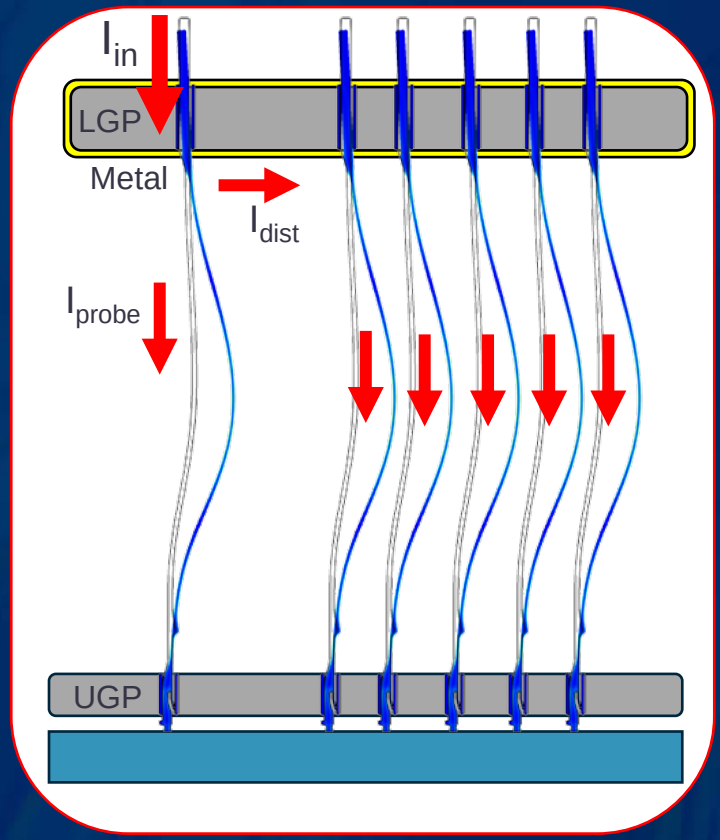


Effective CCC

$$ECCC = I_{probe}\left(\underbrace{1 + \frac{r_b}{r_c + R_{dist}}}_{\text{amplification factor}}\right)$$

$$R_{dist} = \left(\sum_{n=1}^{N} \frac{1}{r_c + r_{tr(n)} + r_b}\right)^{-1}$$

r_b: Probe body + DE Cres
r_c : Tip-MeGP Contact resistance
r_{tr}: Trace resistance
N: Number of probes
R_{dist}: resistance of distributed network



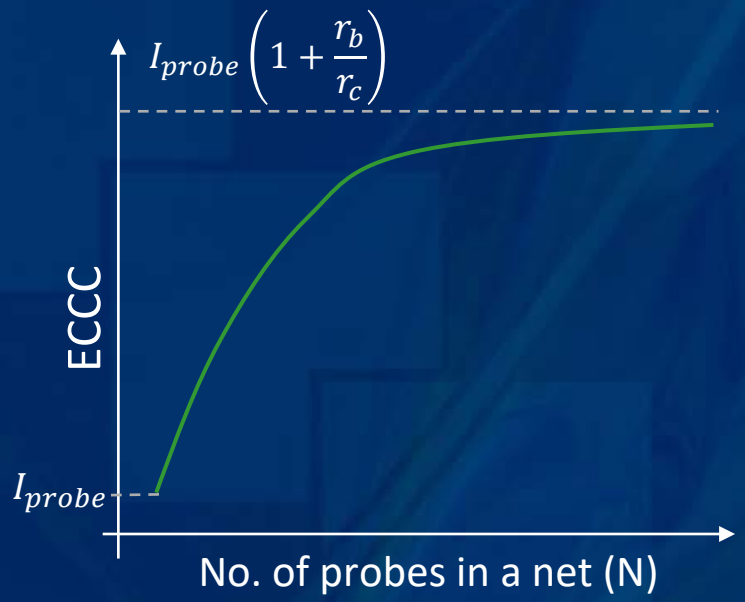
Effect of trace resistance and number of probes

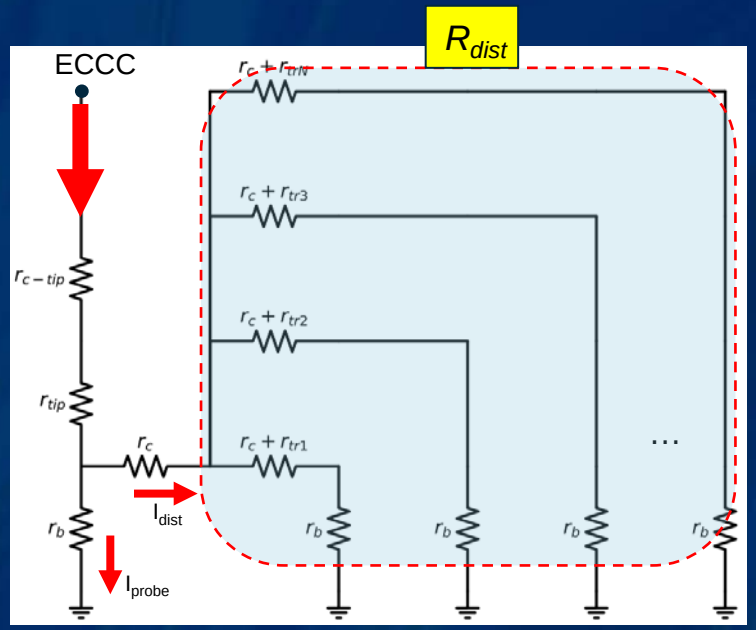
(1) If r_{tr} << $r_c + r_b$, the CCC will be layout independent, and the general equation reduces to:

$$ECCC_1 = I_{probe}\left(1 + \frac{r_b}{r_c + \frac{r_c + r_b}{N}}\right)$$

(2) For large gang numbers, N, the equation reduces to:

$$ECCC_2 = I_{probe}\left(1 + \frac{r_b}{r_c}\right)$$

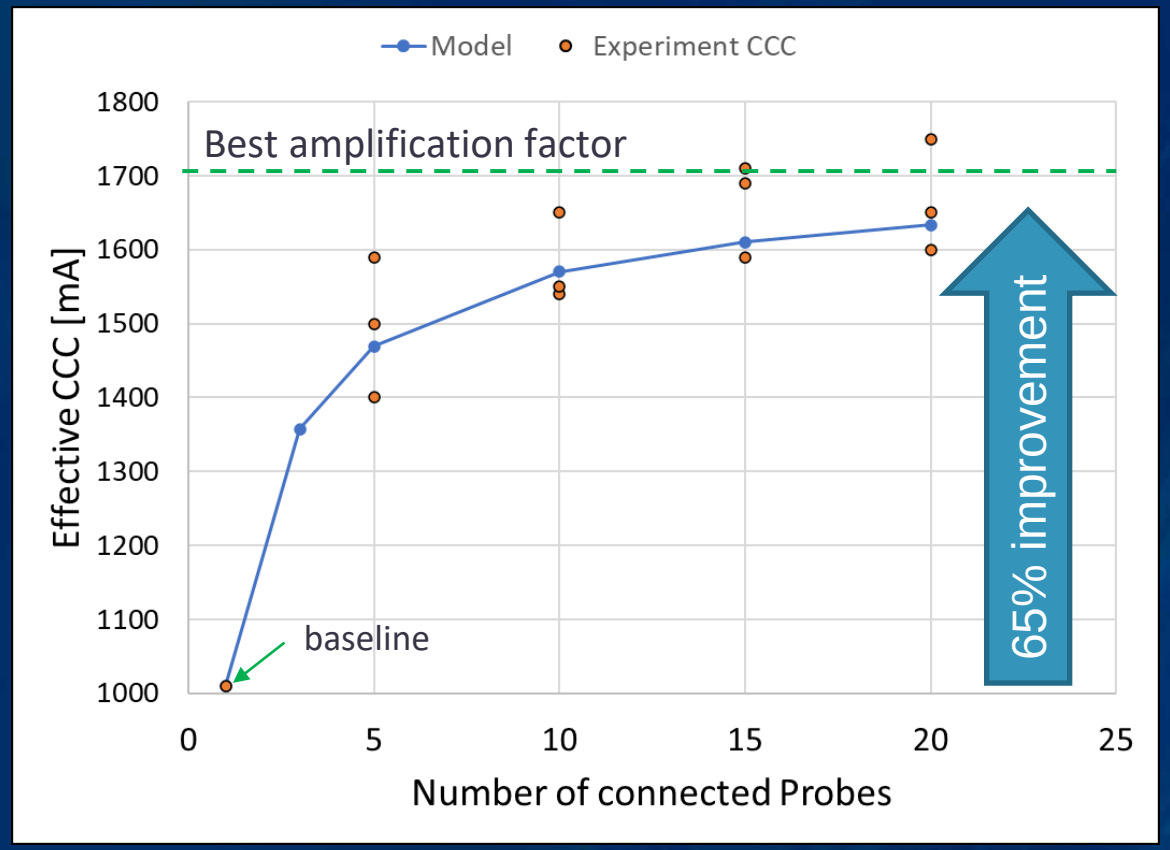




$1 + \frac{r_b}{r_c}$ is the best CCC amplification factor one can get.

r_b: Probe body + DE Cres
r_c : Tip-MeGP Contact resistance
r_{tr}: Trace resistance
N: Number of probes

Validation using measured CCC and True MeGP CRES data

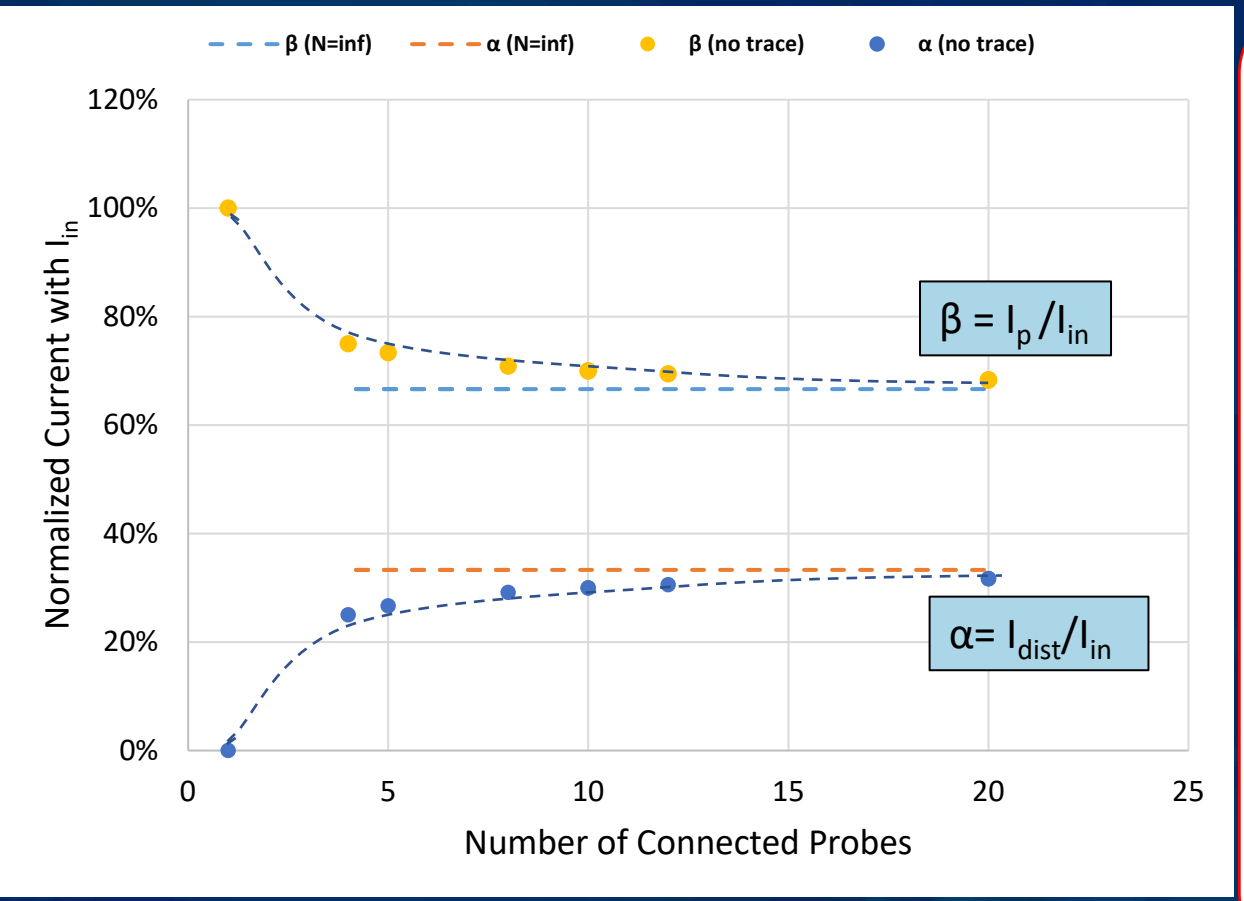


Effective CCC

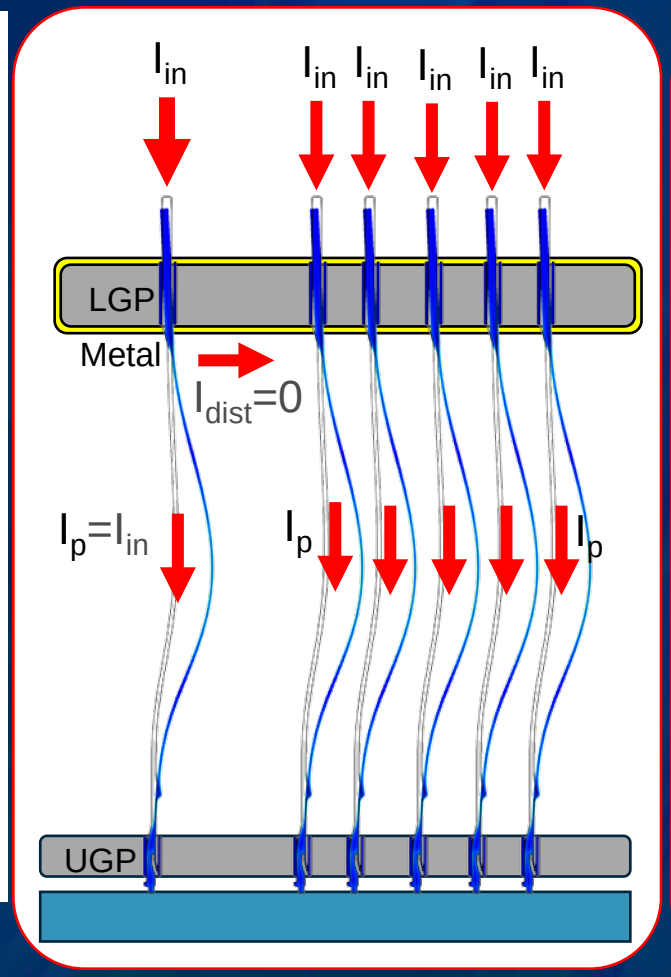
$$ECCC = I_{probe}\left(1 + \underbrace{\frac{r_b}{r_c + R_{dist}}}_{\text{amplification factor}}\right)$$

- Excellent agreement between model and experiment was achieved.
- ECCC showed a 65% average improvement for 20 connected probes.

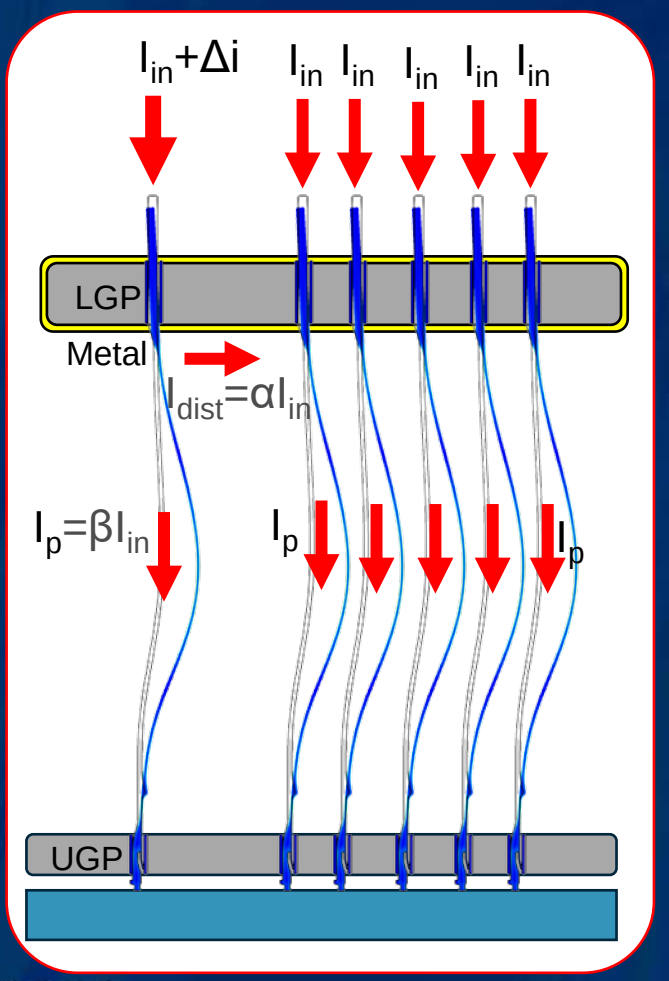
Model Extension to real cases – Current Spike events



Ideal case with no current variation

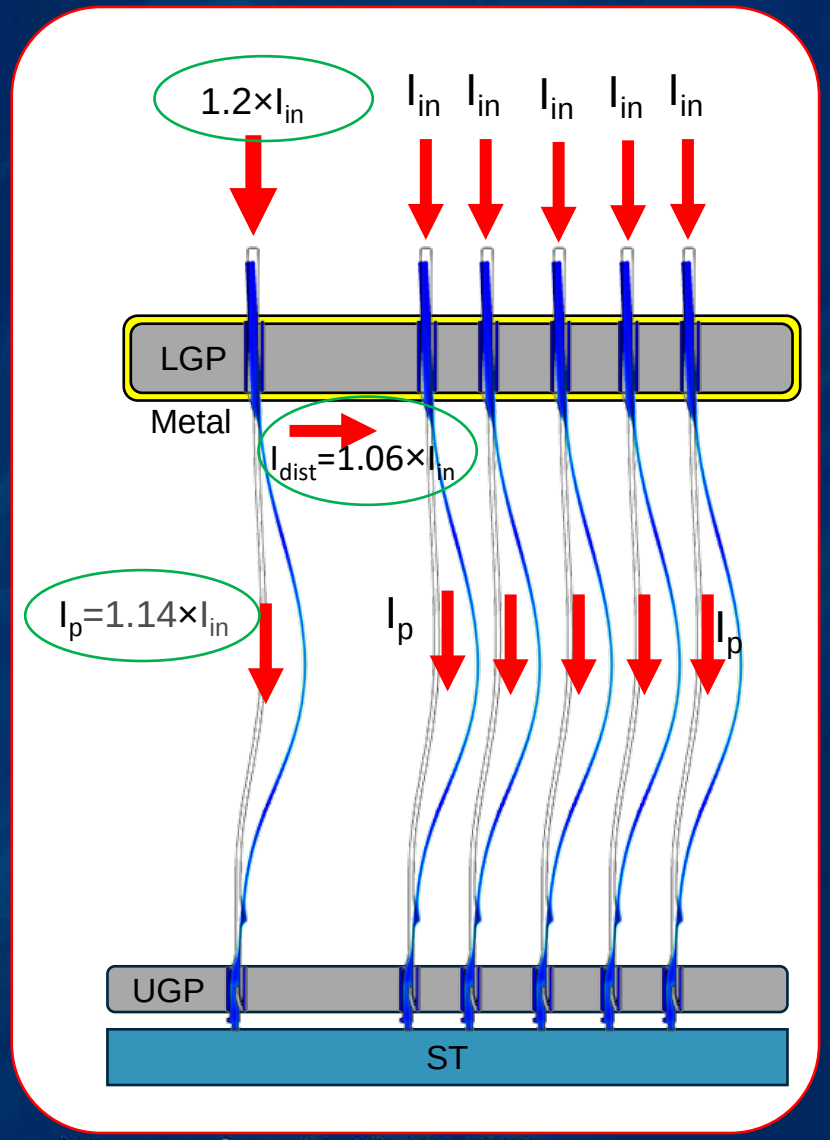


Current spike event



Numerical Example

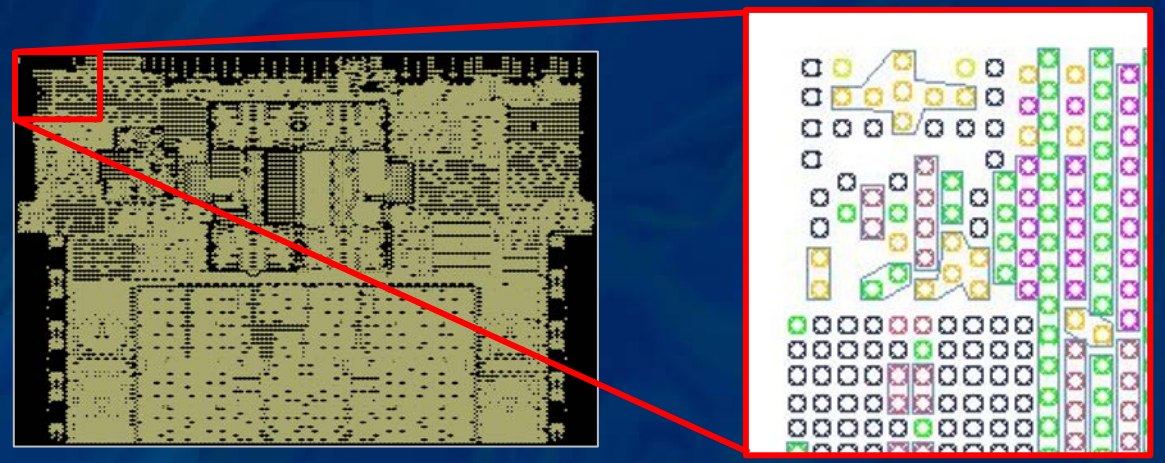
- For a 20-ganged probes with negligeable trace resistance, α = 32% and β = 68%.
- A 20% increase in nominal current (I_{in}), translates to 6.4% increase in I_{dist} and 13.6% in I_{probe}.



MeGP Design Challenges

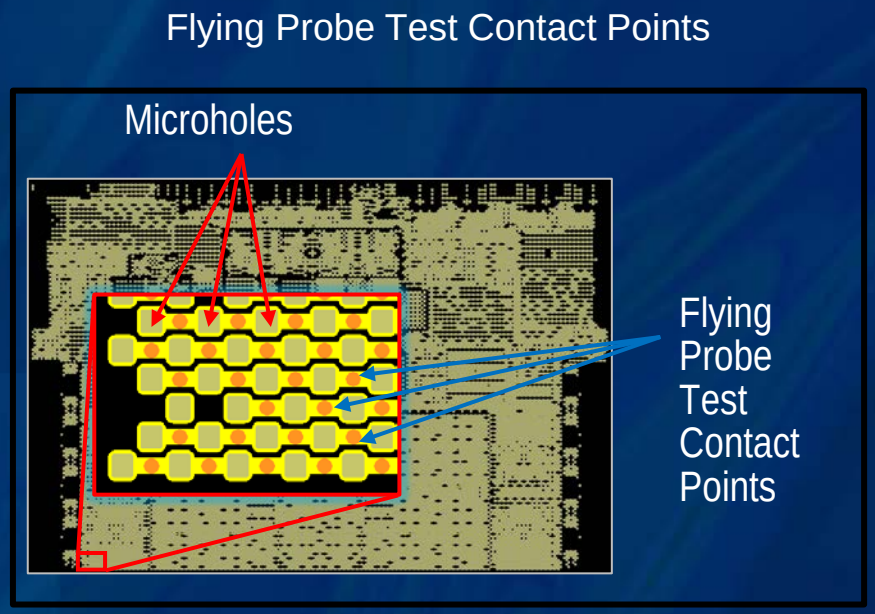
- **Challenge: Design of the MeGP is difficult due to the number of nets and probes involved.**
  - A design error could be fatal in the yield of the MeGP leading to shorts from VDD to GND
  - Design complexity could significantly
- **Solution: Automated Design and DFM rule implementation**
  - Eliminates mistakes from manual design
  - Decreases design cycle time to a few hours

Design Automation Improves Design Cycle Time and Reduces Errors



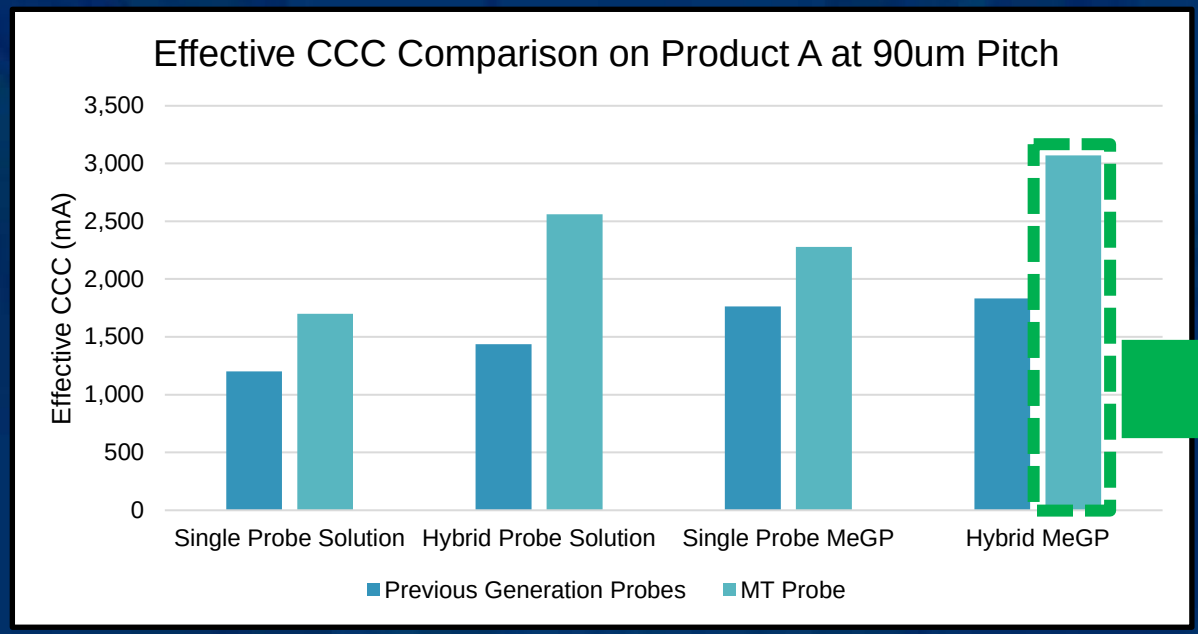
MeGP Verification Challenges

- **Challenge: MeGP needs to be verified for shorts before stitching the probes and completing assembly of the Probe Card**
  - POR process flow verifies electrical continuity with PRVX
    - If short is found the Probe Head would need to be disassembled and fixed
      - Long Cycle times at the last step of the manufacturing process
- **Solution: Implementation of Flying Probe Test after MeGP Plating**
  - Allows rework of GPs if needed
  - Ensures high quality through manufacturing process



Maximizing Effective CCC

- **MeGP Improves Effective CCC by 65% depending on the probe architecture**
- **FFI has achieved the first >3A CCC Probe card at 90um pitch using Next generation MT Probes, Hybrid probes, and Metallized Guide Plate**
  - Short Cycle Time and Excellent quality guaranteed through Design Automation and Outgoing Flying Probe Test



MT Hybrid with MeGP provides Best Effective CCC >3A

Thank You!!

SEAMLESS ATE TEST PROGRAM GENERATION USING A ML APPROACH - MULTI-LABEL CLASSIFICATION

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Kalyana Sundaram
Senthilkumar
Dinesh
Lavanya

Caliber Interconnects Pvt Ltd

4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

Agenda

- Post Silicon Validation: Test program development overview
- Challenges in market
- Proposed Test Program Generation
- ML Approach - Multi label classification
- Results and Conclusion

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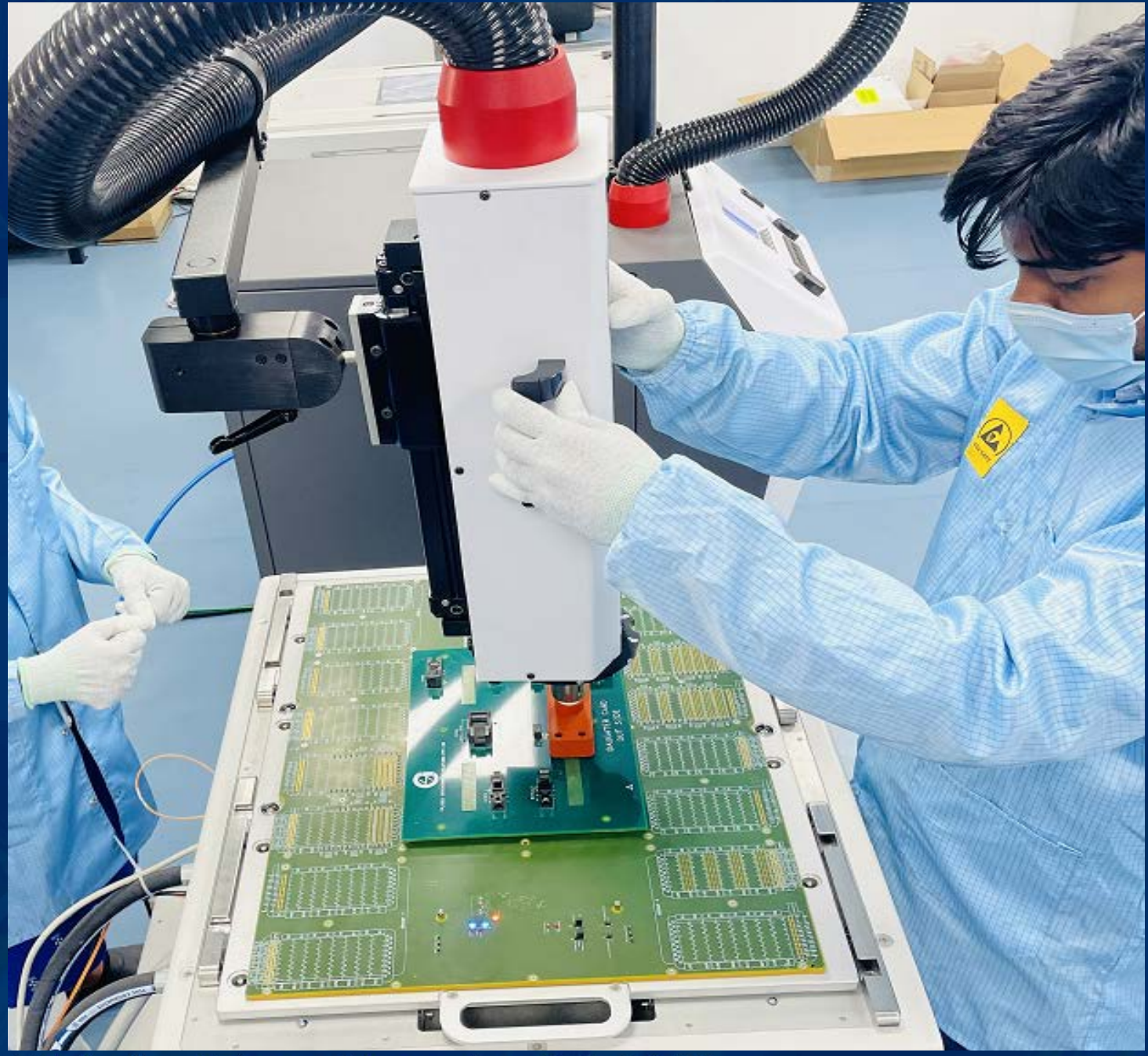
Post Silicon Validation Overview



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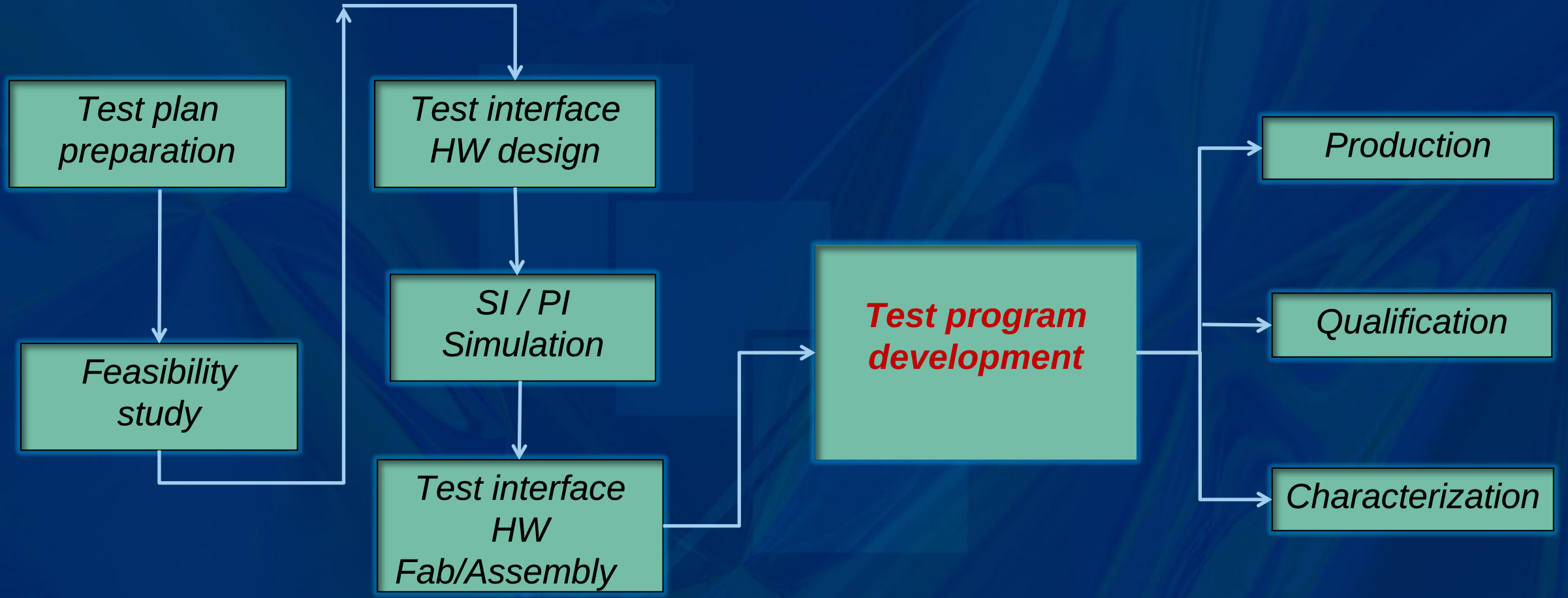
Post Silicon Validation Process



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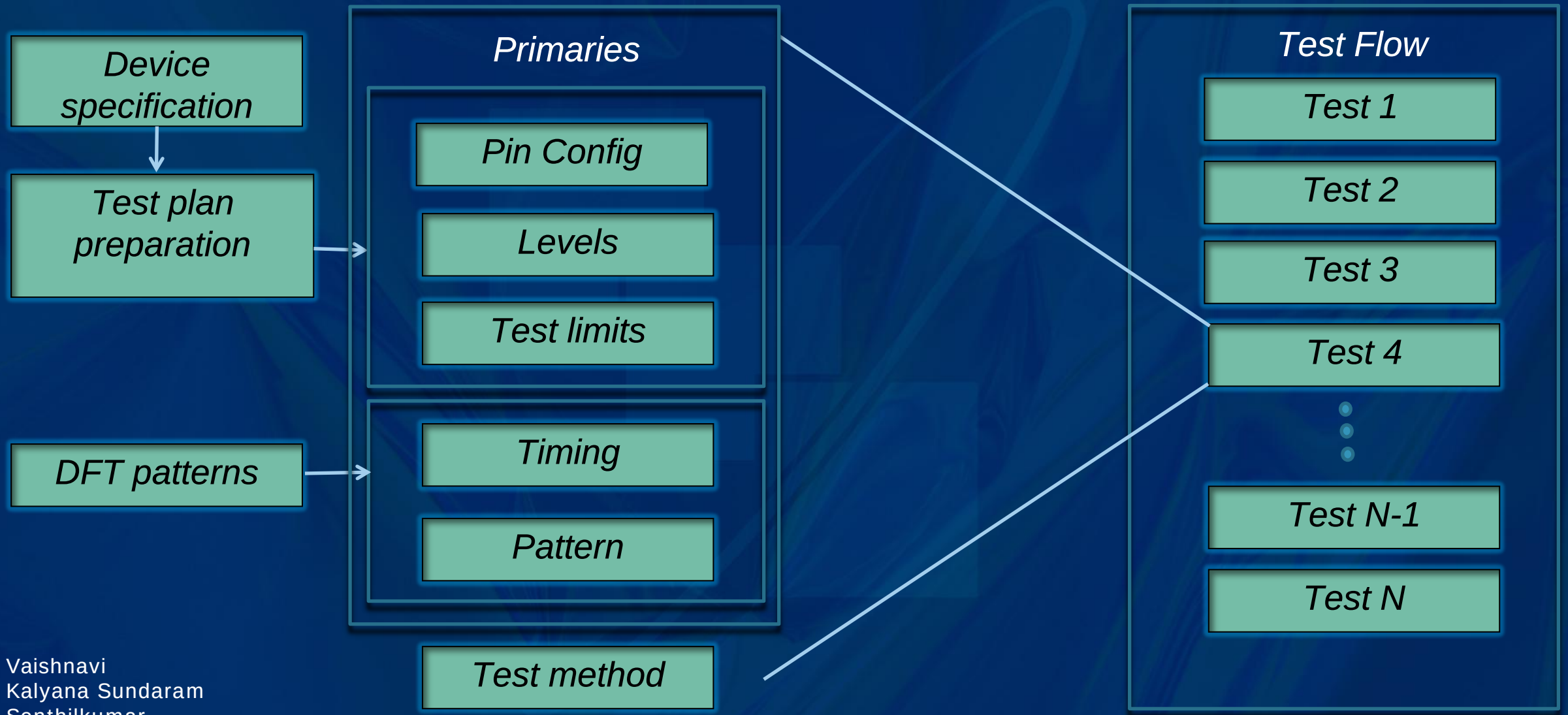
Conventional Test Program Generation



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Challenges in Market

Meeting the demands of intricate IC designs and faster time-to-market necessitates swift, and accurate test plan preparation followed by a production worthy test program development with a huge intervention of test engineer.

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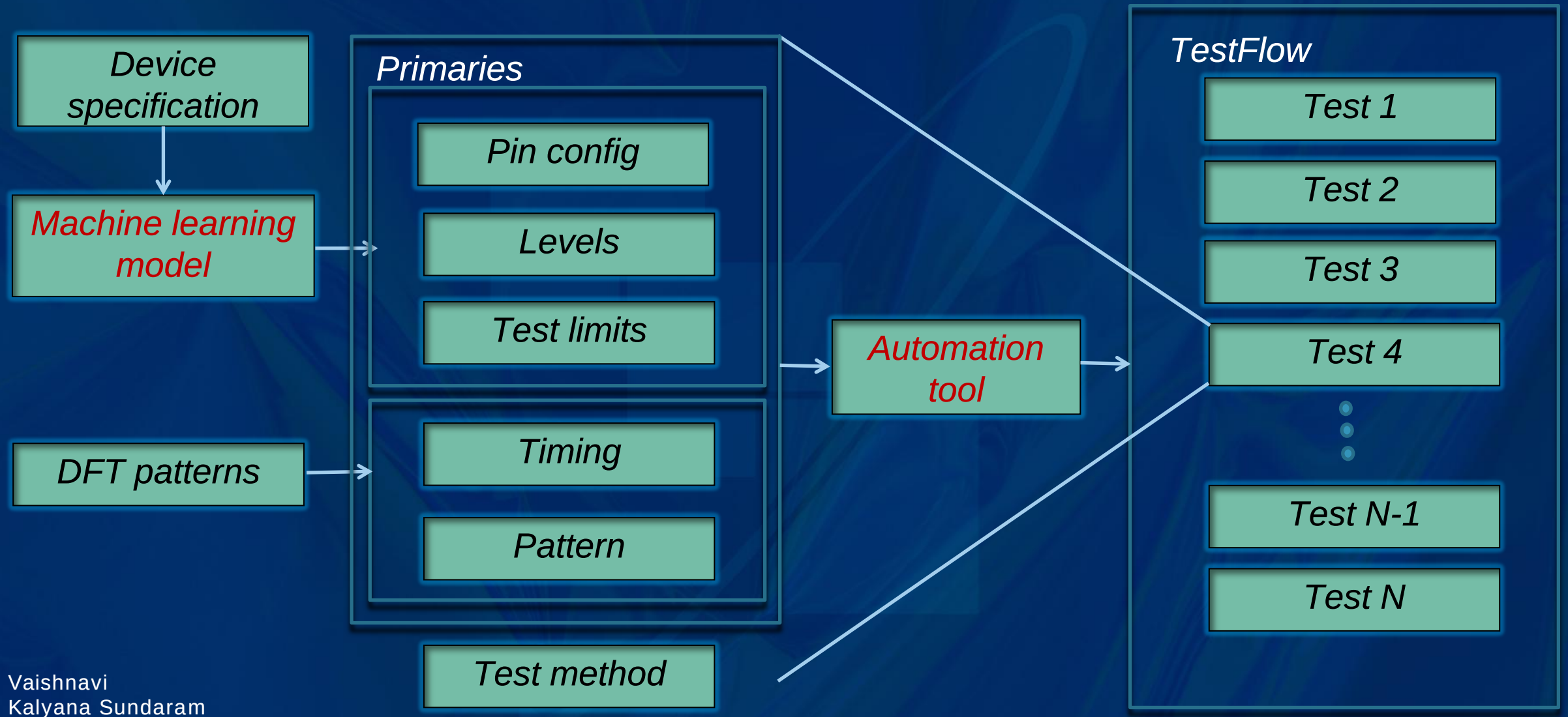
Proposed Solution



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TestGeni- Test Automation IP

- **Automation tool Introduced by Caliber**
- **To generate readily loadable Test files**
  - Pin Config
  - Levels
  - TestFlow
  - Test Limits

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Illustration-Device 1

10. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V_{CC}		2.0 to 5.5	V
Input voltage	V_{IN}		0 to 5.5	V
Output voltage	V_{OUT}		0 to V_{CC}	V
Operating temperature	T_{opr}		-40 to 125	°C
Input rise and fall times	dt/dv	V_{CC} = 3.3 ± 0.3 V	0 to 100	ns/V
		V_{CC} = 5.0 ± 0.5 V	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

11.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	V
				3.0 to 5.5	V_{CC} × 0.7	—	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	V
				3.0 to 5.5	—	—	V_{CC} × 0.3	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			I_{OH} = -4 mA	3.0	2.58	—	—	
			I_{OH} = -8 mA	4.5	3.94	—	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			I_{OL} = 4 mA	3.0	—	—	0.36	
			I_{OL} = 8 mA	4.5	—	—	0.36	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	μA

Test 1

Sample Parameter - Test Setup
Test parameter: VOH
Test method: spec search
VCC=2V
VIL=0.50V
VIH=1.50V
IOL=50uA
IOH=-50uA
VOL=0.1V
Maxlimit= 2V
Minlimit=1.9V
startValue:1.5V
StopValue=2.5V
Step size= 0.01V
Temp=25degC

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Illustration-Device 1

10. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V_{CC}		2.0 to 5.5	V
Input voltage	V_{IN}		0 to 5.5	V
Output voltage	V_{OUT}		0 to V_{CC}	V
Operating temperature	T_{opr}		-40 to 125	°C
Input rise and fall times	dt/dv	V_{CC} = 3.3 ± 0.3 V	0 to 100	ns/V
		V_{CC} = 5.0 ± 0.5 V	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

11.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	V
				3.0 to 5.5	V_{CC} × 0.7	—	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	V
				3.0 to 5.5	—	—	V_{CC} × 0.3	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			I_{OH} = -4 mA	3.0	2.58	—	—	
			I_{OH} = -8 mA	4.5	3.94	—	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			I_{OL} = 4 mA	3.0	—	—	0.36	
			I_{OL} = 8 mA	4.5	—	—	0.36	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	μA

Test 1:
Test parameter: VOH
Test method: spec search
VCC=2V
VIL=0.50V
VIH=1.50V
IOL=50uA
IOH=-50uA
VOL=0.1V
Maxlimit= 2V
Minlimit=1.9V
startValue:1.5V
StopValue=2.5V
Step size= 0.01V
Temp=25degC

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Illustration-Device 1

10. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V_{CC}		2.0 to 5.5	V
Input voltage	V_{IN}		0 to 5.5	V
Output voltage	V_{OUT}		0 to V_{CC}	V
Operating temperature	T_{opr}		-40 to 125	°C
Input rise and fall times	dt/dv	V_{CC} = 3.3 ± 0.3 V	0 to 100	ns/V
		V_{CC} = 5.0 ± 0.5 V	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

11.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	V
				3.0 to 5.5	V_{CC} × 0.7	—	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	V
				3.0 to 5.5	—	—	V_{CC} × 0.3	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			I_{OH} = -4 mA	3.0	2.58	—	—	
			I_{OH} = -8 mA	4.5	3.94	—	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			I_{OL} = 4 mA	3.0	—	—	0.36	
			I_{OL} = 8 mA	4.5	—	—	0.36	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	μA

Sample Parameter - Test Setup

Test 1:

Test parameter: VOH

Test method: spec search

VCC=2V

VIL=0.50V

VIH=1.50V

IOL=50uA

IOH=-50uA

VOL=0.1V

Maxlimit= 2V

Minlimit=1.9V

startValue:1.5V

StopValue=2.5V

Step size= 0.01V

Temp=25degC

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Illustration - Device 2

10. Operating Ranges (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		4.5 to 5.5	V
Input voltage	V_{IN}		0 to 5.5	V
Output voltage	V_{OUT}	(Note 1)	0 to 5.5	V
		(Note 2)	0 to V_{CC}	
Operating temperature	T_{opr}		-40 to 125	°C
Input rise and fall times	dt/dv		0 to 20	ns/V

11.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage	V_{IH}	—		4.5 to 5.5	2.0	—	—	V
Low-level input voltage	V_{IL}	—		4.5 to 5.5	—	—	0.8	V
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	4.5	4.4	4.5	—	V
			I_{OH} = -8 mA	4.5	3.94	—	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	4.5	—	0.0	0.1	V
			I_{OL} = 8 mA	4.5	—	—	0.36	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	μA
	I_{CCT}	Per input: V_{IN} = 3.4 V Other input: V_{CC} or GND		5.5	—	—	1.35	mA
Output leakage current (Power-OFF)	I_{OPD}	V_{OUT} = 5.5 V		0	—	—	0.5	μA

Test 1:
Test parameter: VOH
Test method: Spec search
VCC = 4.5V
VIL = 0.50V
VIH = 1.50V
IOL = 50uA
IOH = -50uA
VOL = 0.1V
Max limit = 4.4V
Min limit = 4.5V
Start value = 4V
Stop value = 5V
Step size = 0.01V
Temp = 25degC

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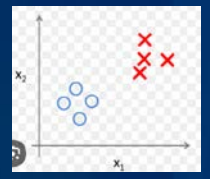
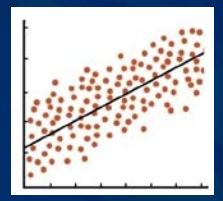
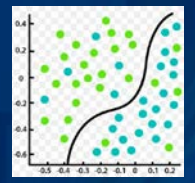
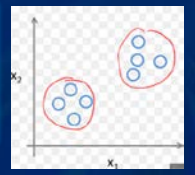
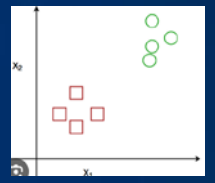
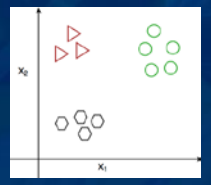
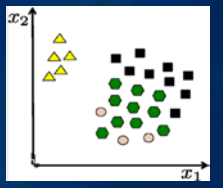
Machine Learning and Proposed Approach

- Machine learning algorithms
  - Supervised learning (labeled data)
    - Regression
    - Classification
      - Binary Classification
      - Multi class Classification
      - Multi label Classification
        - LP,PS,DBPNN,PSt,BCC, CDN,BPNN, RakEL,BRq, etc..
  - Semi supervised learning
  - Unsupervised learning (Unlabeled data)
    - Clustering
    - Dimensionality reduction

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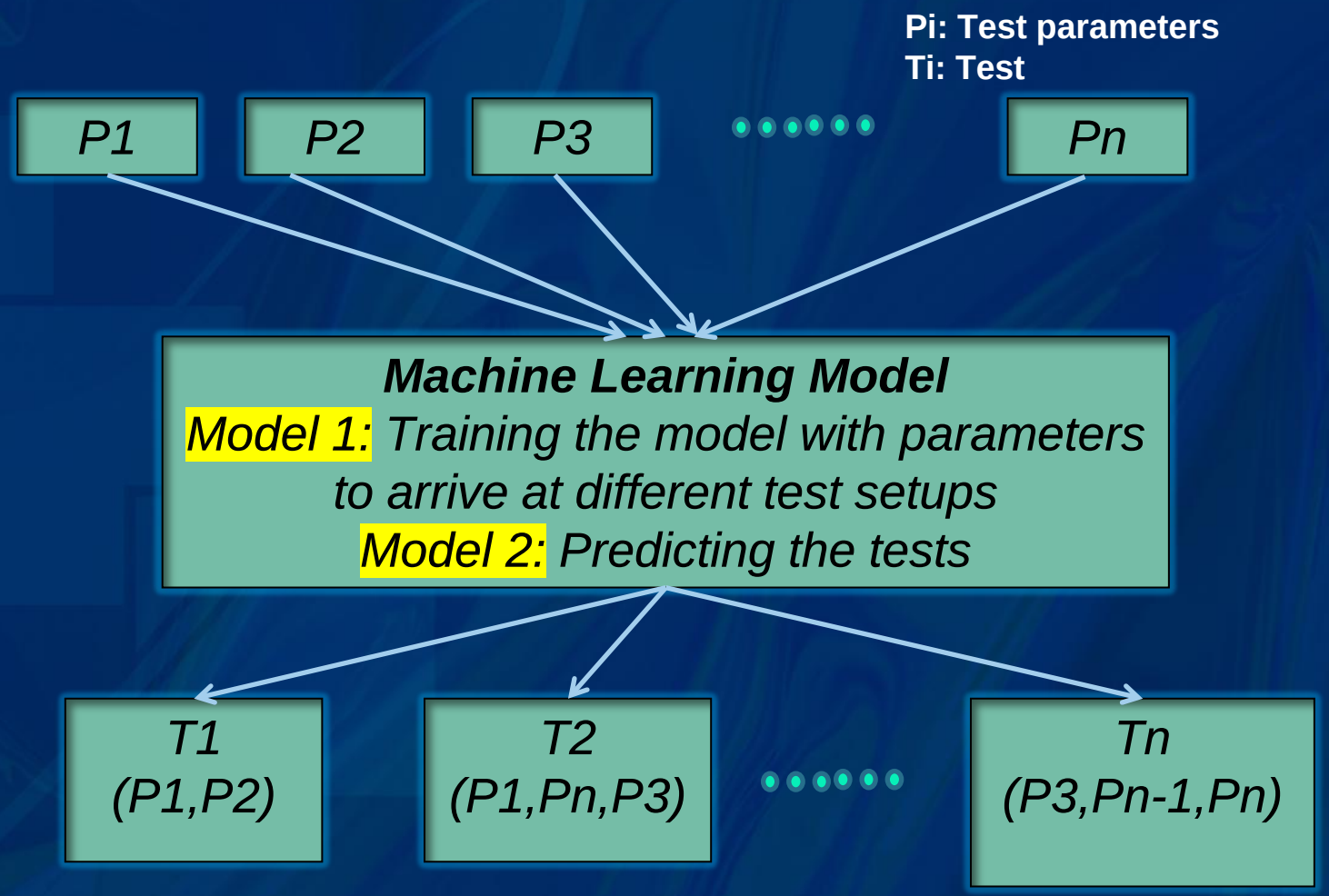
Multi-label Classification Model

Supervised learning method - Multilabel classification:

- Classify data with more than one target variable
- Designed to handle complex tasks where items can belong to multiple categories simultaneously

Ensemble method can give better accuracy



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Machine Learning Model 1

Phase 1:

Feature Engineering:

- Extracting unique features from device specifications
- Creating dictionary with parameters and its levels as “key - value” pair
  - Features extracted - 715
- Reducing overfitting through Principal Component Analysis(PCA) technique
  - Features scaled down - 355
- Zero imputation to make the sparse data as clean data

Phase 2:

- Classify objects using PS: Pruned sets algorithm(Ensemble method)
  - Base classifier:J48
  - Pruning value(pv): It defines an infrequent labelset as one which occurs less than ‘p’ times in the data.{pv ∈ Z | 1 ≤ pv ≤ 5}.
  - Subsampling value (sv)[-N] :Subsample value defines the (maximum) number of frequent labelsets to subsample from the infrequent labelsets.

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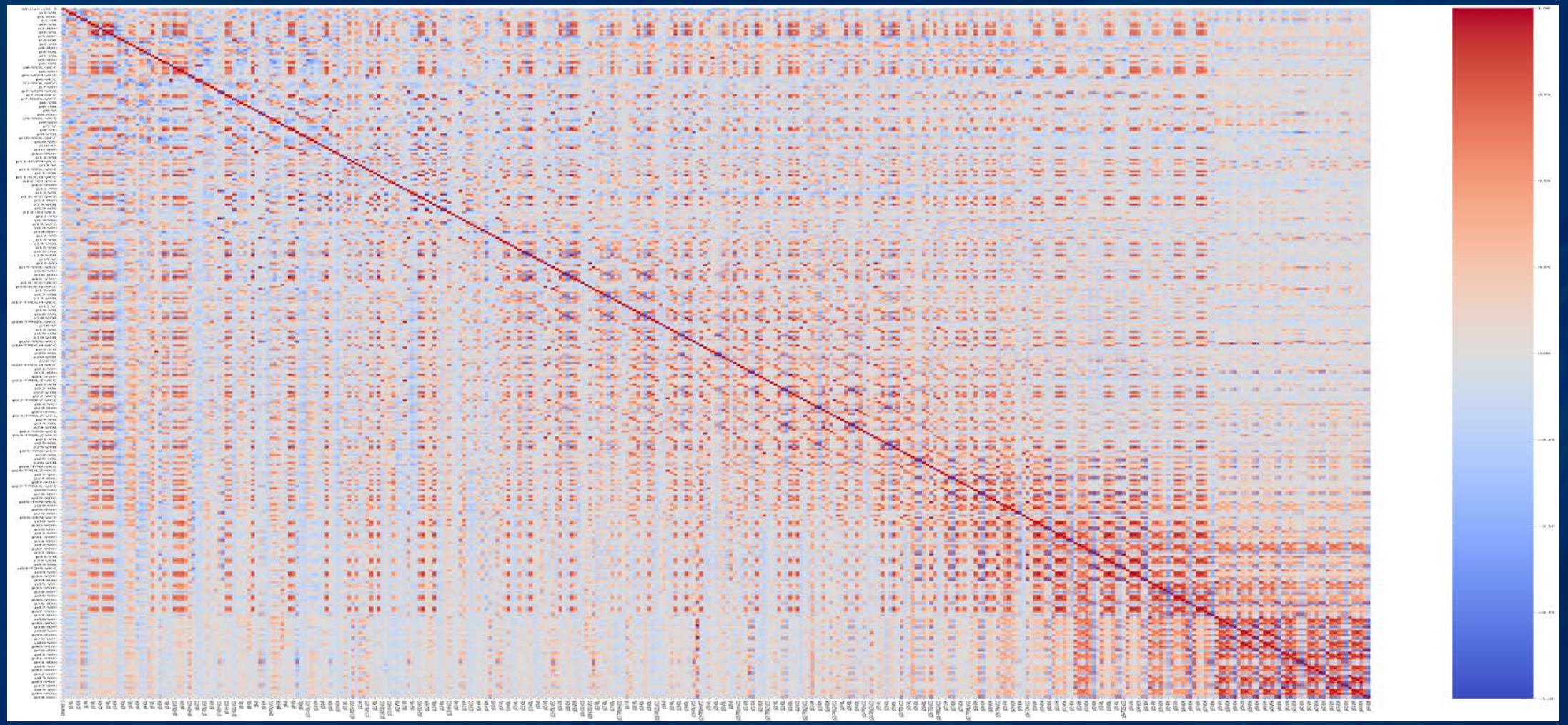
Correlation Analysis of Features



Highly correlated

Least correlated

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Comparative Model Evaluation

Sl.No	Algorithm	Accuracy(%)	Jaccard index	Hamming score	Avg precision
1	PS(Pruned Sets)	62.9	0.371	0.014	0.876
2	RakEL (Random K-Label Pruned Sets)	56	0.44	0.985	0.594
3	DBPNN (Back Propagation Neural Networks)	41.7	0.583	0.981	0.992
4	PSt (Pruned Sets with Threshold)	43	0.43	0.889	0.471

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Resultant Features

	p1-VOH-VCC	p1-VIL	p1-VIH	p1-IOH	p1-VIK-VCC	p1-IIK	p2-VOH-VCC	p2-VIL	p2-VIH	p2-IOH	p3-VOH-VCC	p3-VIL	p3-VIH	p3-IOH	p3-VOL-VCC	p3-IOL	p4-VOH-VCC	p4-VIL	p4-VIH	p4-IOH
0	2.0	0.00	2.00	-20.00	0.0	0.0	4.50	0.0000	4.5000	-20.00	6.0	0.00	6.00	-20.00	0.0	0.00	4.50	0.0000	4.5000	-6.00
1	2.0	0.50	1.50	-0.05	0.0	0.0	3.00	0.9000	2.1000	-0.05	4.5	1.35	3.15	-0.05	0.0	0.00	3.00	0.9000	2.1000	-4.00
2	0.0	1.65	3.85	0.00	0.0	0.0	0.00	0.4950	1.0725	0.00	0.0	0.70	1.70	0.00	2.3	8.00	0.00	0.7000	1.7000	0.00
3	2.0	0.50	1.50	-0.05	0.0	0.0	3.00	0.9000	2.1000	-0.05	4.5	1.65	3.85	-0.05	0.0	0.00	3.00	0.9000	2.1000	-4.00
4	1.8	0.15	1.65	-0.05	0.0	0.0	3.00	0.9000	2.2000	-0.05	4.5	1.35	3.15	-0.05	0.0	0.00	3.00	0.9000	2.2000	-8.00
5	1.8	0.15	1.65	-0.05	0.0	0.0	3.00	0.9000	2.2000	-0.05	4.5	1.35	3.15	-0.05	0.0	0.00	3.00	0.9000	2.2000	-8.00
6	3.6	0.80	2.00	-0.10	0.0	0.0	1.65	0.5775	1.0725	-6.00	2.3	0.70	1.70	-12.00	0.0	0.00	2.30	0.7000	1.7000	-18.00
7	0.0	0.90	2.00	0.00	0.0	0.0	0.00	0.3850	0.7150	0.00	0.0	0.49	0.91	0.00	1.4	1.70	0.00	0.5775	1.0725	0.00
8	5.0	1.50	3.50	-10.00	0.0	0.0	10.00	3.0000	7.0000	-15.00	15.0	4.00	11.00	-20.00	0.0	0.00	0.00	1.5000	3.5000	0.00
9	3.0	0.90	2.10	-12.00	0.0	0.0	4.50	1.3500	3.1500	-24.00	5.5	1.65	3.85	-24.00	0.0	0.00	0.00	0.9000	2.1000	0.00
10	3.0	0.90	2.10	-12.00	0.0	0.0	4.50	1.3500	3.1500	-24.00	5.5	1.65	3.85	-24.00	0.0	0.00	0.00	0.9000	2.1000	0.00
11	3.0	0.90	2.10	-3.60	0.0	0.0	4.50	1.3500	3.1500	-6.00	6.0	1.80	4.20	-7.80	0.0	0.00	0.00	0.9000	2.1000	0.00
12	0.0	0.70	1.70	0.00	0.0	0.0	0.00	0.8000	2.0000	0.00	0.0	0.80	2.00	0.00	3.0	16.00	0.00	0.8000	2.0000	0.00
13	2.7	0.80	2.00	-12.00	0.0	0.0	3.00	0.8000	2.0000	-18.00	3.0	0.80	2.00	-24.00	0.0	0.00	3.60	0.8000	2.0000	-0.10
14	2.0	0.50	1.50	-0.05	0.0	0.0	3.00	0.9000	2.1000	-0.05	4.5	1.35	3.15	-0.05	0.0	0.00	3.00	0.9000	2.1000	-4.00
15	2.0	0.50	1.50	-0.05	0.0	0.0	3.00	0.9000	2.1000	-0.05	4.5	1.35	3.15	-0.05	0.0	0.00	3.00	0.9000	2.1000	-4.00
16	3.0	0.53	1.20	-0.05	0.0	0.0	4.50	0.8000	2.0000	-0.05	3.0	0.53	1.20	-4.00	0.0	0.00	4.50	0.8000	2.0000	-8.00
17	2.0	0.50	1.50	-0.05	0.0	0.0	3.00	0.9000	2.1000	-0.05	4.5	1.35	3.15	-0.05	0.0	0.00	3.00	0.9000	2.1000	-4.00
18	0.0	0.00	0.00	0.00	2.7	-18.0	2.70	0.8000	2.0000	-0.10	2.7	0.80	2.00	-8.00	0.0	0.00	3.00	0.8000	2.0000	-32.00
19	0.0	0.00	0.00	0.00	2.0	-18.0	2.00	0.5000	1.5000	-0.05	3.0	0.90	2.10	-0.05	0.0	0.00	4.50	1.3500	3.1500	-0.05

Resultant Targets

	DPS-short	ICC-VCC=6	VIL=0	VIH=6	IOL=0	IOH=0	VOL=0	VOH=6	FUNCGR-VCC=6	VOL=3	VOH=3	FUNCSTR-VCC=2	VIH=2	VOL=0.1	VOH=1.9	FUNCSTR-VCC=4.5
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	1	1	1	1	0	0	0	1	0	1	1	1
2	1	0	1	0	1	1	0	0	0	0	0	0	1	0	0	0
3	1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1
4	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1
5	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1
6	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0
7	1	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0
8	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
9	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
10	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
11	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	0
12	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0
13	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0
14	1	0	1	0	1	1	0	0	0	0	0	1	0	1	0	1
15	1	0	1	0	1	1	0	0	0	0	0	1	0	1	0	1
16	1	0	1	0	1	1	0	0	0	0	0	0	1	0	0	1
17	1	0	1	0	1	1	0	0	0	0	0	1	1	1	0	1
18	1	0	1	0	1	1	0	0	0	0	0	0	1	0	0	0
19	1	0	1	0	1	1	0	0	0	0	0	1	0	1	0	1
20	1	0	1	0	1	1	0	0	0	0	0	1	0	1	0	1
21	1	0	1	0	1	1	0	0	0	0	0	1	0	1	0	1
22	1	0	1	0	1	1	0	0	0	0	0	0	1	0	0	1
23	1	0	1	0	1	1	0	0	0	0	0	0	1	0	0	1
24	1	0	1	0	1	1	0	0	0	0	0	0	1	0	0	1
25	1	0	1	1	1	1	0	0	1	1	1	1	0	1	1	1

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Dinesh
Lavanya

Machine Learning Model 2

Phase 1:

- Targets of Phase 1 is the features for ML model 2
- One hot encoding is used to change it as feature for next phase

Phase 2:

Classify objects using LC: Label Powerset

Base classifier:J48

Require_dense – whether the base classifier requires dense representations for input features and classes/labels matrices in fit/predict.(Total targets 797)

Phase 3:

Associate the tests using MMAC(Multiclass Multilabel Associative Classification) Apriori

Produce rule set using frequent items

Rank the rule set based on support and confidence

Repeat untill no frequent item is found

Merge rules and classify objects

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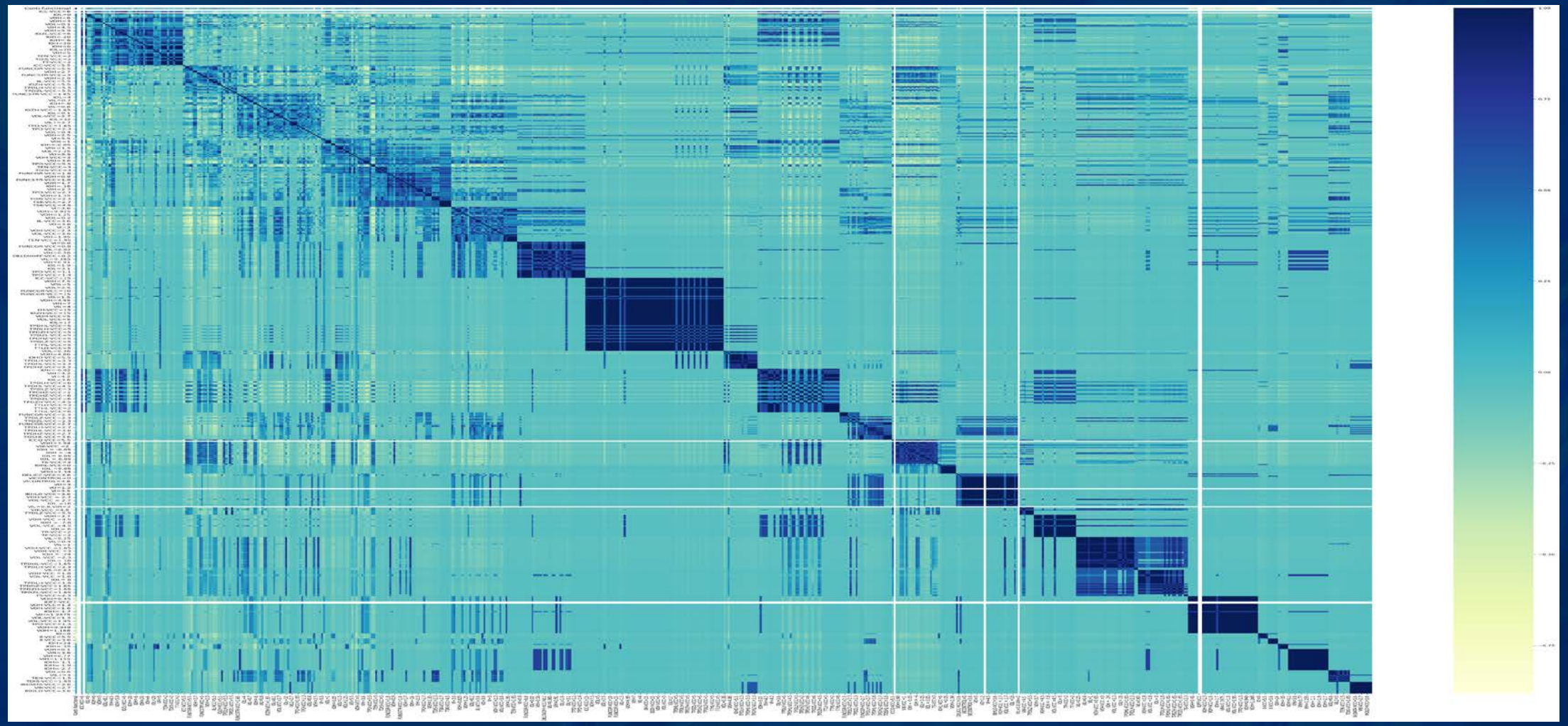
Correlation Matrix of the Targets



Highly correlated

Least correlated

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Comparative Model Evaluation

Sl.No	Algorithm	Accuracy(%)	Jaccard index	Hamming score	Avg precision
1	LC(Label Powerset)	76.9	0.231	0.992	0.8
2	BCC (Bayesian Classifier Chain)	76.9	0.231	0.992	0.8
3	CDN (Conditional Dependency Networks)	54.1	0.451	0.986	0.88
4	BRq (Binary Relevance – Quick Version)	75.6	0.244	0.67	0.7998

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Test Program Generation Summary

Use case:

Device : ASIC ICs

ATE platform: Advantest V93K

Total devices: 250

ATE loadable files

Pin Config files:	TestGeni
Levels:	ML and TestGeni
Timing:	Vector conversion
Pattern:	Vector conversion
Test limits:	ML and TestGeni
Test flow:	ML and TestGeni

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Conclusion and Future Work

- In the quest for precision, a symphony of AI automation plays its part, yet the conductor's touch of human intervention ensures the perfect performance.

- Test development time slashed significantly.

Future work:
Training the model to generate the schematic design from test specifications

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- Jesse Read. 2008. A Pruned Problem Transformation Method for Multi-Label Classification. In Proceedings of the New Zealand Computer Science Research Student Conference (NZCSRS’08). University of Canterbury, Christchurch, Canterbury, New Zealand, 143–150. [47]

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Thank you

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Senthilkumar
Dinesh
Lavanya

Probes Cleaning Effectiveness challenges for fine pitch and high-densities Logic Probe Cards with MEMS tips

Wen Jung CHANG
Micron Memory Taiwan Inc.

Outline

- **Introduction**
- **Challenges of effectiveness online Needle Cleaning**
  - Overlapping cleaning movement
  - Reuse cleaning foils at limited cleaning substrate
  - Constraints of in-situ cleaning selections
  - Ineffective cleaning leads to dirty tips
  - Consequences of contaminated probe tips
- **Consequences after needle cleaning**
- **Out of the box thinking - possible solutions**
- **Follow-on Works**

Outline

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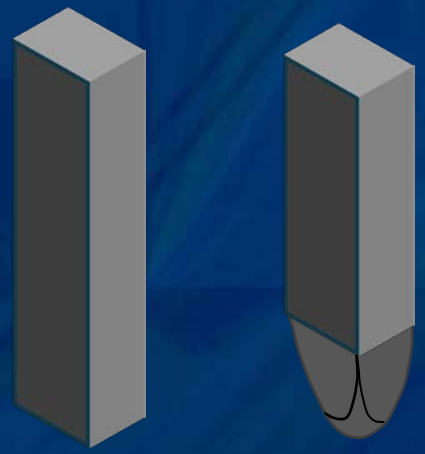
- **Out of the box thinking - possible solutions**
- **Follow-on Works**

Introduction

- MEMS probes are widely used in logic probe cards.
- MEMS advantages: position accuracy, fine pitch, high pin counts, low contact force, easy maintenance, etc.
- Variety of probe shapes to contact wafer side, such as flat, radius, point, etc.

Micro-Electrical-Mechanical Systems



Introduction

- Debris build-up occurs on probe tips during testing. And on-line cleaning is required to maintain good contact.
- In the presentation today, we will be focusing on vertical and flat type of probes to contact Cu-pillar bumps.
- After several on-line cleaning cycles, what happens to probe tips?
- What's the best of cleaning process?

Outline

- Introduction
- **Challenges of effectiveness online Needle Cleaning**
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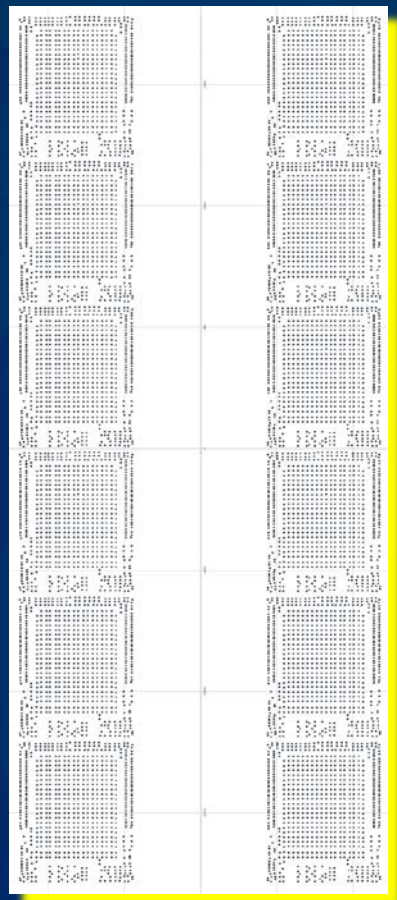
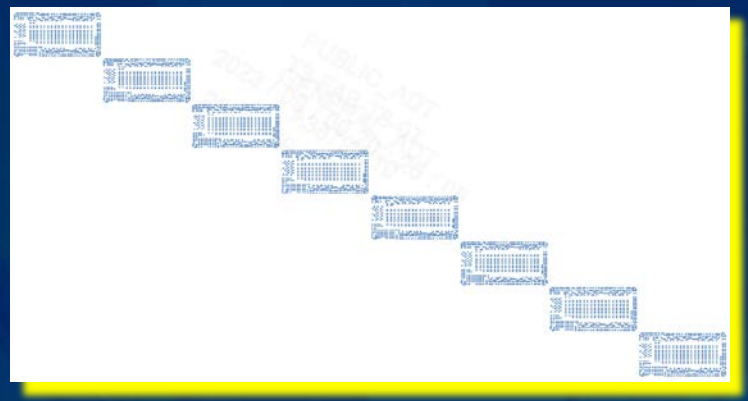
- Consequences after needle cleaning
- Out of the box thinking - possible solutions
- Follow-on Works

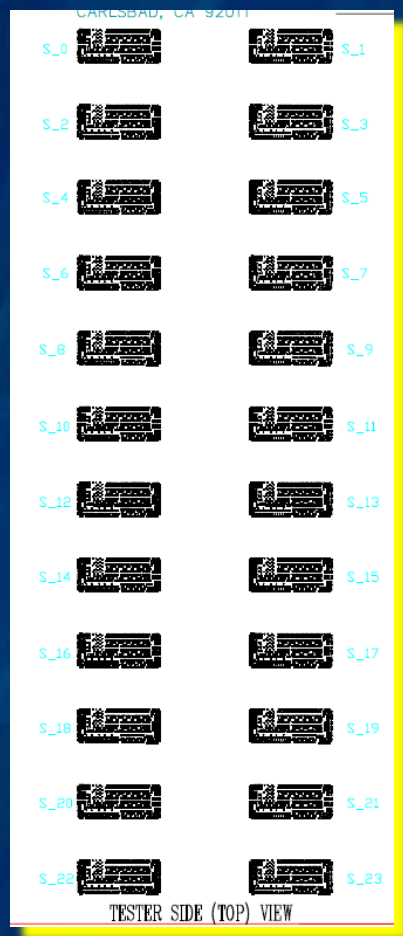
Challenges of Effectiveness on Needle Cleaning

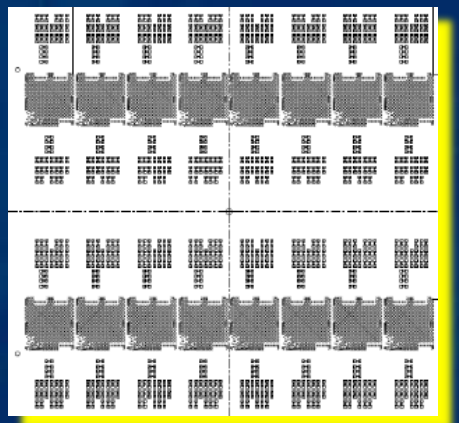
- **MEMS probe cards are frequently designed for fine pitch, high density, high parallelism, and high pin count devices.**

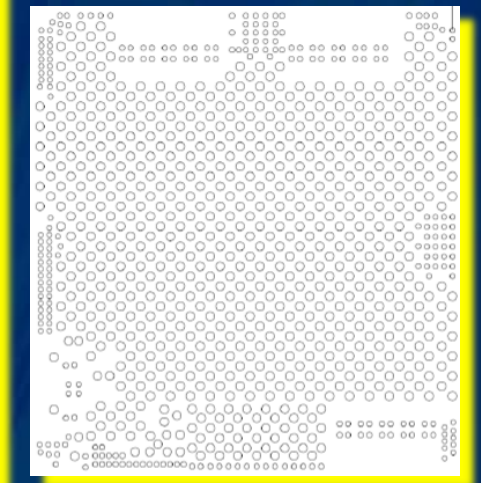




Fine pitch and high density < 80um
High Pin Counts > 8K pins
High Parallelism > 8 DUTs or more



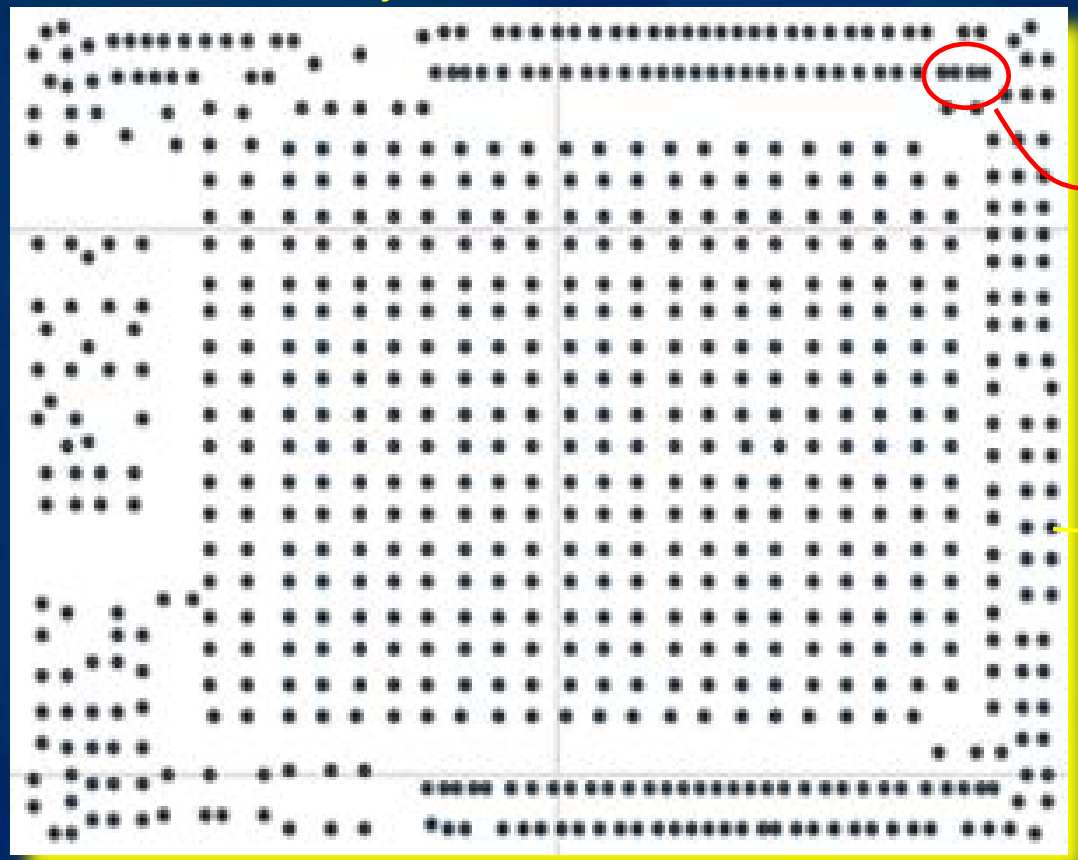




Challenges of Effectiveness on Needle Cleaning

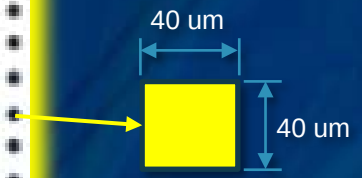
- **Example #1: Single cleaning movement, no overlapping.**
  - **Moving distance calculated accurately.**

Needles layout on one of DUTs



Minimum clearance= 50um

Needle size

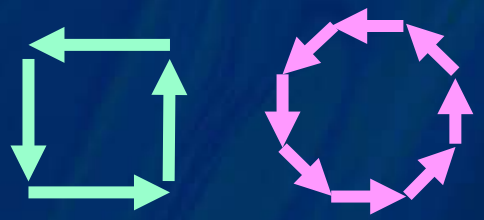


Cleaning movement:
At X direction < 40~50um

At Y direction < 80~100um

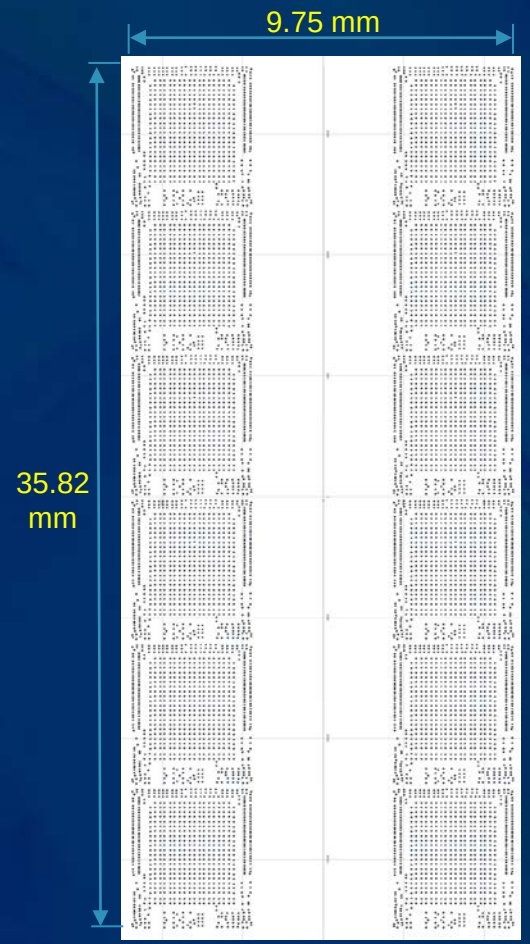
At X+Y direction < 40~50um

At Octagon direction < 40~50um

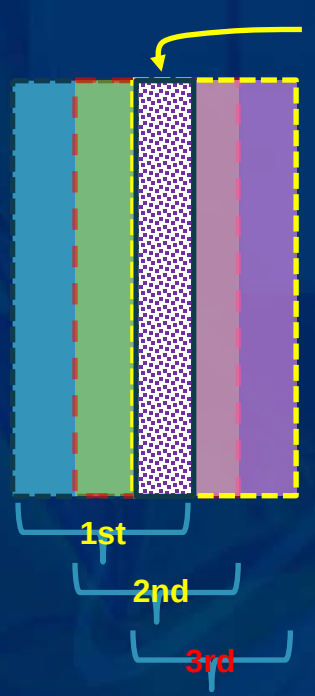


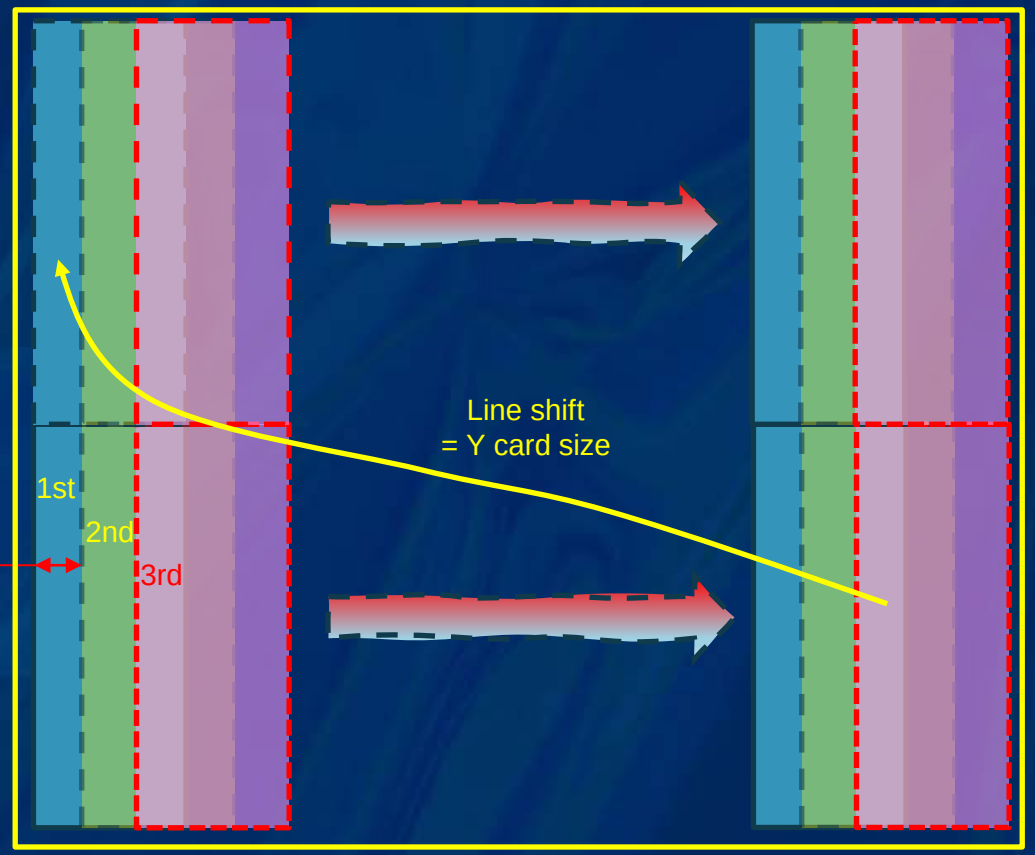
Challenges of Effectiveness on Needle Cleaning

- **Example #2: > 3rd TD, overlapping occurs on cleaning material**
  - Most probes touch dirty area of cleaning foils.

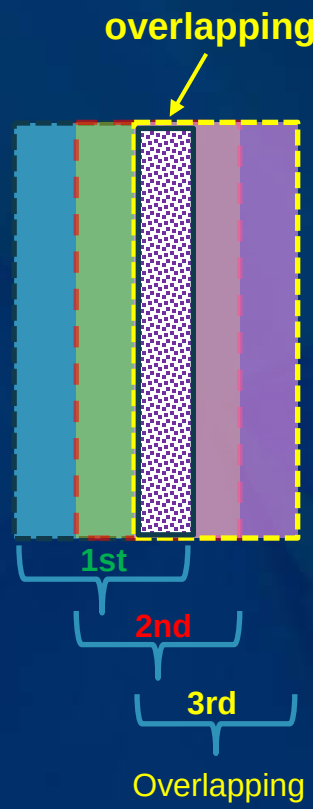


Layout: X=2, Y=6, 12 DUTs, X skip 1
Probe diameter = 40 x 40 (um)
Probe Tip Shape: Flat
Pitch: < 80um
Number of Probes: > 8K

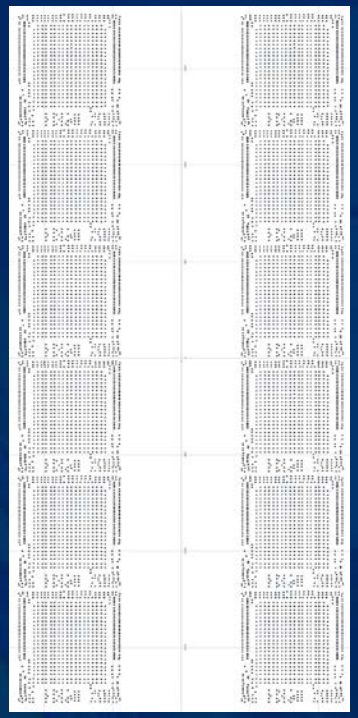




• Why do we care overlapping at needle cleaning?

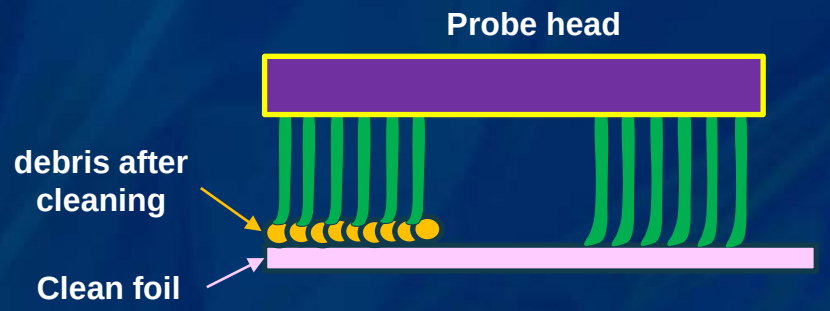


Left side will be touching dirty foil



Right side will touch a cleaner foil

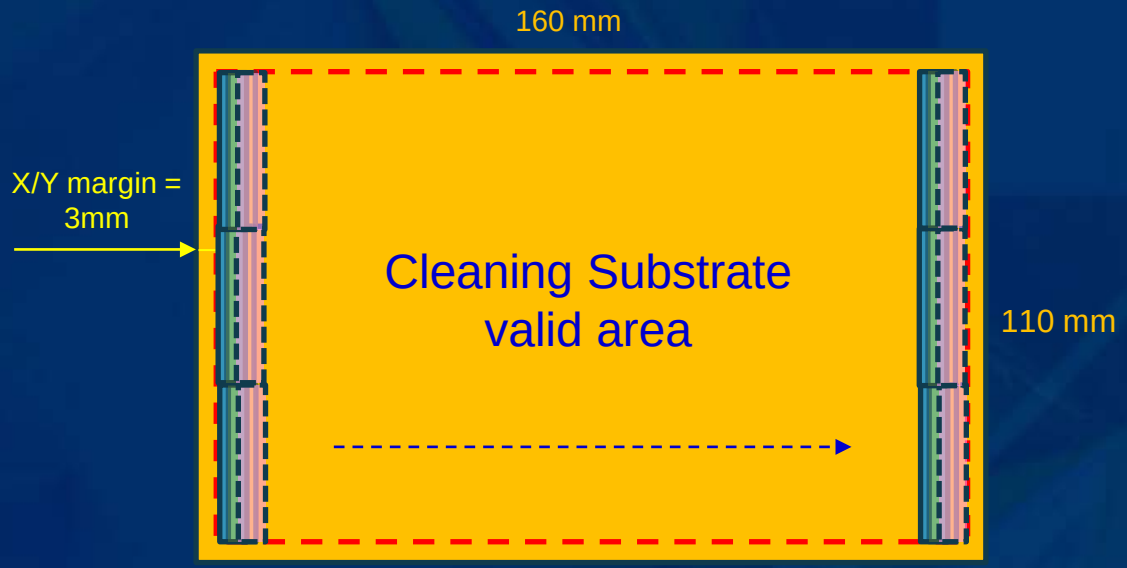
Microscopic feature of cleaning movement

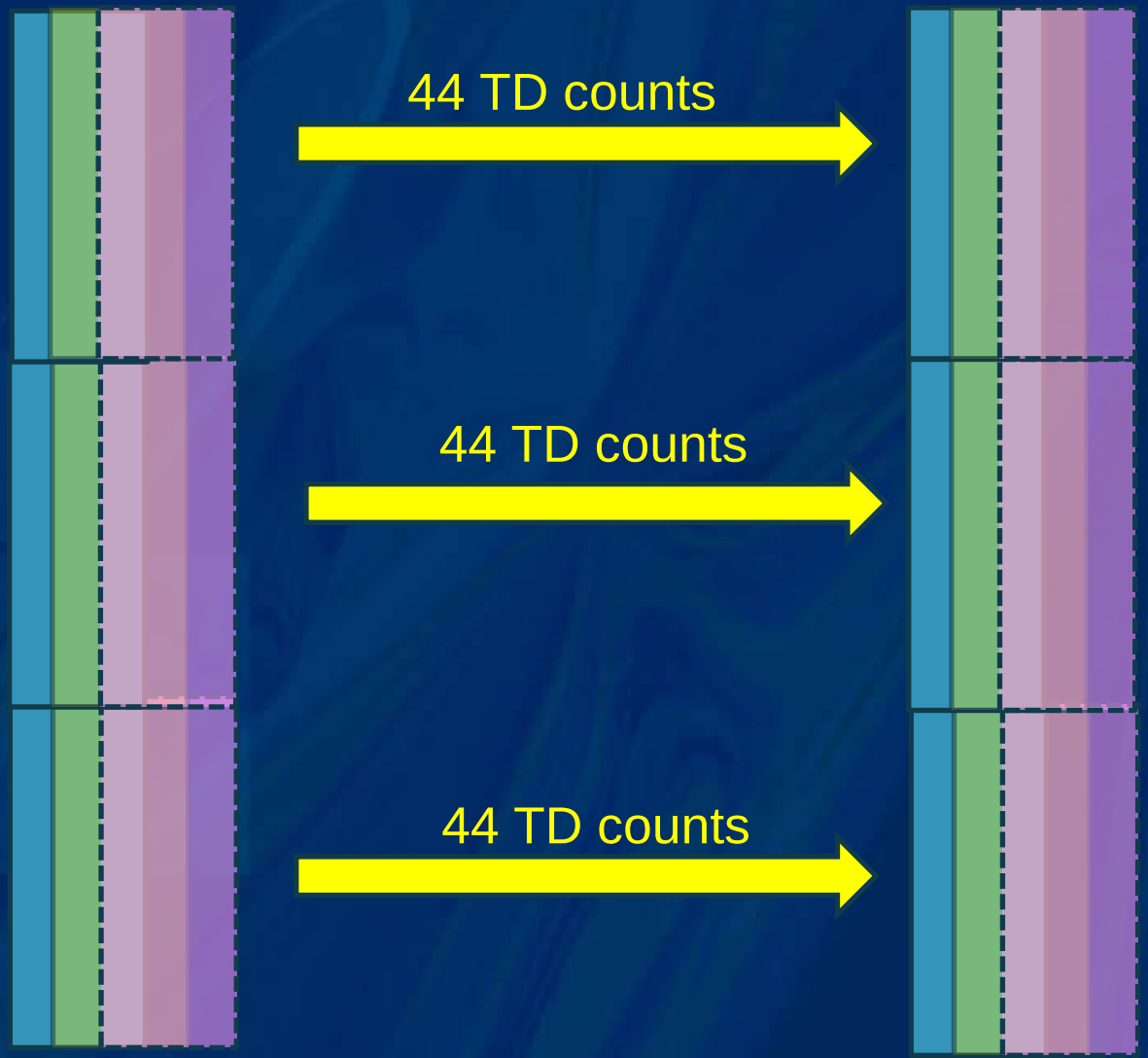


Compared to left side of DUTs, right side of probe tips will always be touching new foil area and scratched stronger. Cleaning effectiveness in between and probe length will cause adverse effects in the long run.

Reuse cleaning foil at limited cleaning substrate

TD counts at X direction : 154 / 3.5 = 44
TD counts at Y direction : 104 / 35.82 = 3
One cycle can ONLY use 44x3=132 cleaning TD
The prevailing practice is to reuse the same cleaning foil touching the same positions. And recycle material several times without replacing.
This clean paper will be getting dirty again.



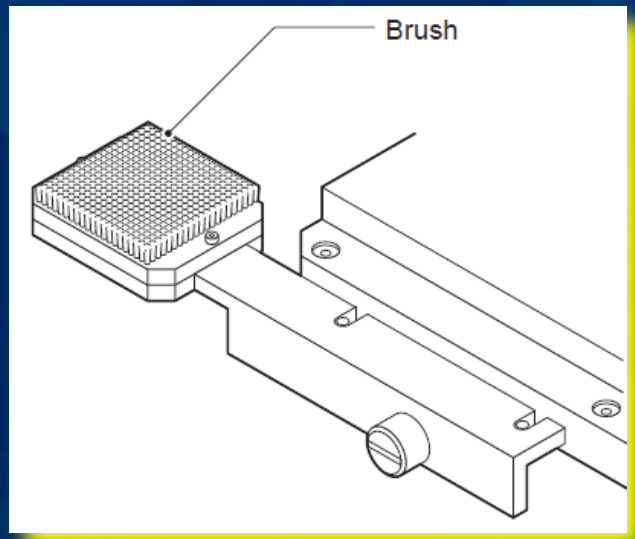


Constraints of In-situ cleaning selections

With current prober configurations, no obvious way to use large area and multiple lapping films at the same time. No obvious way to use liquid or chemical materials, no obvious way to install other tools for cleaning.

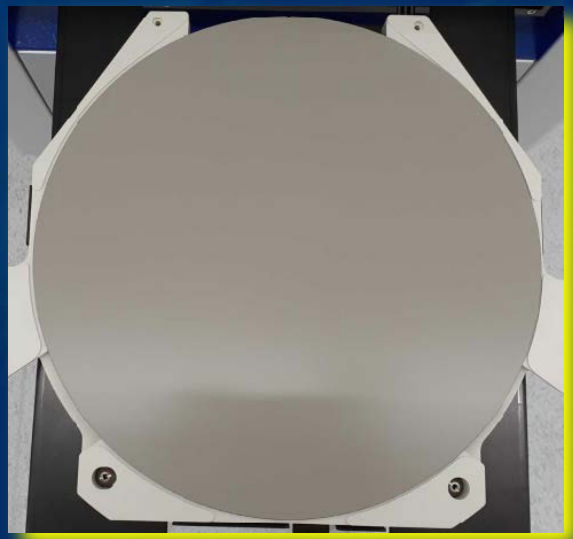
Clean Substrate

Brush



source: Accretech document

Clean wafer

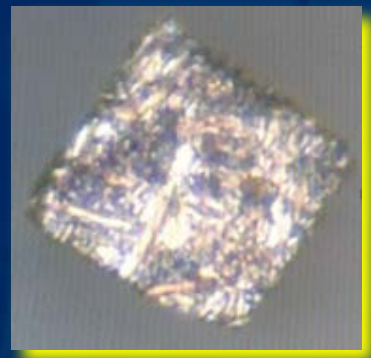


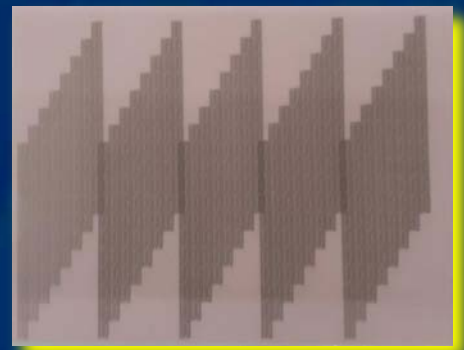
Ineffective cleaning leads to dirty tips

Probe tips get contaminated frequently because of …

- Overlapping at cleaning movement
- Reuse cleaning foil at limited cleaning substrate
- Constraints of cleaning unit selections







Pictures do not necessarily represent Micron's production condition

Consequences of contaminated Probe tips

- Contact issues (a.k.a. CRES instability)
- Affect testing data quality
- Wafer yields drop
- IRT (In-line Retest) rises and Lower OEE (Overall Equipment Effectiveness)
- Push up testing costs
- Affect equipment uptime and prober setup
- Engineers assist needed for setup or troubleshooting
- Lapping needles abrasively required to remove contaminations
- Shorten lifespan of probe cards

…etc.

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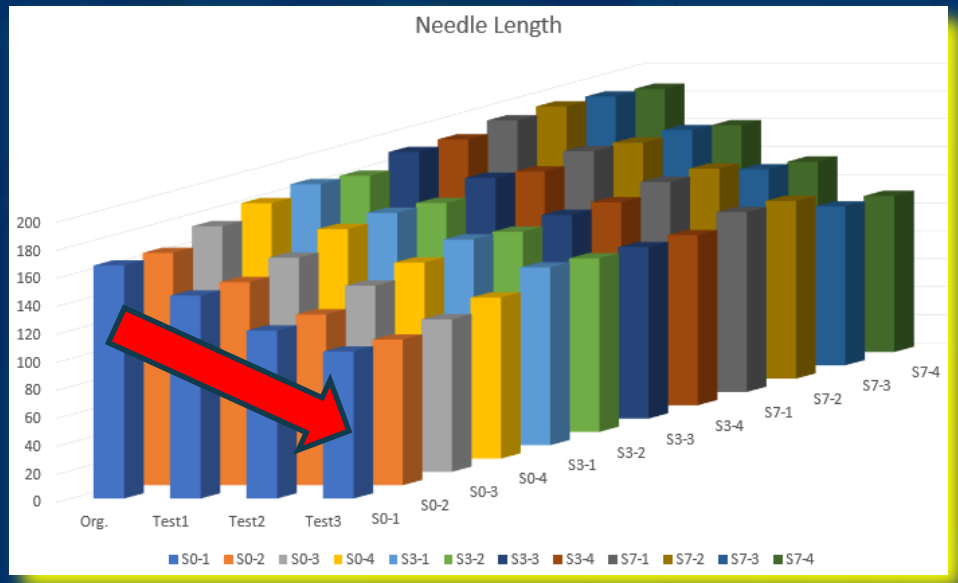
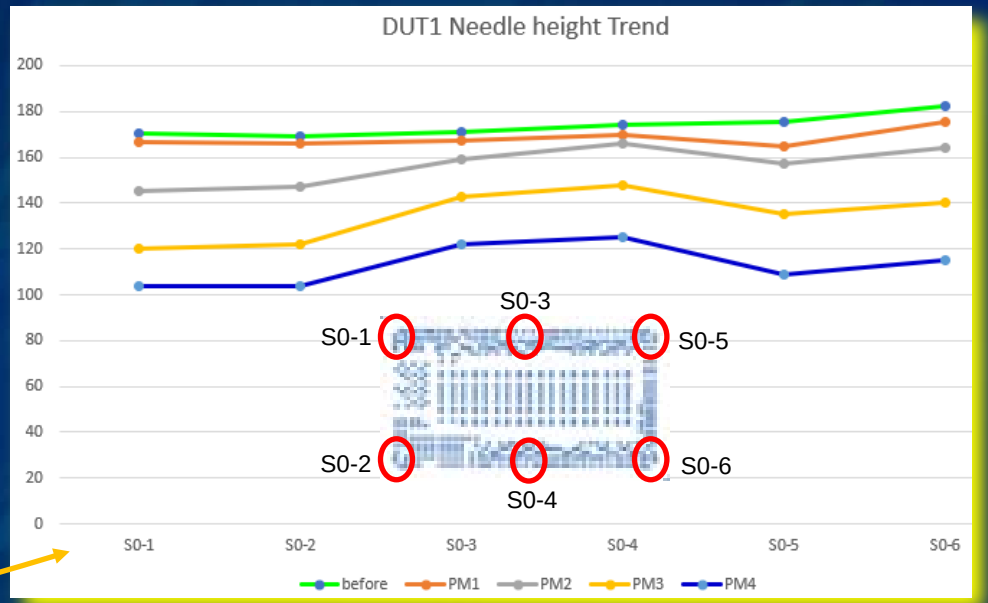
- **Consequences after needle cleaning**
- Out of the box thinking - possible solutions
- Follow-on Works

Consequences after needle cleaning

Cleaning conditions: the same COD, frequency, X+Y movement & same paper.

- Probes are getting shorter and shorter.



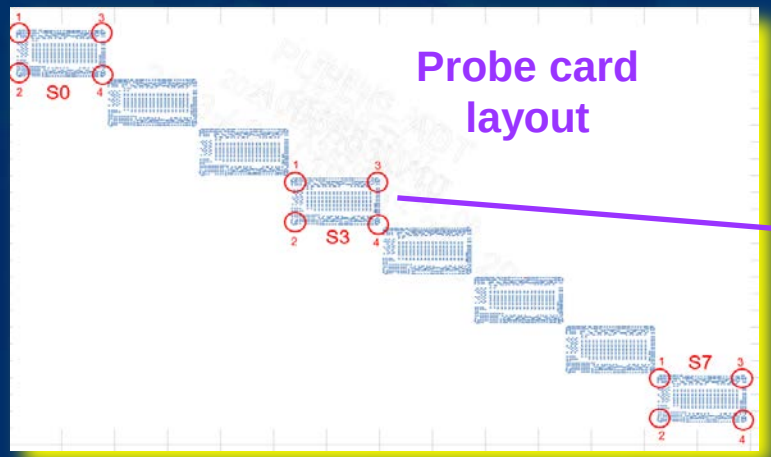


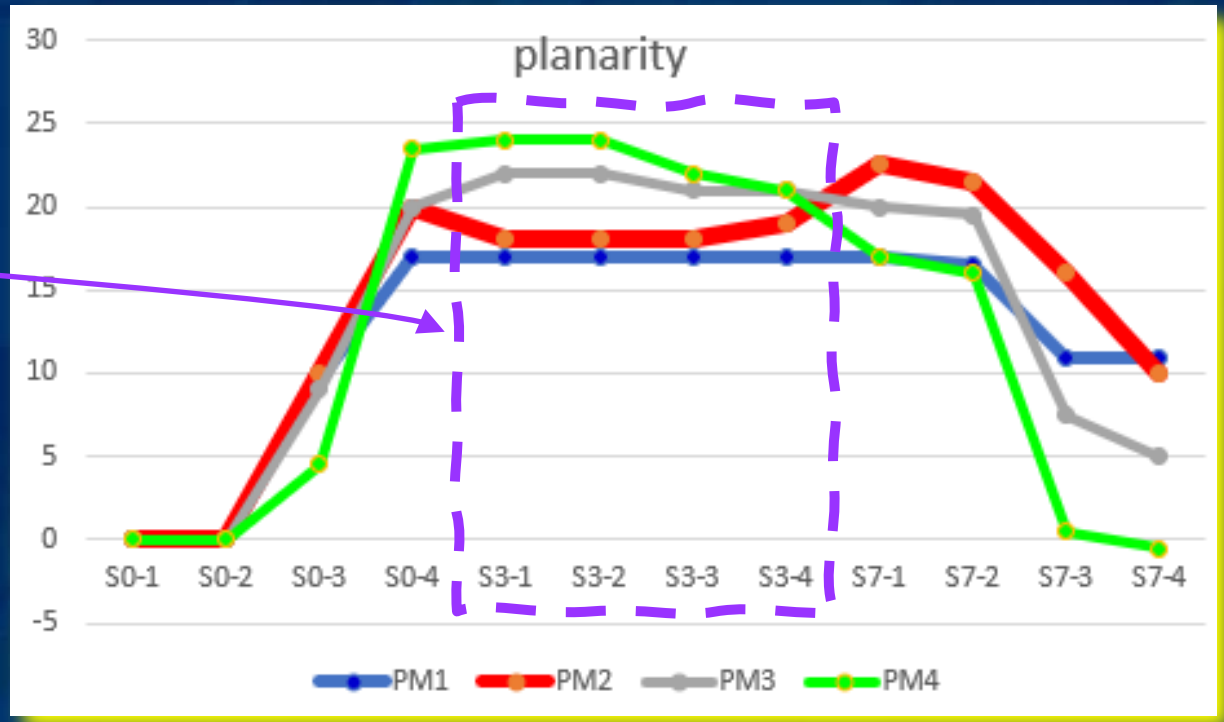
- Probes uneven in one DUT

Consequences after needle cleaning

- **Probes planarity between DUTs is getting worse.**

  Coplanarity between center DUTs and both ends of DUTs will be getting worse along with consecutive cleaning on the same film.

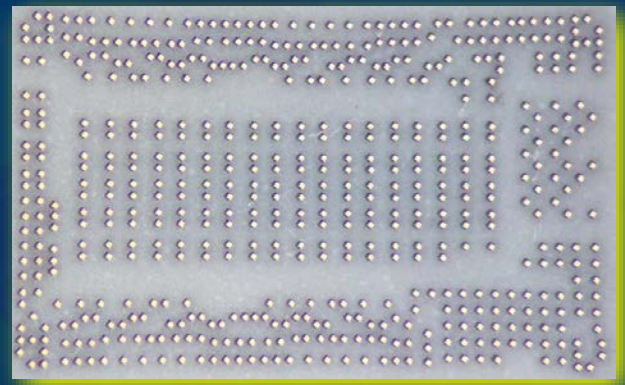


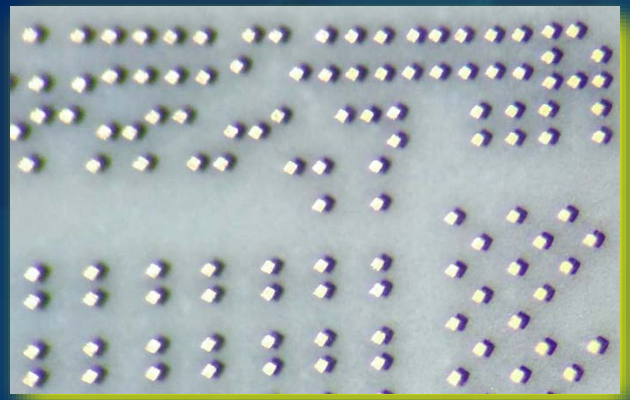


Consequences after needle cleaning

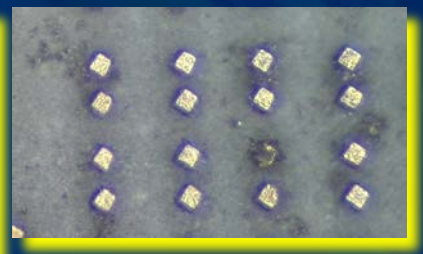
- **Ineffective cleaning**

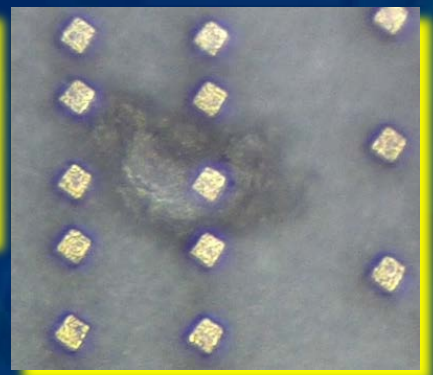
Before Testing, probe tips are clean.

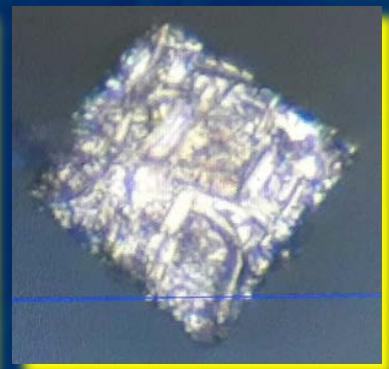


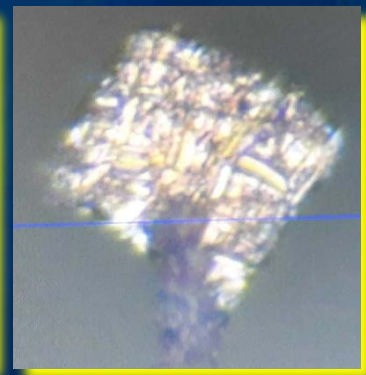


During testing, debris build up despite on-line cleaning being enabled.









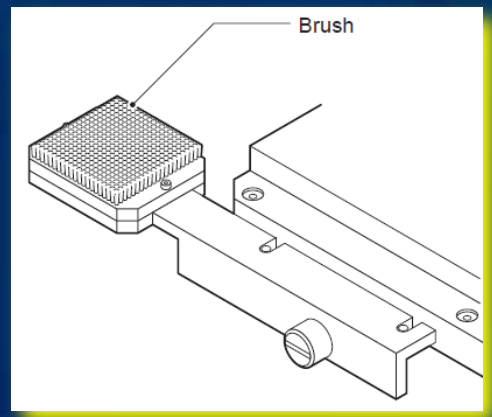
Outline

- Introduction
- Challenges of effectiveness online Needle Cleaning
  - Overlapping cleaning movement
  - Reuse cleaning foils at limited cleaning substrate
  - Constraints of in-situ cleaning selections
  - Ineffective cleaning leads to dirty tips
  - Consequences of contaminated probe tips
- Consequences after needle cleaning
- **Out of the box thinking - possible solutions**
- Follow-on Works

Out of the box thinking possible solutions

Brush clean

- ☹ Feasible for online clean, risk of probe damage & ineffective



Ultrasonic

- ☹ Wet cleaning, liquid, effective for loose debris, unfeasible for online clean

Laser

- ☹ High risk, may affect or damage PH, infeasible for online clean

Chemical

- ☹ Often toxic, high risk and might affect or even damage PH, unfeasible for online clean

Abrasive

- ✓ **Feasible & primary method for online clean.**
- **Drawbacks include: lifespan, maintenance & lower OEE**

What's the best cleaning process?

The better answer could be "NO Cleaning required". ☺

Micron's Challenge to the Industry !

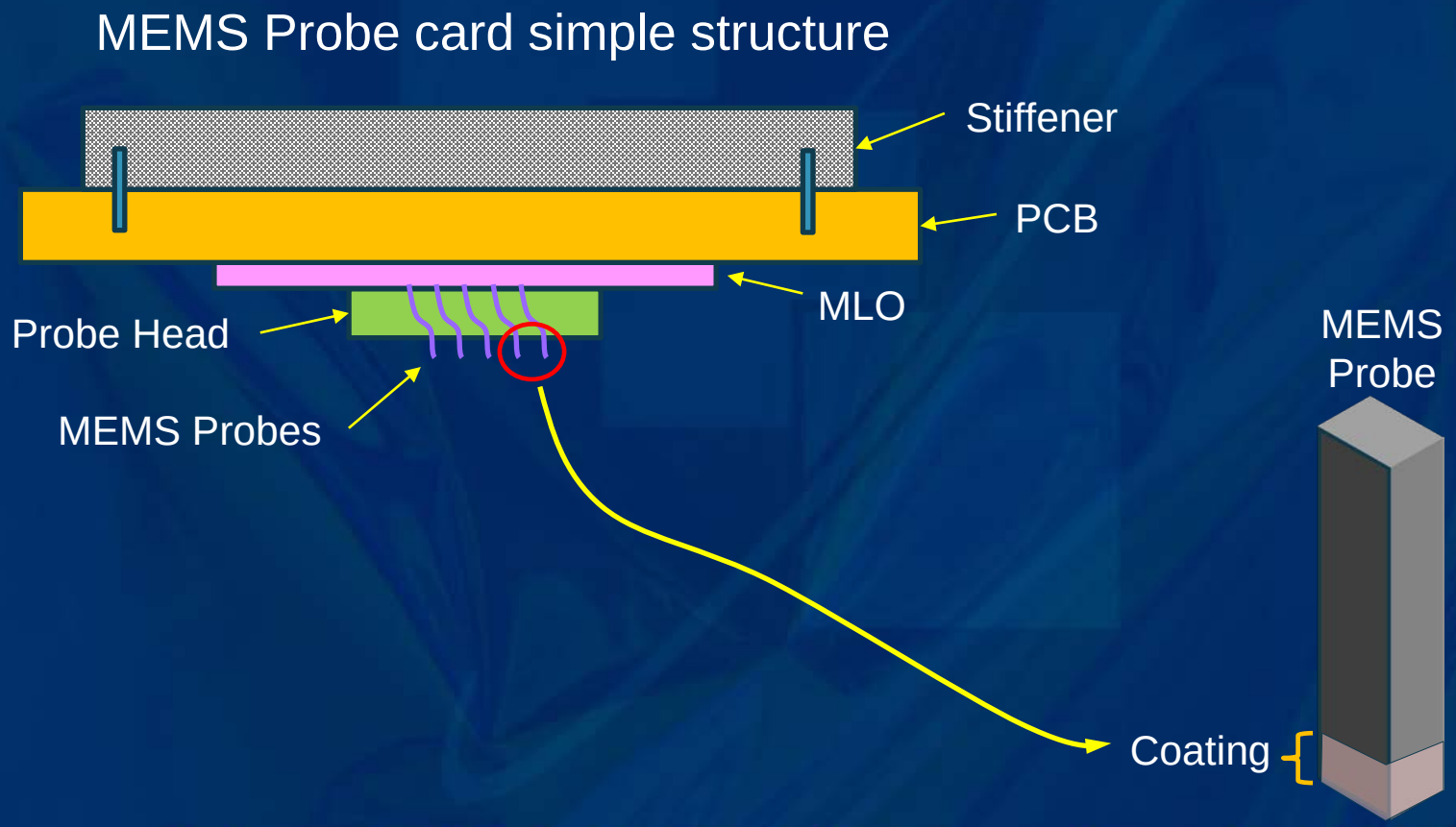
Probe tips sealed with a COATing.

NOTHING STICKS TO
"HAPPY PROBE CARDS"
☺

Teflon, nothing sticks to cookware.

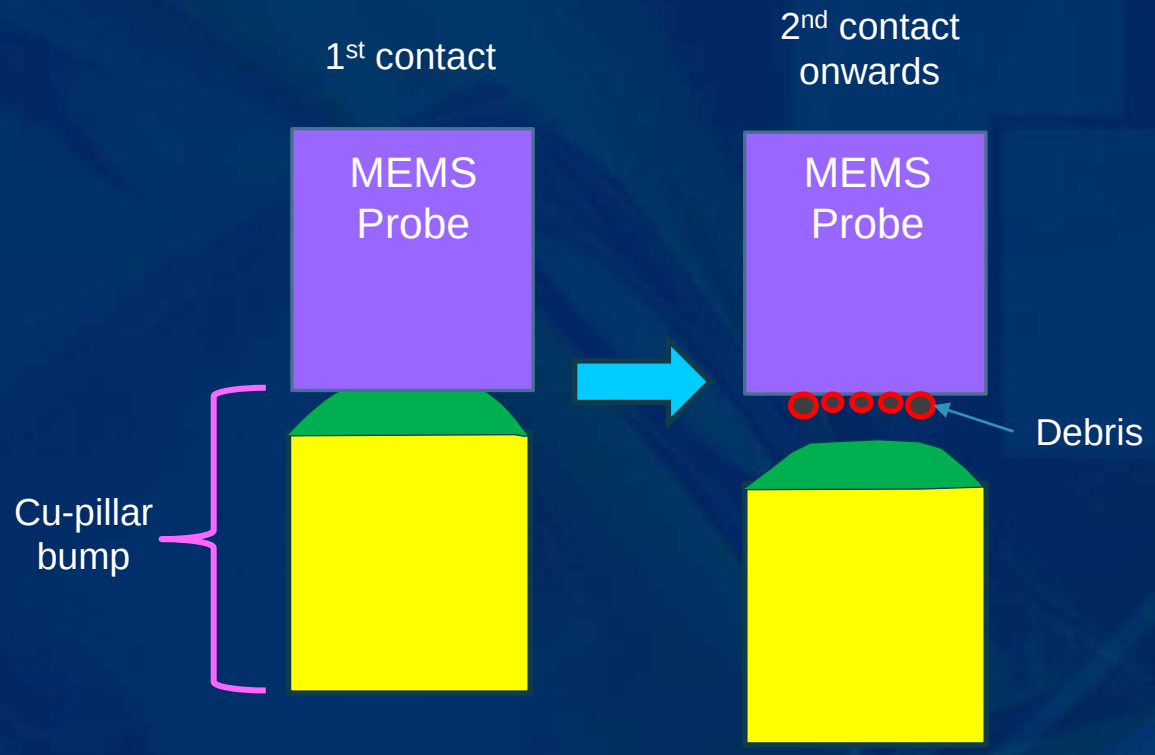
Coating illustration of Probes tips

The coating must be conductive, extremely hard, low-frictional materials and can prevent debris build-up.

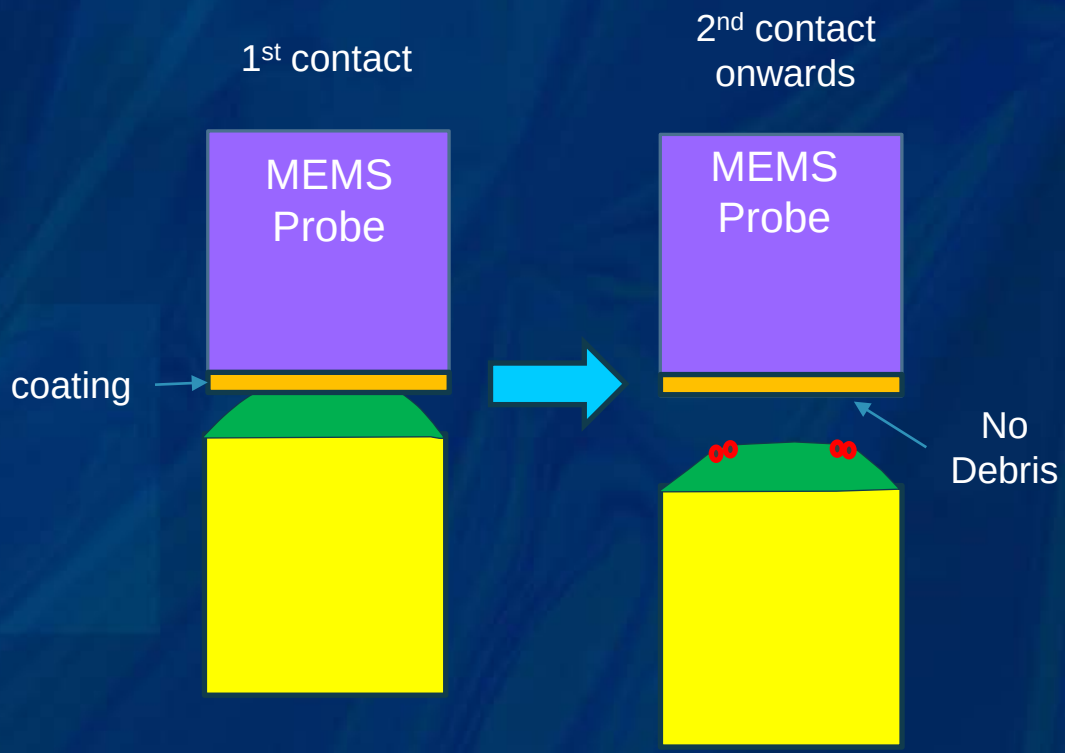


Schematic: Coating prevents debris build-up

Probe tip WITHOUT coating



Probe tip WITH coating



Goal of Coating for NO-Cleaning Probes

Probes won't get contaminated & provide zero wear out.

- ✓ **A reliable CRES**
- ✓ **Excellent First Test Yields**
- ✓ **Less Re-test**
- ✓ **Less probe cards maintenance**
- ✓ **Preserving the overall shape of the probe tip**
- ✓ **Long life-span of probe cards**
- ✓ **A higher OEE**

… etc.

Outline

- **Introduction**
- **Challenges of effectiveness online Needle Cleaning**
  - Overlapping cleaning movement
  - Reuse cleaning foils at limited cleaning substrate
  - Constraints of in-situ cleaning selections
  - Ineffective cleaning leads to dirty tips
  - Consequences of contaminated probe tips
- **Consequences after needle cleaning**
- **Out of the box thinking - possible solutions**
- **Follow-on Works**

Follow-On works

- Coating thickness
- Yield performance at high and low temperature testing
- Lifespan of coating at high and low temperature testing
- In-situ simple clean require?
- Clean sheet selection for on-line clean if necessary.
- Off-line PM cycle time and clean tools?
- CRES condition if it is idle for a period of time
- Feasibility to do re-coating for used MEMS probes

Acknowledgements

- **Special thanks to:**
  - **Ardentec**
    - PTE: Bradley Chen
    - H/W: Ji Jeng
    - P/C Team: Jack Hsieh
  - **Micron Memory Taiwan**
    - TSE/KEG:
      - Alistair Laing
      - Hoi Foo Mak

SWTEST ASIA

Probe Card Maintenance with Artificial Intelligence Assistance System

MPI CORPORATION

Anthony Fan, Adolph Cheng

1 2 3

Ying-Jen Chen[1], Jia-Yu Peng[2], Chen-Fu Chien[2,3]

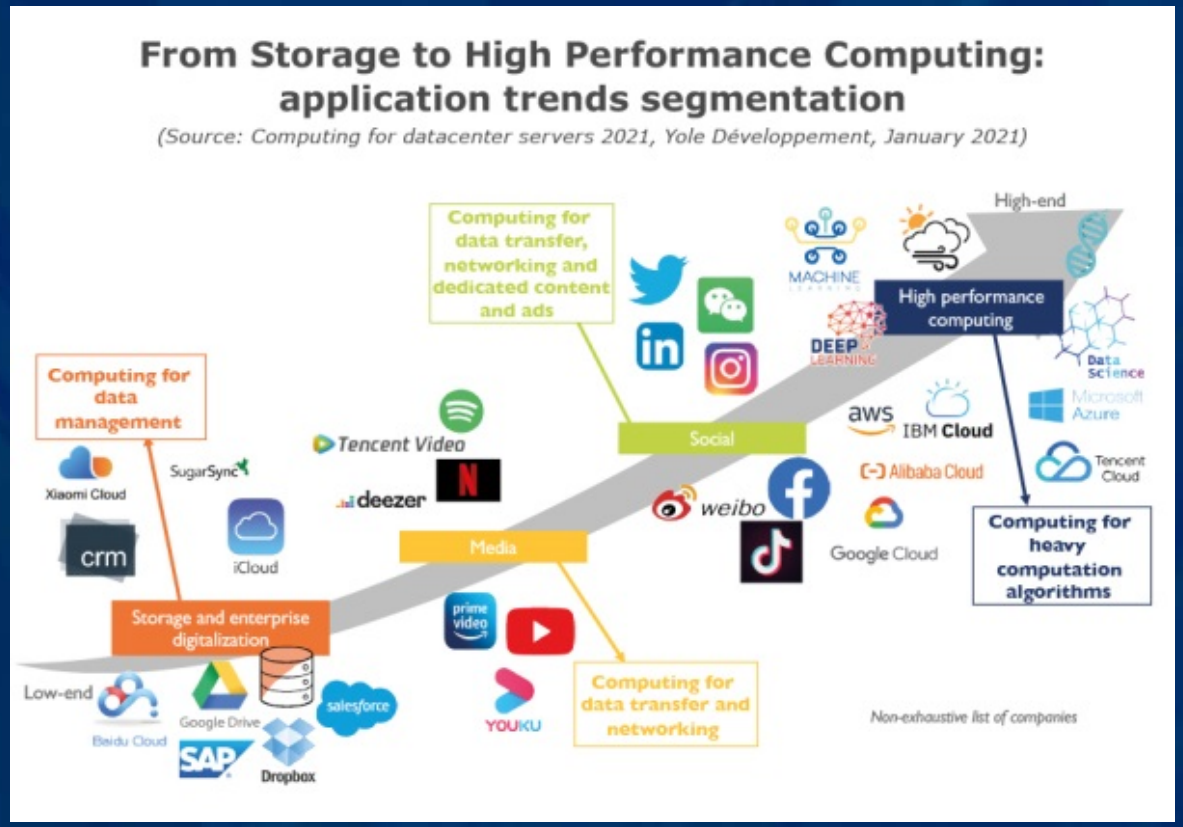
4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

Outline

- IoT、Data Center and AI Effect to Chip Probing
- Bottleneck of Probe Card Maintenance
- Benefits of Artificial Intelligence Assistance System
- Artificial Intelligence Assistance Methodology
- Summary

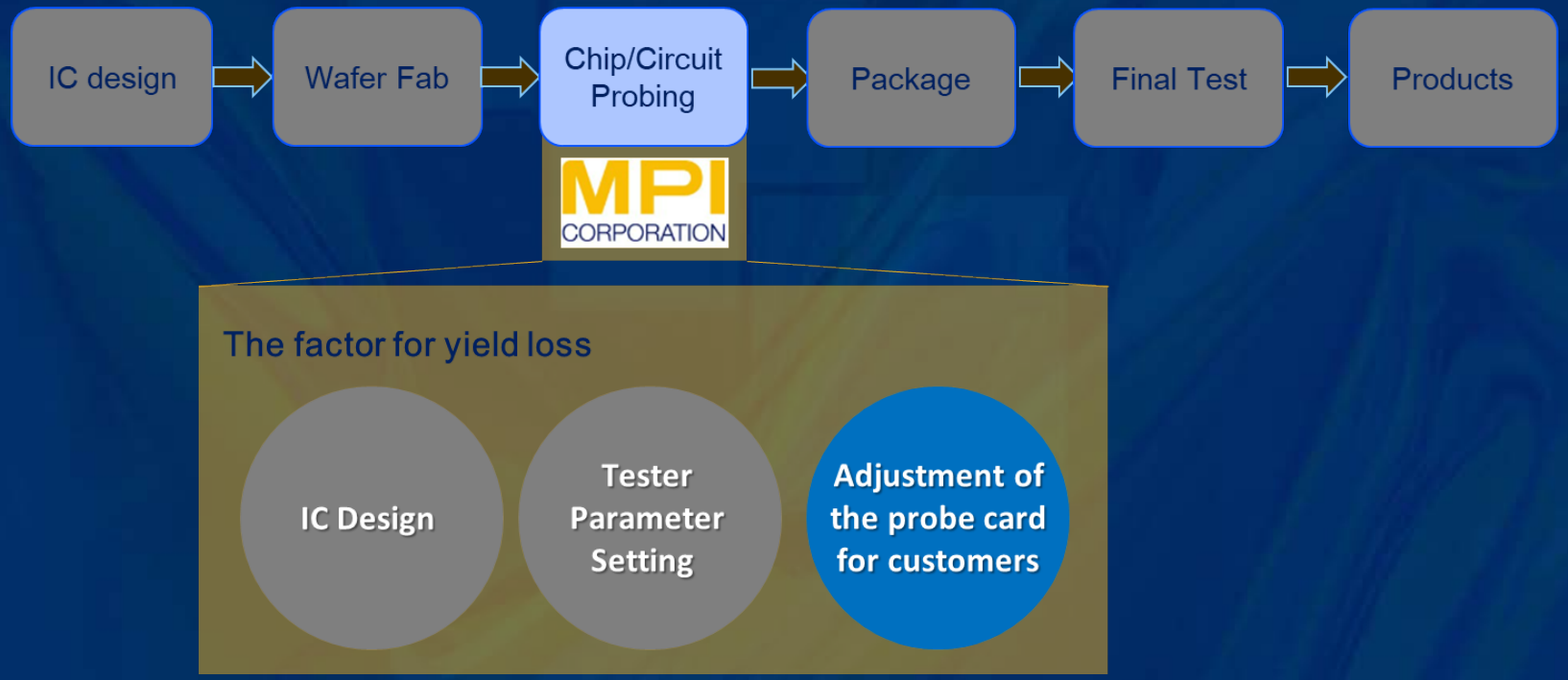
IoT、Data Center and AI Effect to Chip Probing

- **With the development of technologies such as IoT, Data Center and AI, the terminal applications of integrated circuits have become more diverse, which has also led to an increase in the complexity of chip probing.**



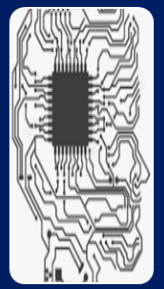
IoT、Data Center and AI Effect to Chip Probing

- In the face of increasing test complexity, the entire test system of integrated circuit still has many adjustments to be made in the test function design and the tester parameters and usage settings.
- If the combination is not good, yield loss or even loss will occur in the test. It cannot be tested, so the probe card manufacturer must adjust (repair) the probe card to assist customers in smooth mass production troubleshooting.



Bottleneck of Probe Card Maintenance

- **No easy to train maintenance personnel with multiple professional abilities.**
- **Due to know-how and business secrets, the tester program is locked, causing the testing factory to be unable to provide accurate abnormal information.**
- **How to reduce the timeliness and improve the accuracy of repairing abnormal probe cards is very challenging.**

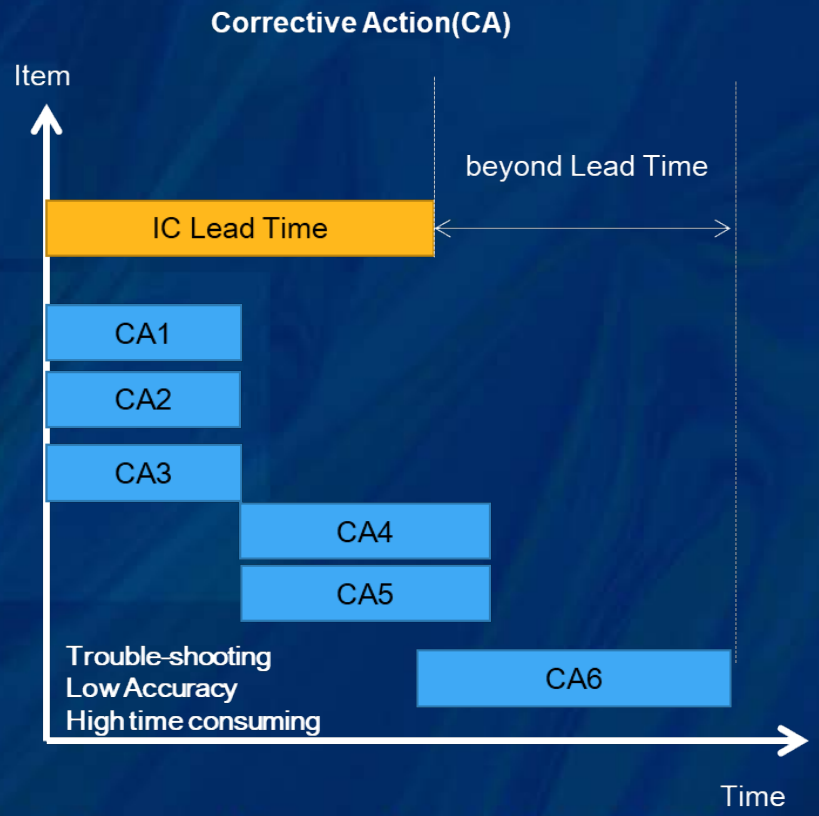


Not easy to train personnel

- Personnel with Diverse professional abilities in the use of mechanical/electrical/tester hardware and software

Information Lacking

Due to know-how and business secrets, the program is locked, causing the testing factory to be unable to provide accurate abnormal information.



Benefits of Artificial Intelligence Assistance System

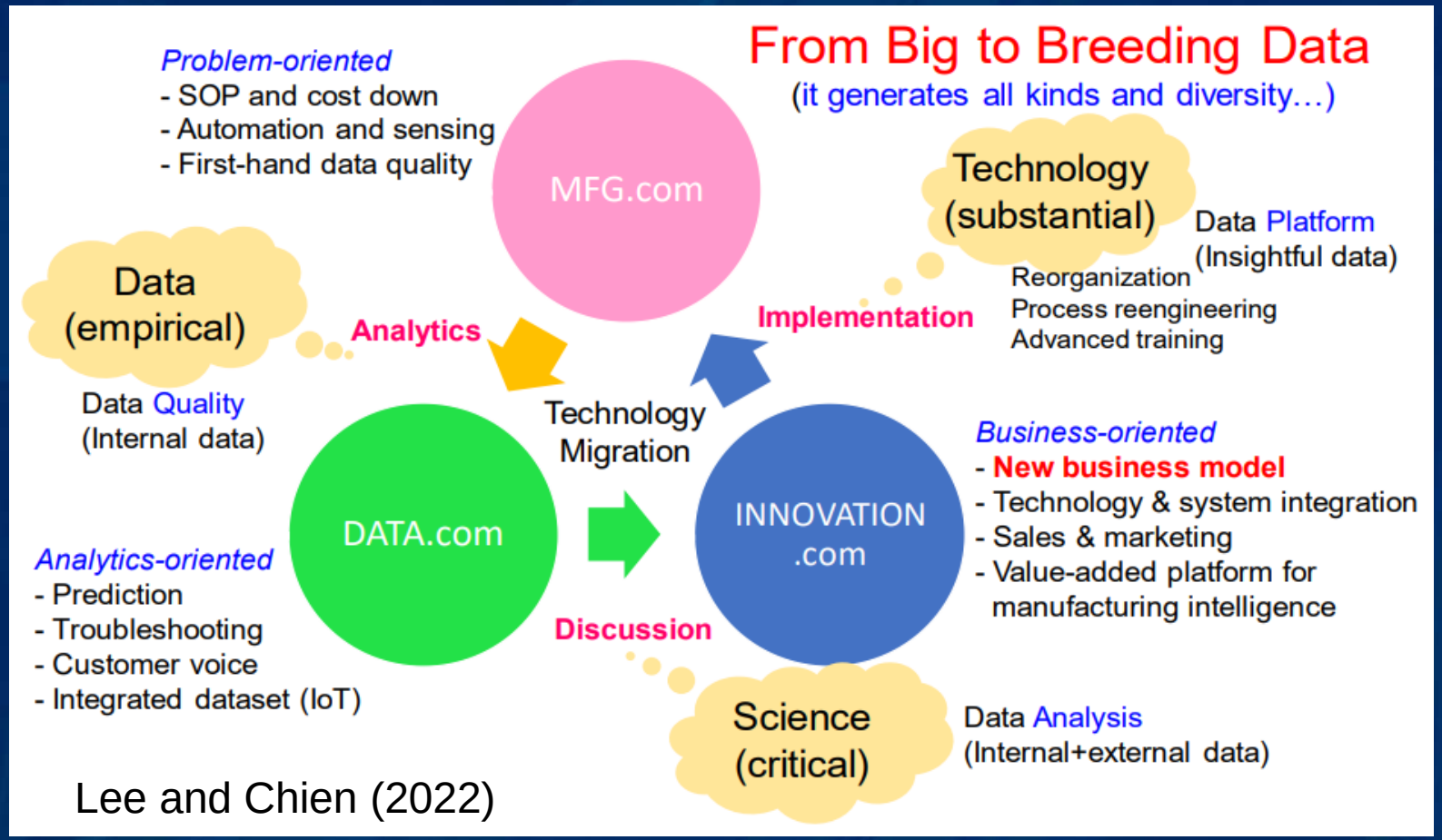
- **With only 0.5 years of training time, maintenance personnel can propos the 60% overall accuracy of corrective action.**

Maintenance Personnel
First Time Right

Overall Accuracy 60%
with Only 0.5 Years Training

Data Health Check-up

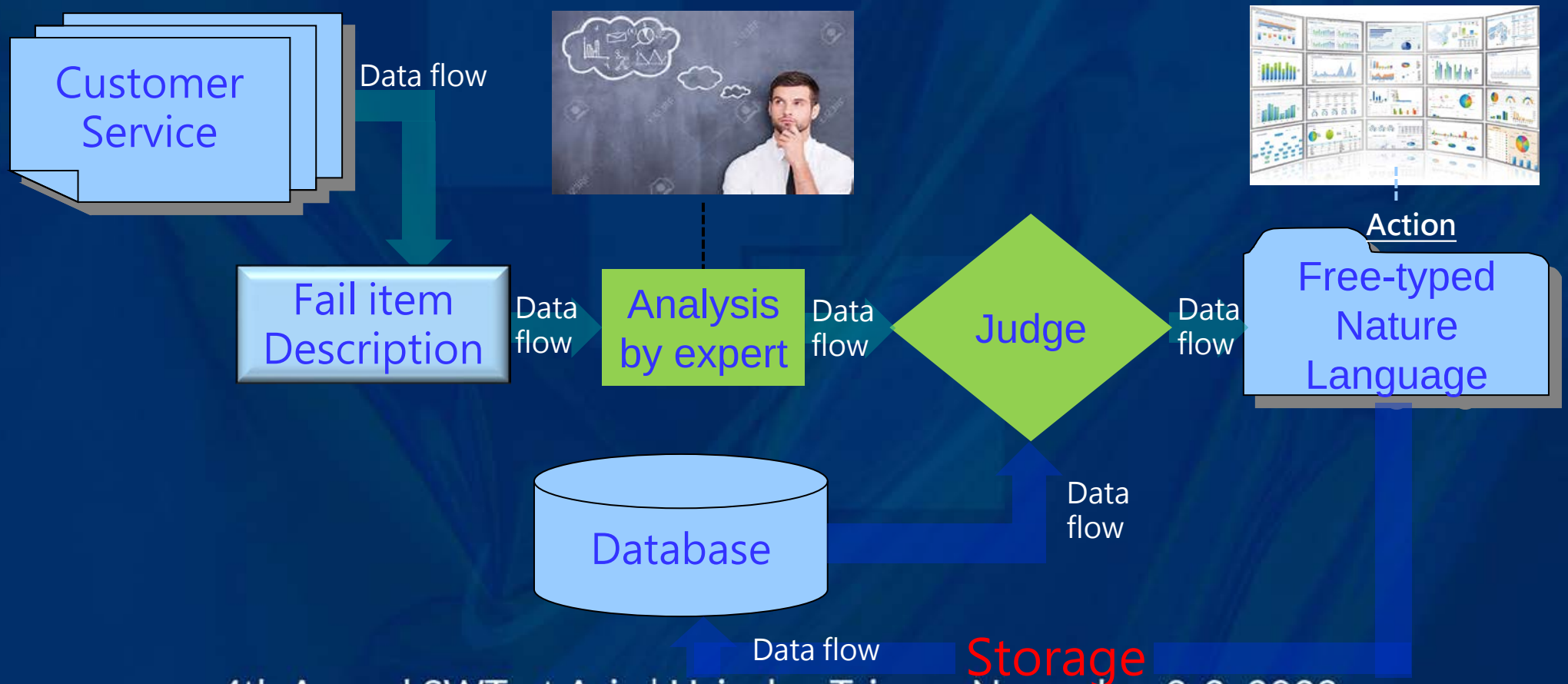
- **Begin with the end in mind! How data is used determines data value as well as IT system design.**
- **Analytic-oriented IT system design: collecting data for analytic purposes, under the existing operation process.**



Lee and Chien (2022)

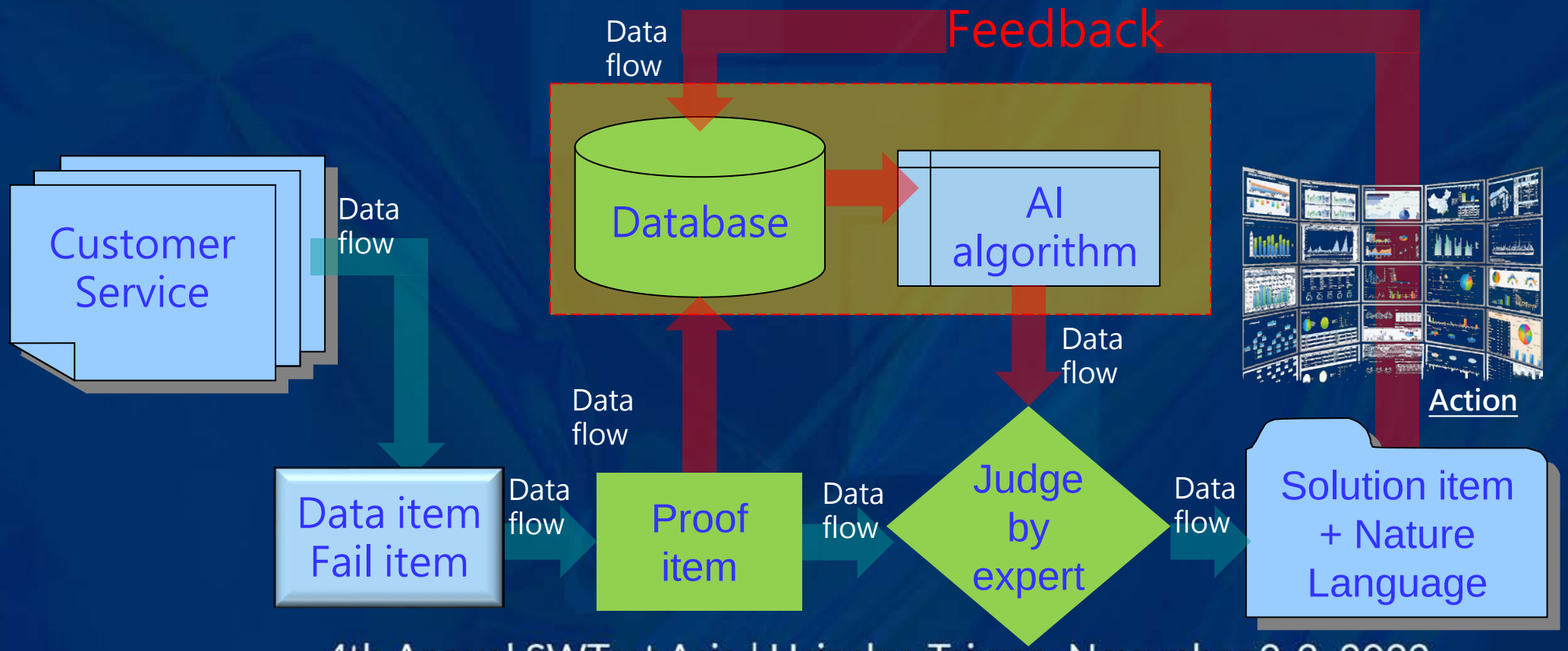
MPI Digital Transformation (MFG.com)

- **Data collected from the IT system is unstructured and only for domain expert judgment and operation purposes.**



MPI Digital Transformation (DATA.com)

- **Structured data is now used for constructing the MLBI algorithm to provide effective solutions in a few seconds.**



Multi-labeled Bayesian Inference (MLBI)

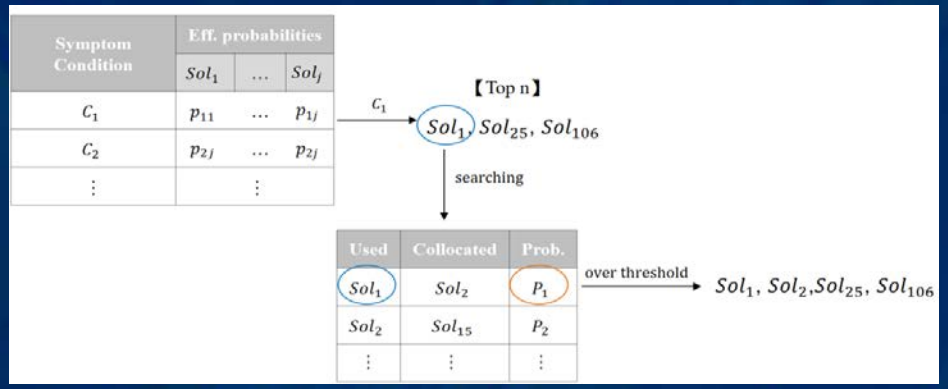
- **Calculating effective probabilities of maintenance actions under different abnormal conditions and collocated probabilities of two different maintenance actions**

Condition	Sol_1	Sol_2	…	Sol_j	Eff. Level
C_1	$u_{11} = 1$	u_{12}	…	u_{1j}	$r_1 = 1$ (effective)
C_2	$u_{21} = 0$	u_{22}	…	u_{2j}	$r_2 = 0.5$ (half effective)
C_{76}	u_{31}	u_{32}	…	u_{3j}	$r_2 = 0.01$ (non effective)
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
C_{xxx}	u_{N1}	u_{N2}	…	u_{Nj}	r_N

$$P(Sol_j|C_k) = \frac{P(Sol) \cdot P(C_k|Sol_j)}{P(C_k)}$$

$$P(Sol_a|Sol_b) = \frac{P(Sol_a) \cdot P(Sol_b|Sol_a)}{P(Sol_b)}$$

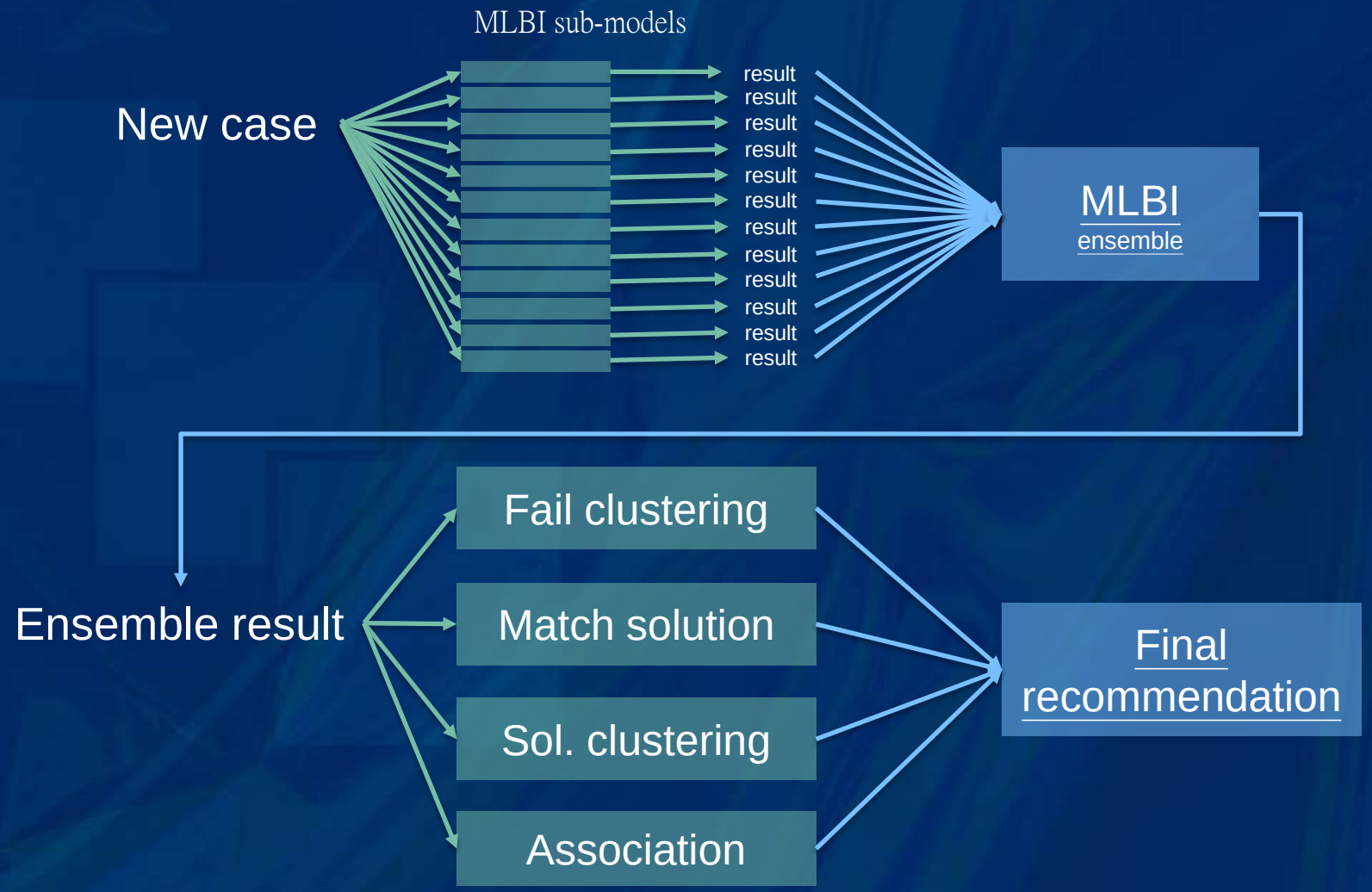
- **Predict the data that inputs certain symptom condition**
  1. suggests a certain number of maintenance actions with top n effective probabilities
  2. searching the suggested maintenance actions from (1) having collocated actions or not (over threshold)



Chien and Wu (2022)
Fu, Chien, and Tang (2022)

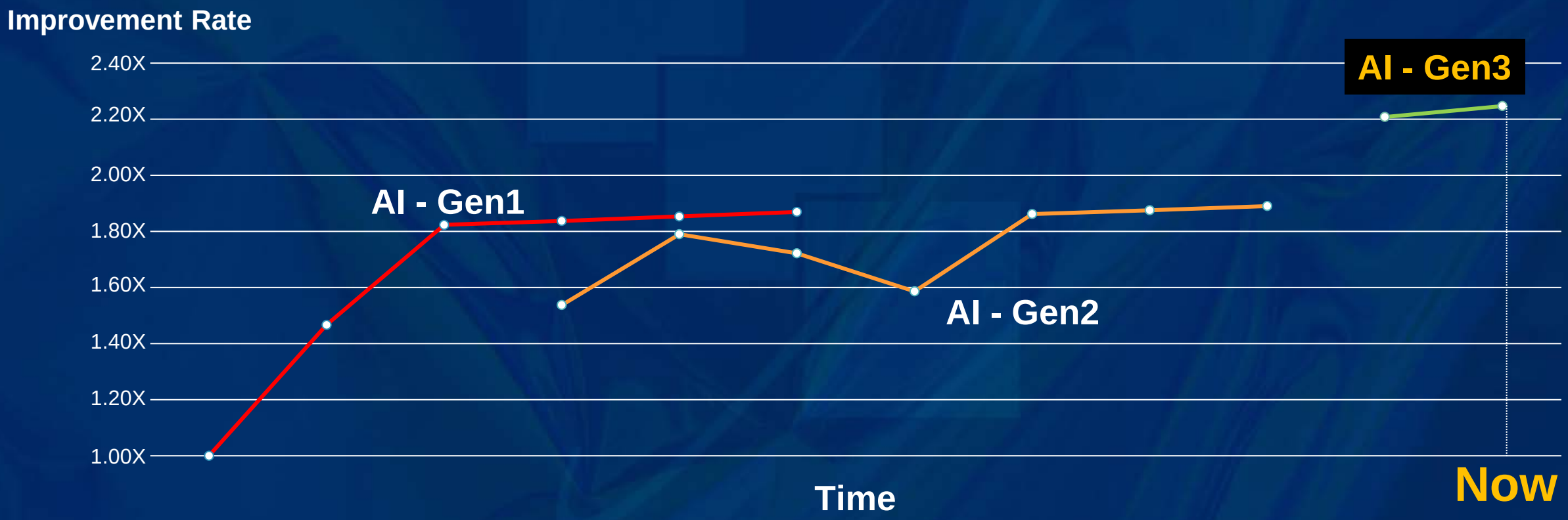
AI recommendation for Probe Card Maintenance

Sub-modules	Sub-models
A	M_I1
	M_I2
	M_I3
	M_I4
B	M_D1
	M_D2
	M_D3
	M_D4
C	M_F1
	M_F2
	M_F3
	M_F4
D	M_A1
	M_A2



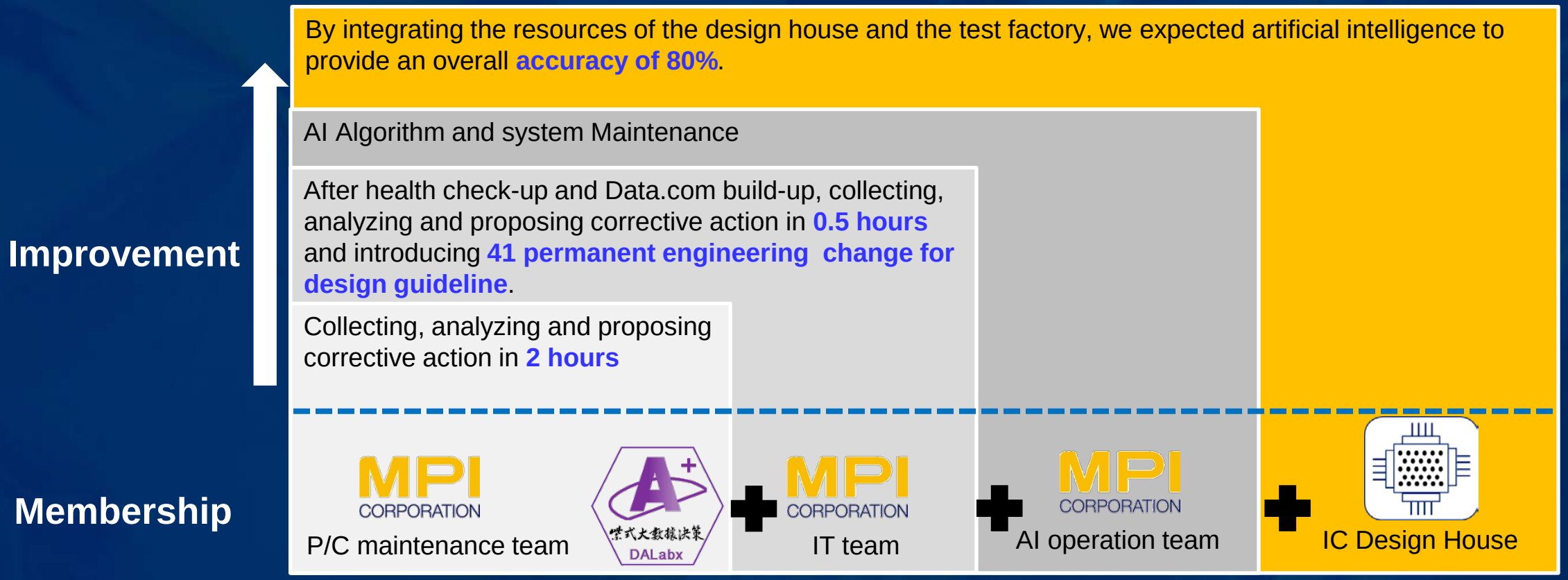
Accuracy Improvement Rate Ramping

- After data health check-up, accuracy improvement rate of AI-Gen1 model ramps up 1.87X.
- Accuracy improvement rate of AI-Gen3 ramps up from 1.87X to 2.25X because of good data accumulation and model structure improvement.



Summary

- **Our AI assistance system can propos 60% accuracy of corrective action in 0.5 hours.**
- **For higher overall accuracy, we expected artificial intelligence to provide an overall accuracy of 80% by integrating the resources of the design house and the test factory.**



Acknowledgment

- **Special Thanks to:**

  Kevin Yang、Pala Chen、Arthur Fan

  Eric Su 、Louis Chang 、 Nonie Lin

  Lily Liu 、Joyce Lee

  Alex Yang、Mark Sun、Samson Tang、Alex Wei

Questions

Reference

- Chien, CF., Wu, HJ. Integrated circuit probe card troubleshooting based on rough set theory for advanced quality control and an empirical study. J Intell Manuf (2022). https://doi.org/10.1007/s10845-022-02042-8

- Fu, W., Chien, CF. & Tang, L. Bayesian network for integrated circuit testing probe card fault diagnosis and troubleshooting to empower Industry 3.5 smart production and an empirical study. J Intell Manuf 33, 785–798 (2022). https://doi.org/10.1007/s10845-020-01680-0

- Lee, CY., Chien, CF. Pitfalls and protocols of data science in manufacturing practice. J Intell Manuf 33, 1189–1207 (2022). https://doi.org/10.1007/s10845-020-01711-w

Technical Program
SWTest Asia 2023

Friday, November 3, 2023

SWTEST ASIA

3D microprinted probes for testing at sub 20 µm pitch

EXADDON

捷鸃科技股份有限公司
Xsquare Technology Co., Ltd.

Premtek 技鼎股份有限公司

Koelmans[1], Lin[2], Wang[3], Huang[3], Hepp[1], Colangelo[1], Schürch[1]

[1]Exaddon, [2]Xsquare, [3]Premtek

4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

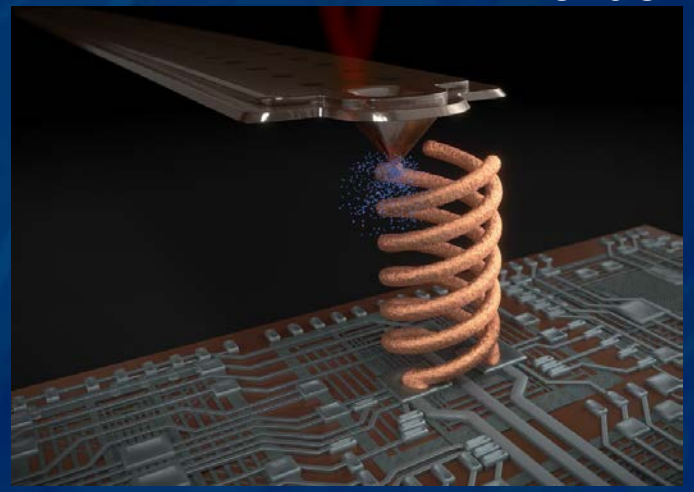
Outline

- Introduction: µ3D printing
- Objectives: µLED testing
- Methods: core-shell & manufacturing process
- Results: probe testing & simulation
- Discussion
- Conclusion
- Follow-up work

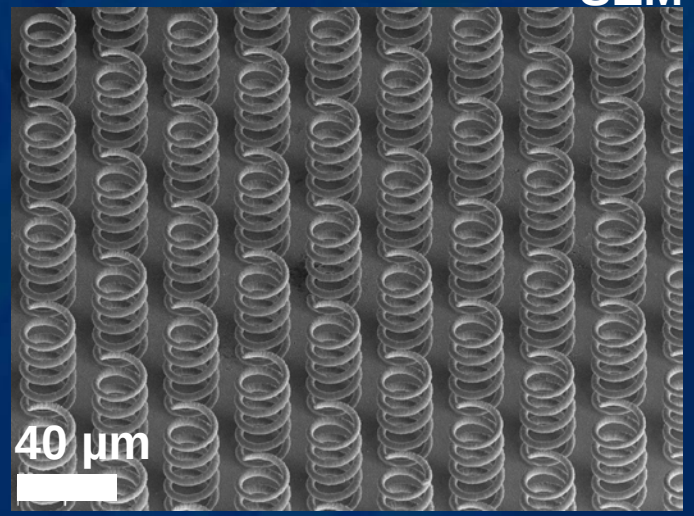
Introduction to µ3D printing

- 3D print with a 500-nm-wide nozzle
- Nanopositioning stages
- Micrometer-sized objects
- Template-free
- Local electrodeposition
- Print pure copper

render



SEM

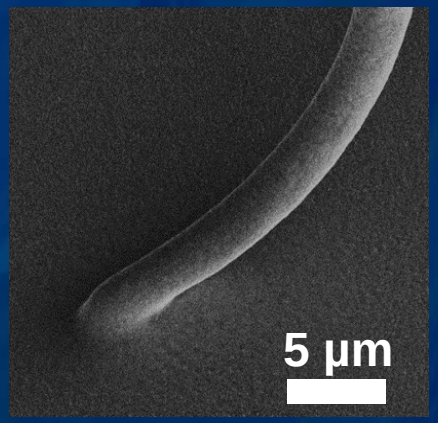


Motivation for µ3D printing in testing

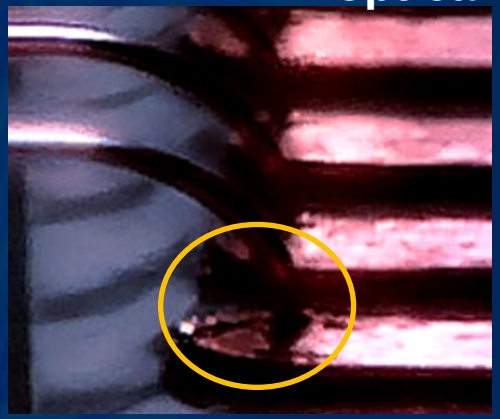
- **Unlocks a small probe pitch**
  - 3D design freedom
  - High material quality
- **Quick reconfiguration of probes**
  - Template-free process
  - Print directly on space transformer
- **Automated process**
  - Accurate dimensions probe printing
  - Seamless merging with contact trace

render

SEM



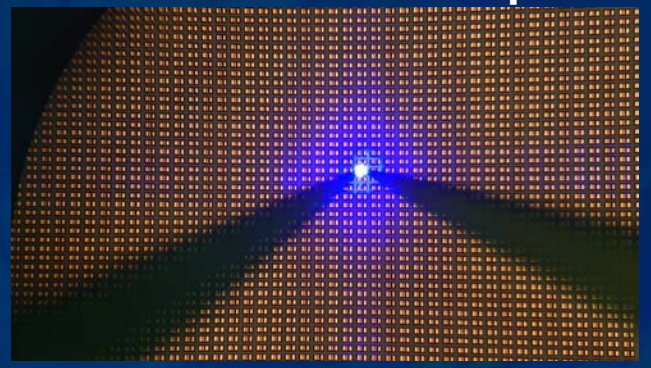
optical



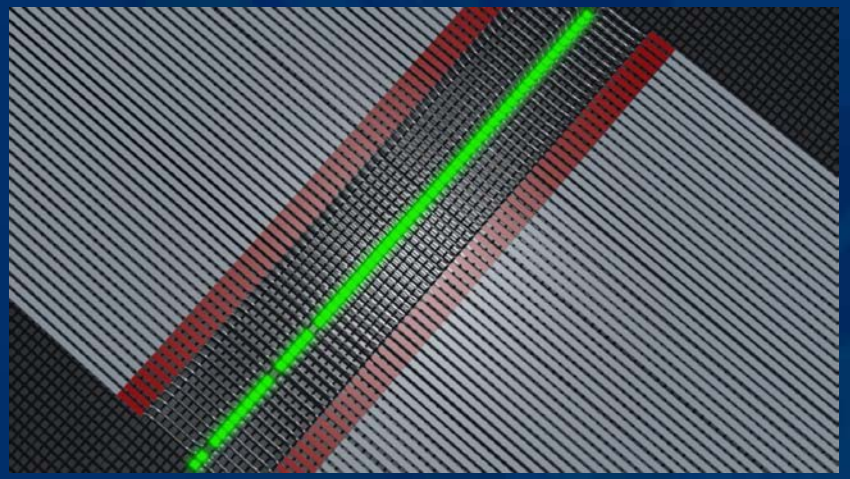
Initial case: µLED

- **µLED is an upcoming technology**
  - Wearables, smart devices, etc.
  - CAGR 82%*
- **Challenge: small-pitch probe arrays**
  - 18.5 µm / 35.5 µm (provisional)

optical



render



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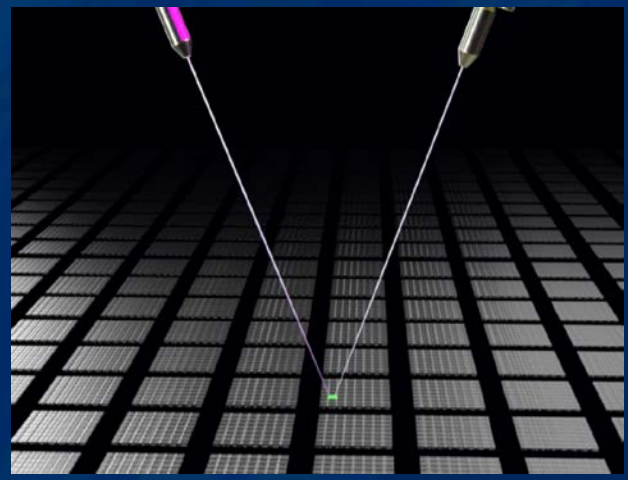
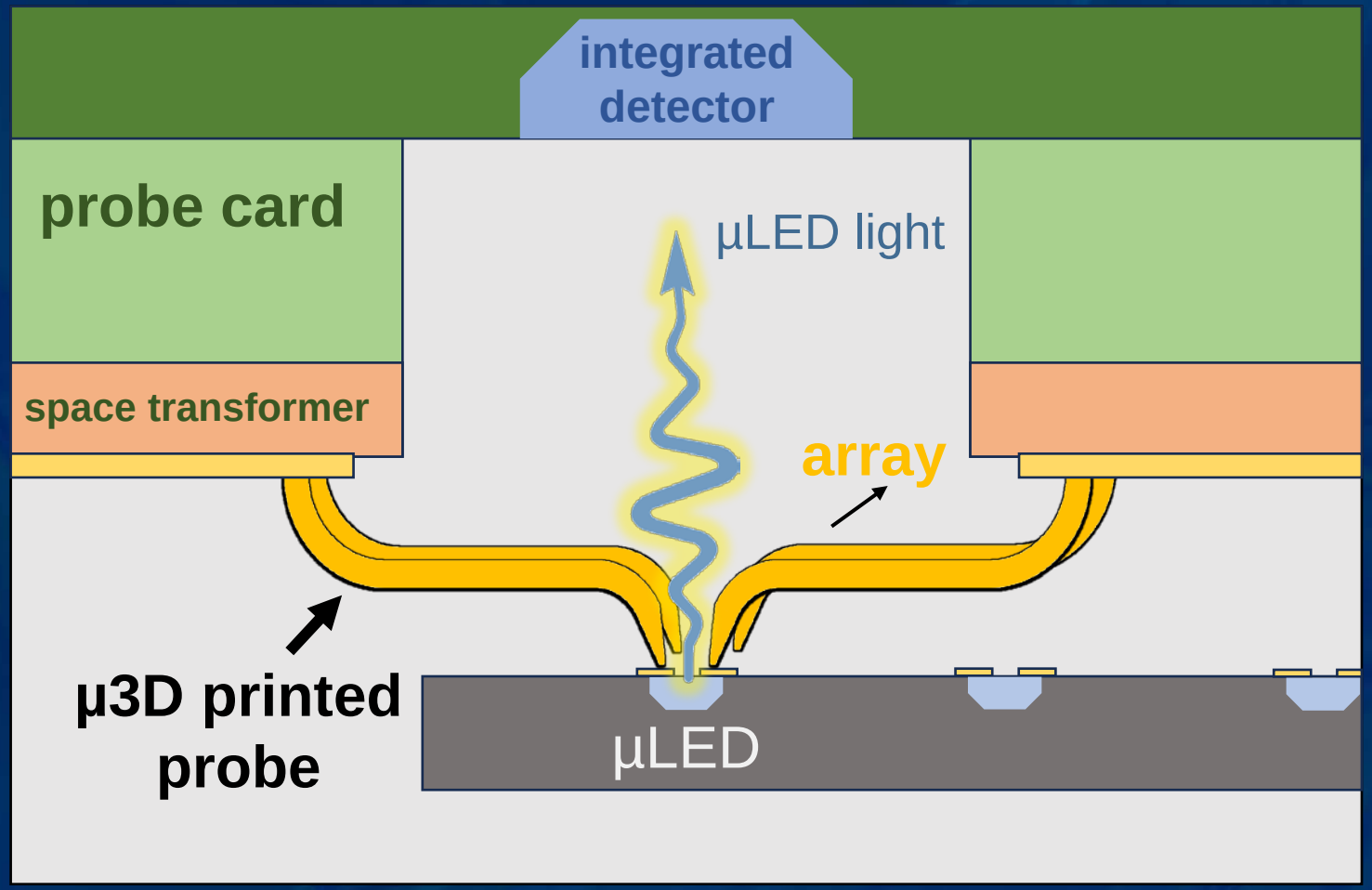


* Markets and Markets Research Private Ltd. Jan. 19, 2023

µLED testing principle

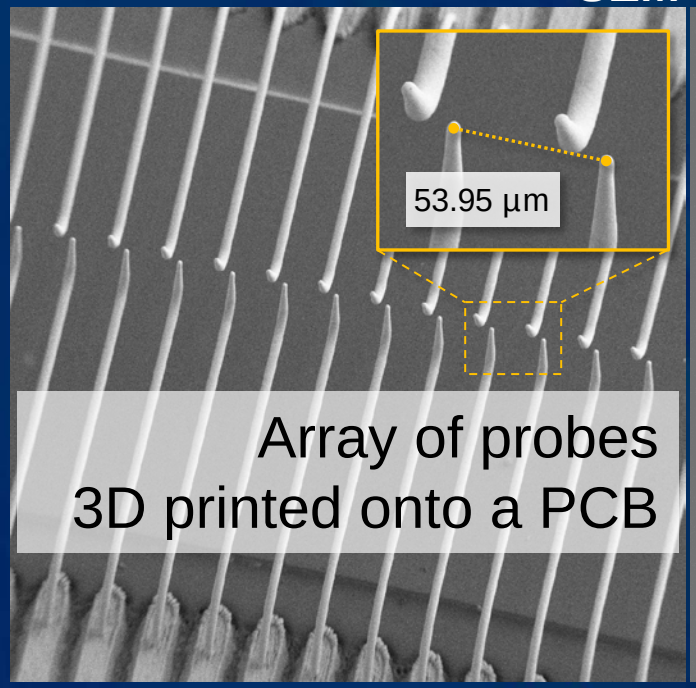


µ3D printing results

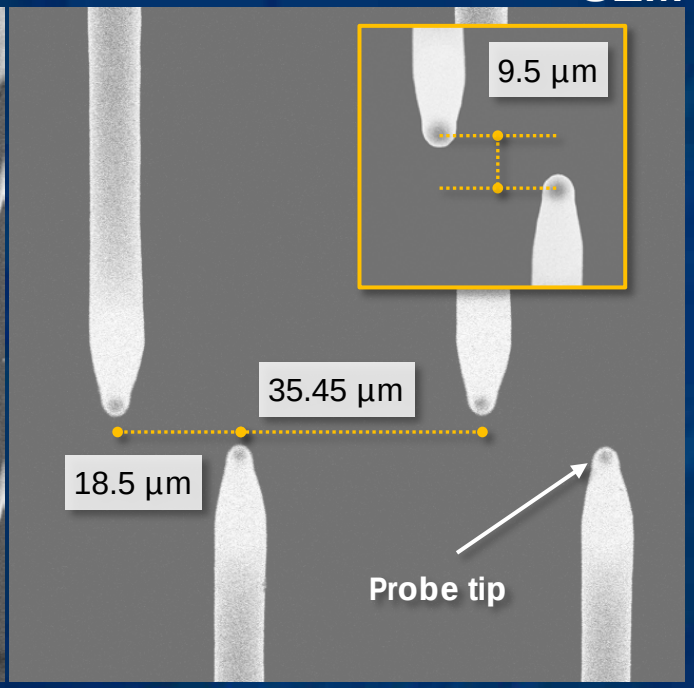
- Copper probes
- Up to 128 probes per array
- FR4 Printed Circuit Board (PCB)

optical

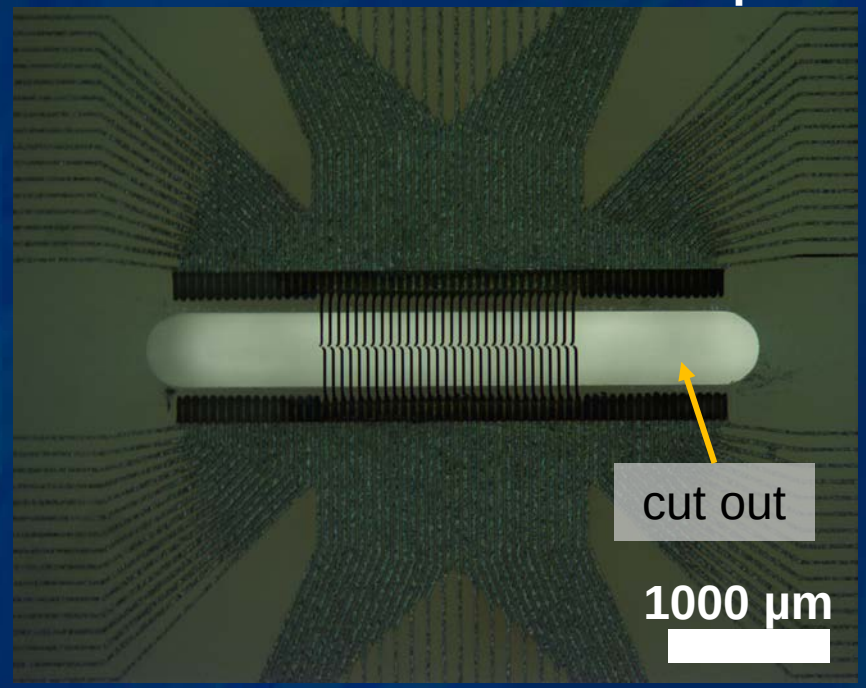
SEM



SEM

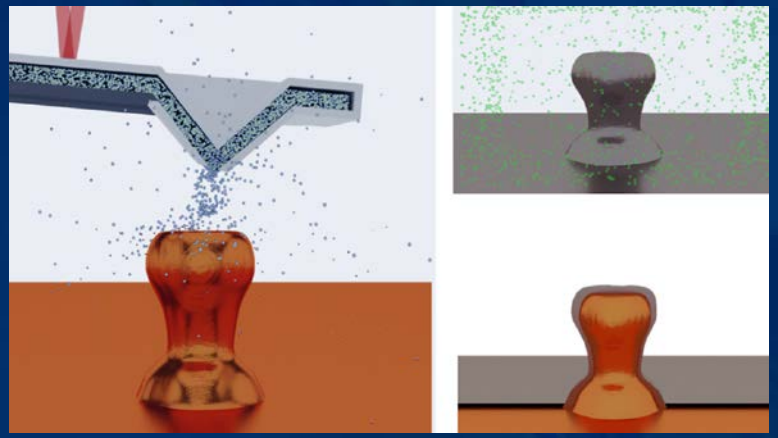


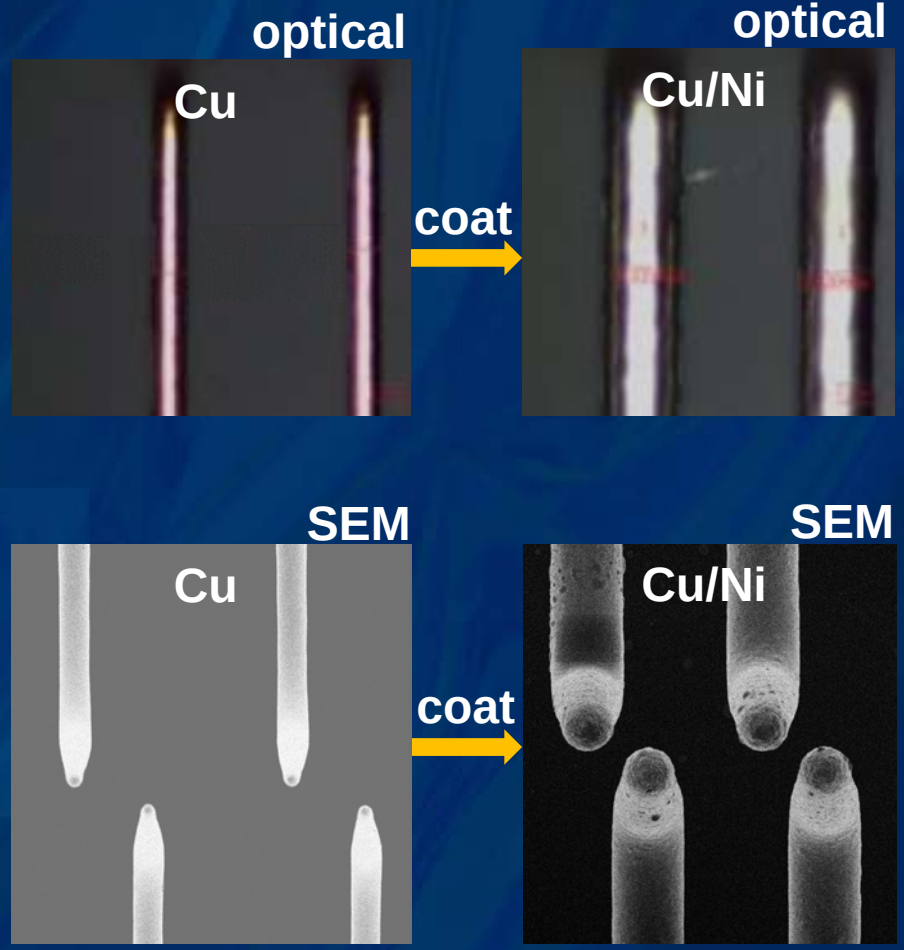
optical



Core - shell

- **Print copper**
  - Conductivity: 87% of bulk[1]
  - Yield strength: 0.4 to 1.0 GPa[2]
- **Coat with nickel for strength:[3]**

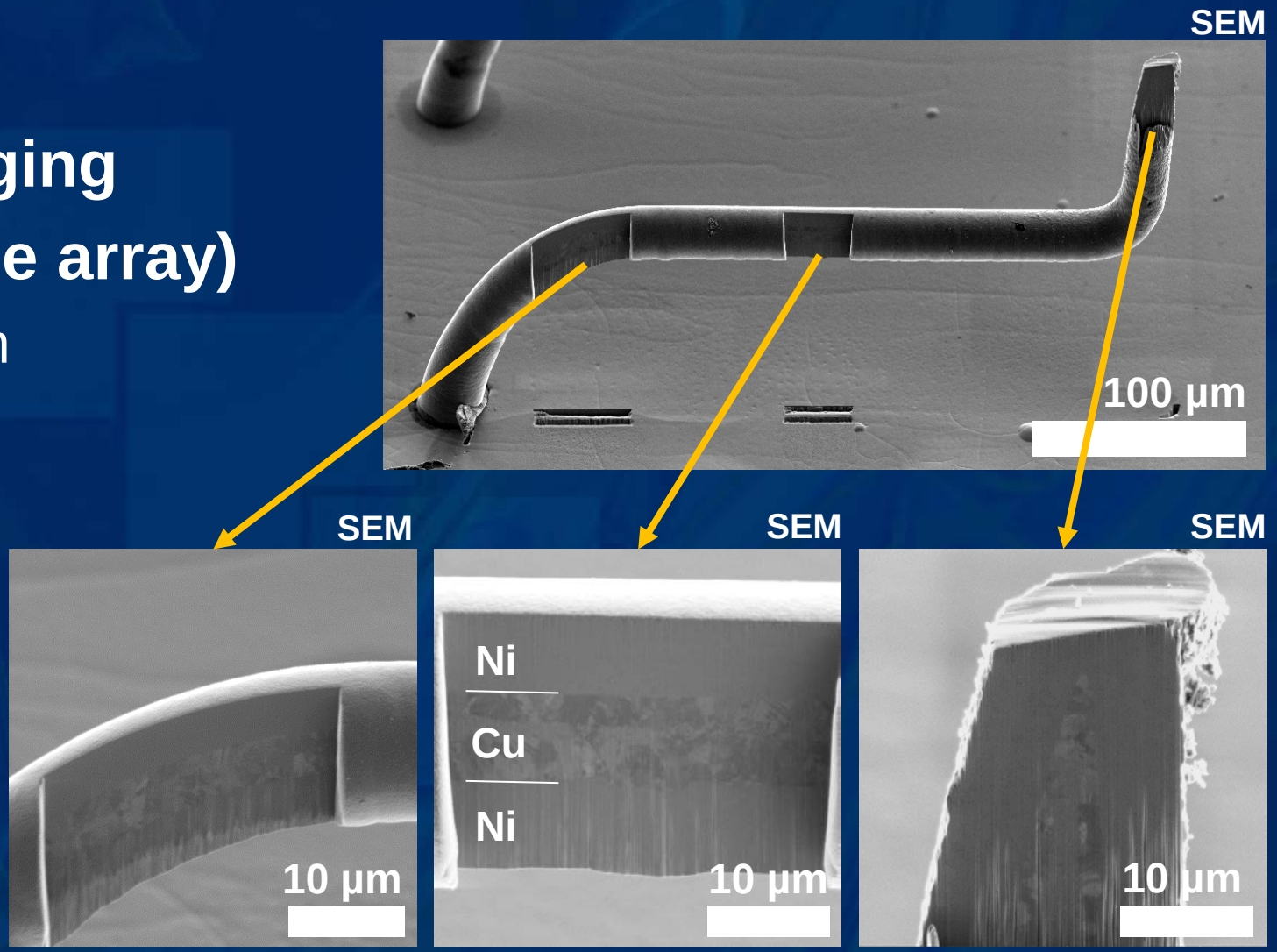




[1] Schürch *et al.* Materials & Design, 2023.
[2] Ramachandramoorthy *et al.* Appl. Mat. Today, 2022.
[3] Jain *et al.* Materials & Design, 2023

Quality inspection by Focused Ion Beam

- **Void-free materials**
- **Seamless layer merging**
- **Diameters (128-probe array)**
  - Cu: 8.6 ± 0.5 µm
  - Cu / Ni: 21.9 ± 1.5 µm



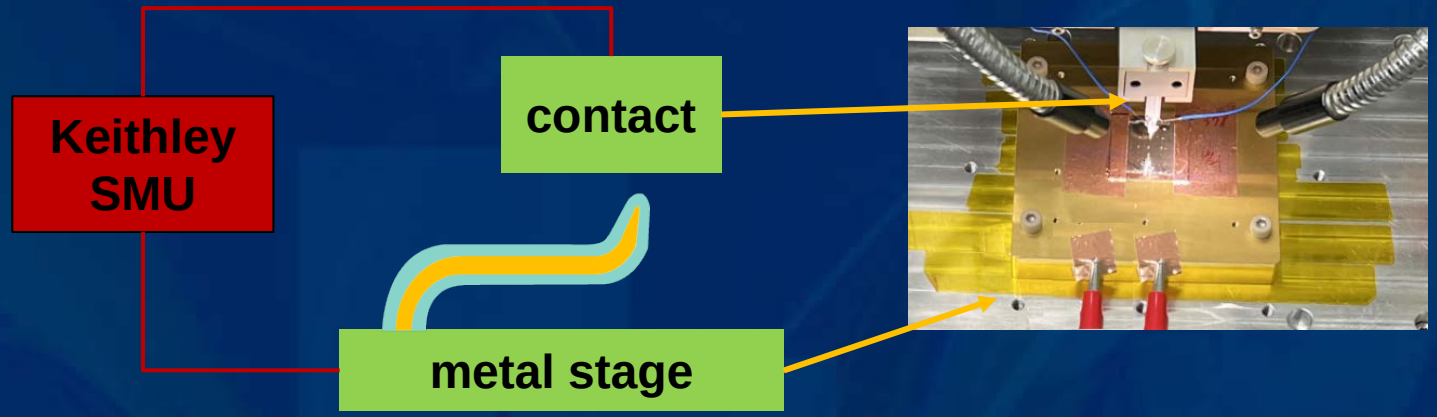
Manufacturing process

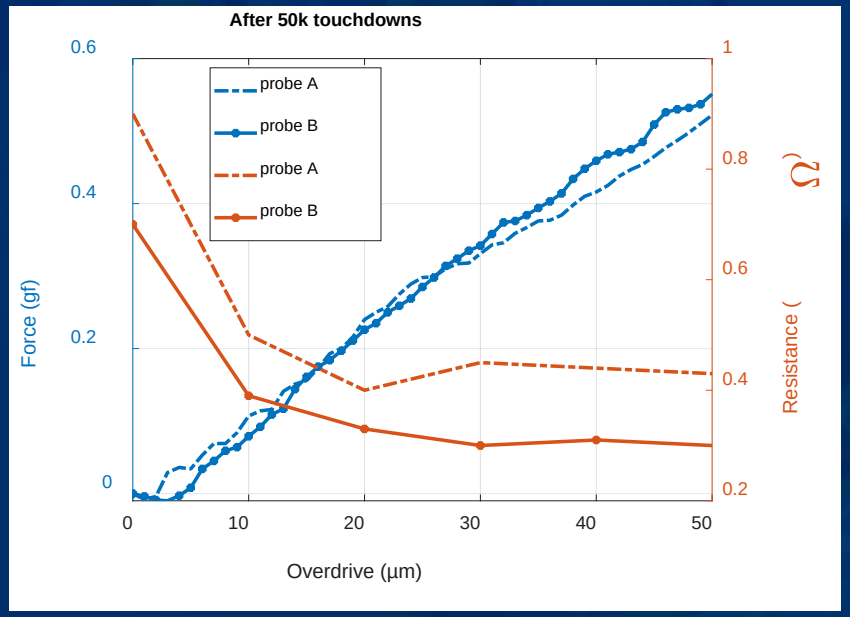
Step 1.
Make space transformer

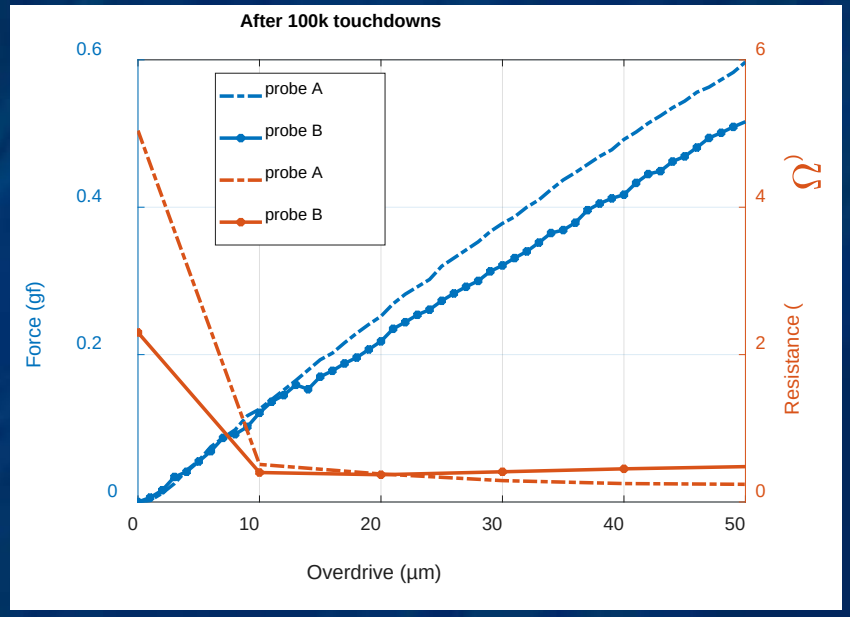
Step 2.
Local 3D printing

Step 3.
Global coating

Results: force and resistance

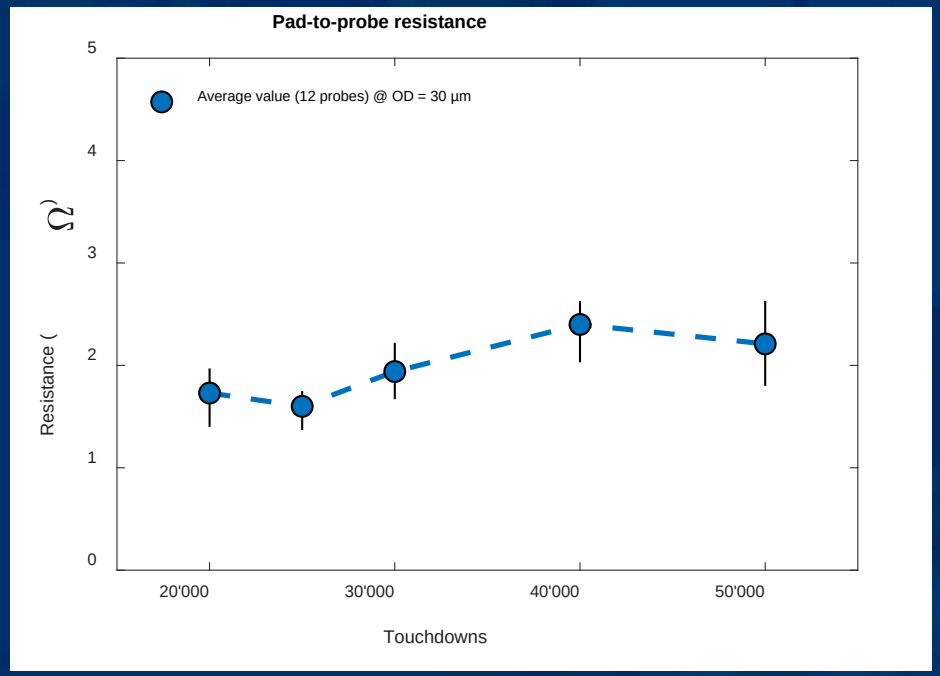


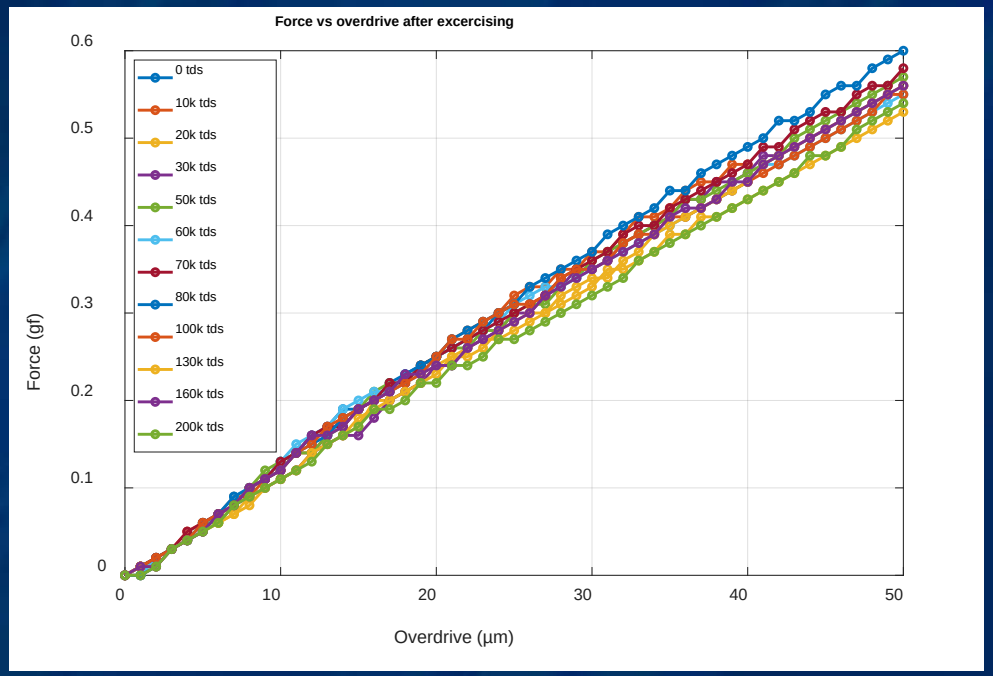




Longevity

- Tip wear <10 µm for 250k touchdowns
- Tests done on Au sputtered wafer
- Compatible with standard cleaning (ITS)





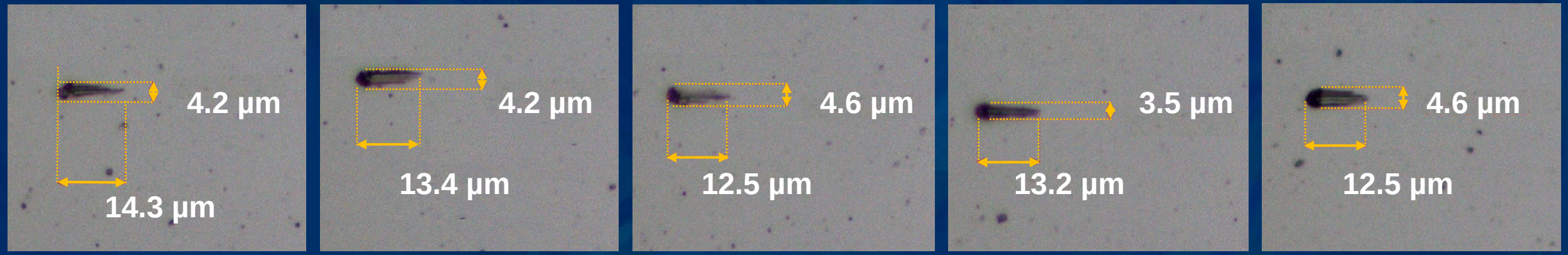
Scrub length

- **Scrub length at 50 µm overdrive (OD)**
  - Measured: 13.2 µm (mean)
  - Simulated: 13.5 µm

simulated by FEM

Overdrive (µm)	Scrub length (µm)
25	7.8
40	11.5
50	13.5

optical

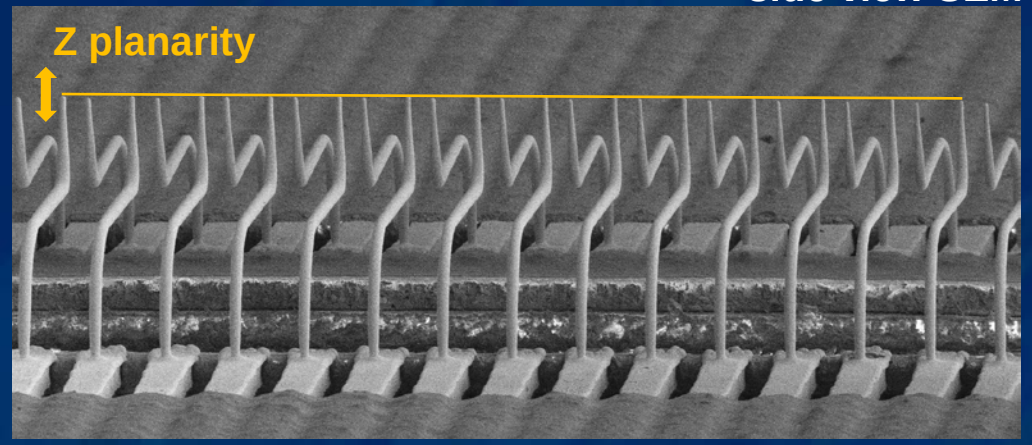


Z planarity and XY position in array

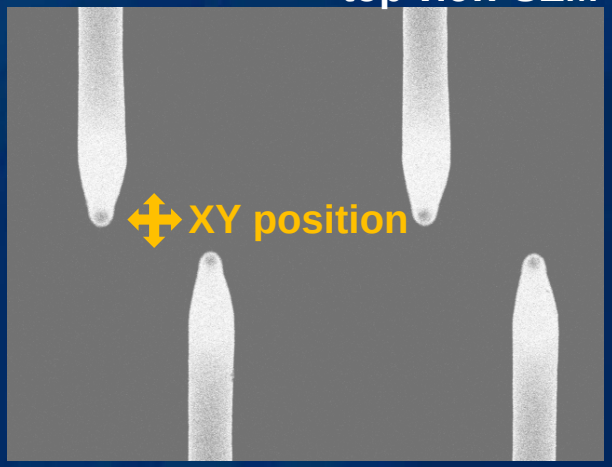
Analysis on 128-probe array:

- **Z-planarity: ± 1.4 µm**
  - Space transf.: ± 1.0 µm
  - Printing: ± 0.1 µm
  - Coating: ± 0.3 µm
- **XY position accuracy**
  - ΔX: < ± 1.5 µm
  - ΔY: < ± 1.5 µm

side view SEM



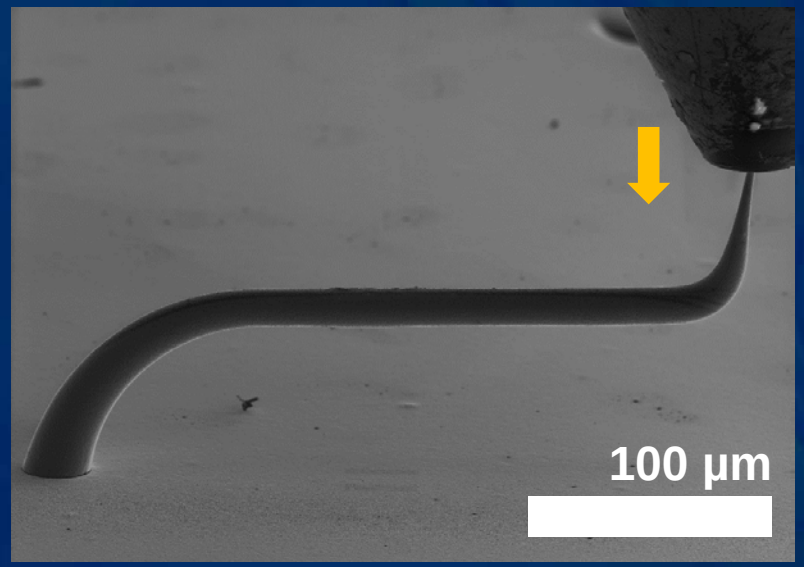
top view SEM

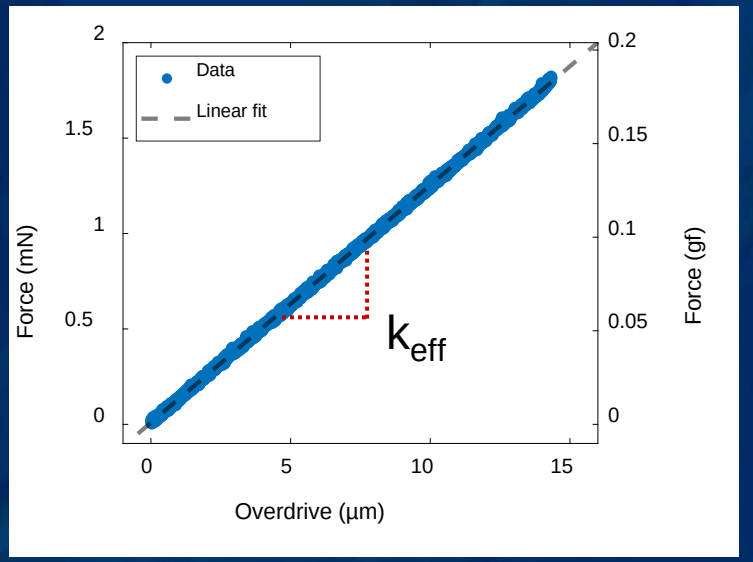


In situ mechanical testing

- **Measure the effective spring constant (k_{eff})**
- **Study probe deformation and failure**
- **Calibrate Finite Element Model simulations**

***in situ* SEM**





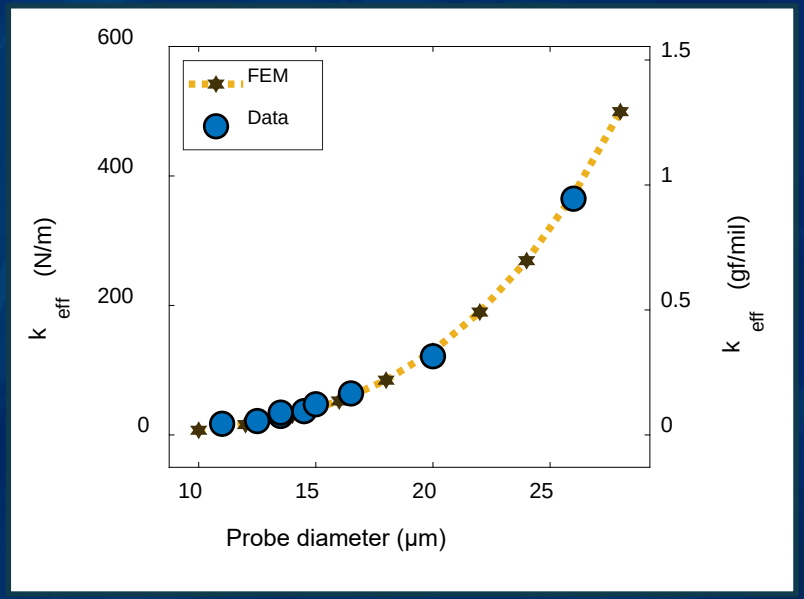
Cu / Ni with a 20-µm-diameter:
k_{eff} = 125 N/m (0.32 gf/mil)

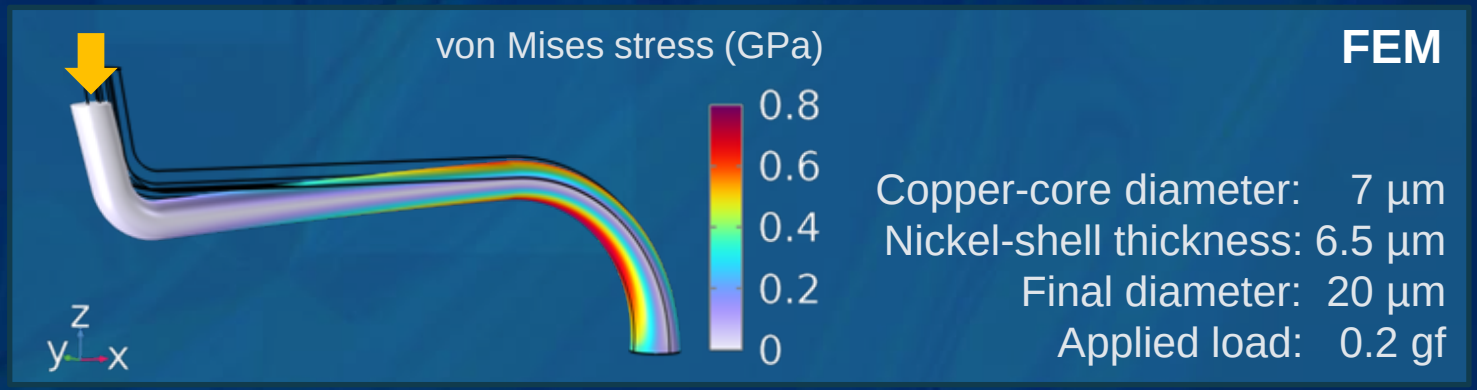
Due to Ni coating:
- k_{eff} is 40 times larger
- No plasticity for OD < 50 µm

Finite Element Method simulations

Calibrated model enables:

- **Designing complex geometries**
  - k_{eff}
  - Scrub length
  - Plasticity onset
- **Core-shell optimization**
  - Geometry
  - Material
  - Layer-stack





Discussion

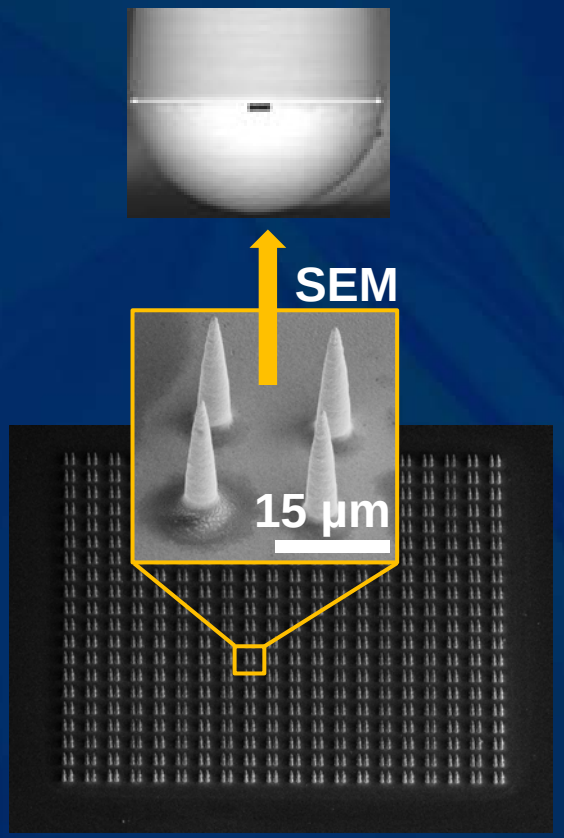
- **Array size to increase (128 to 256 probes)**
- **Optimize coating material and stack**
  - For longevity (creep, wear)
  - Larger temperature range
- **Optimize space transformer**
- **Probe station for fine-pitch**
  - ‘Chicken & egg’ situation?

Conclusions

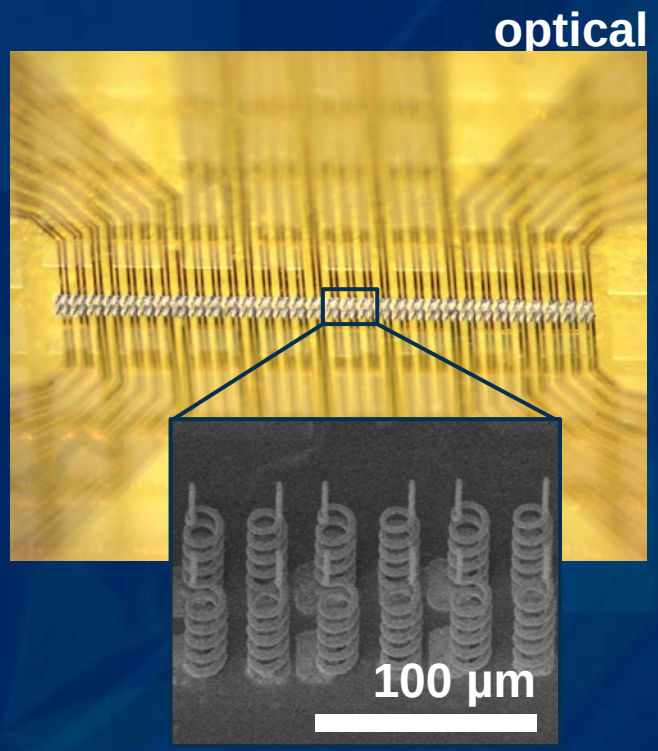
- **We introduced µ3D printing for testing**
  - Fine pitch, below 20 µm demonstrated
  - Quickly reconfigure without template changes
  - High-precision µ3D printing on variety of space transformers
- **Prototype ready for µLED testing**
- **Many other applications are possible**
  - Design process established with a Finite Element Model
  - Use the potential of µ3D printing to create even finer probes?

Follow-up work

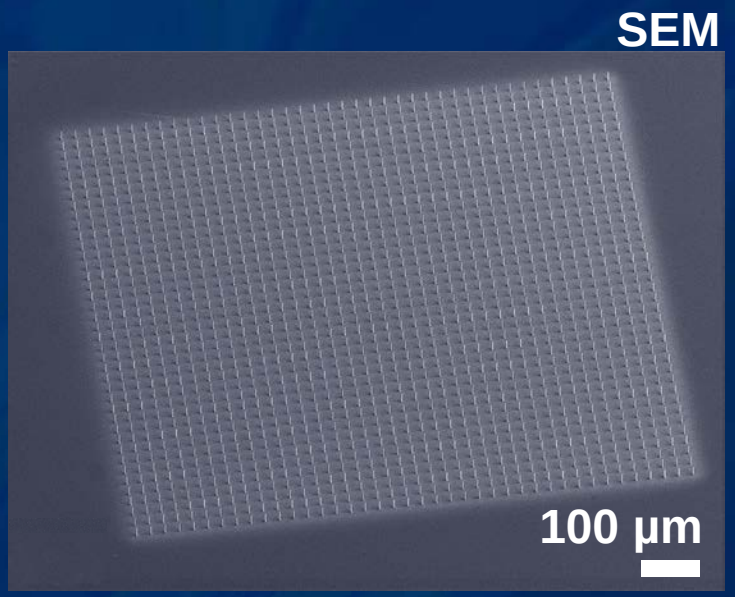
Micro bump contacting



µLED testing on polyimide membrane 18.5 µm / 35.5 µm pitch



40 x 40 array contact needles 25 µm pitch (2D)



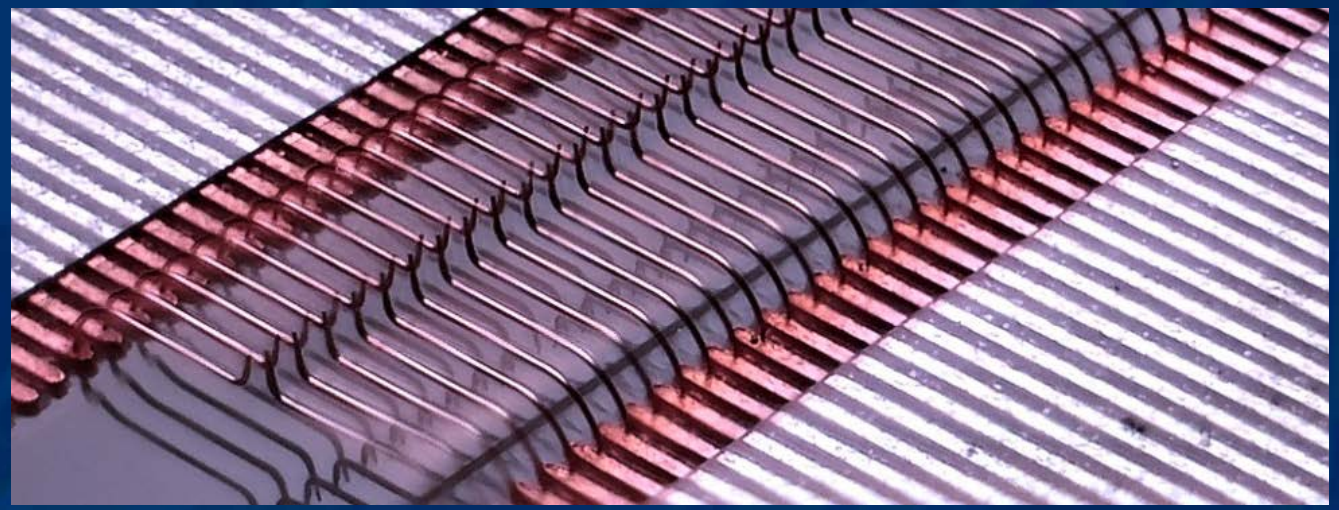
Thank you!

- Questions?
- Comments?

► Meet us at booth #215

► E-Mail: hello@exaddon.com

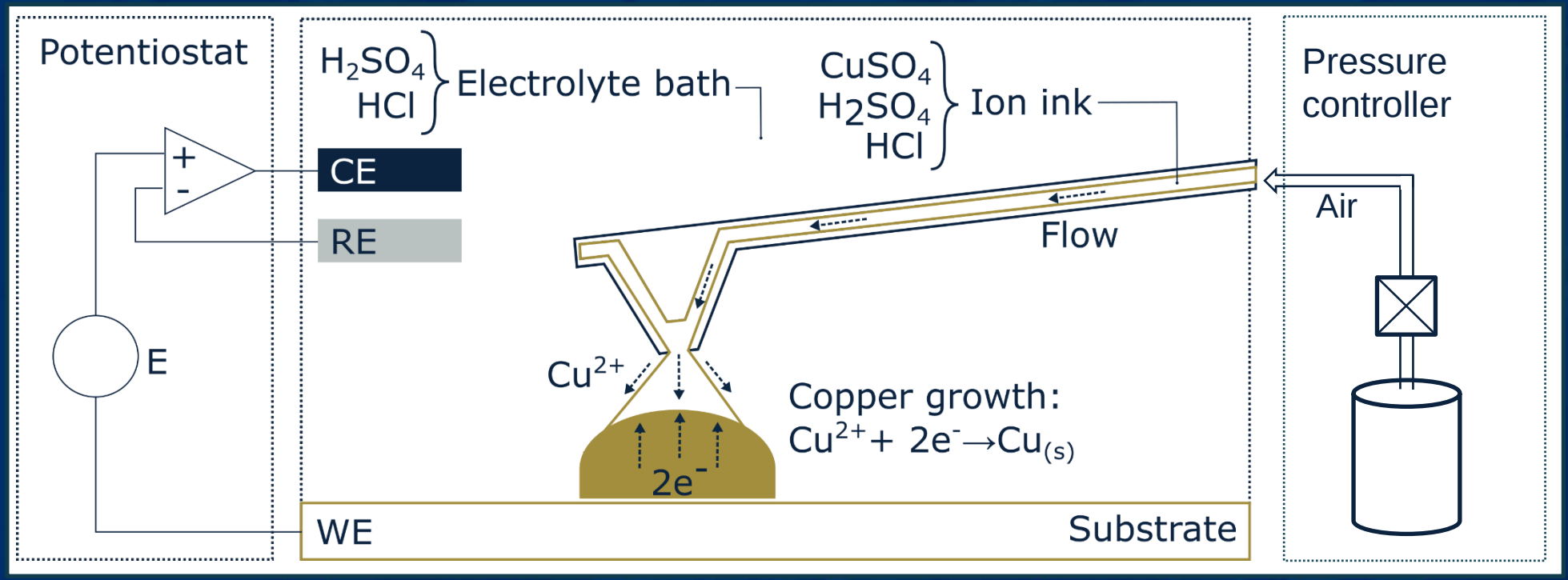
► Web: probes.exaddon.com



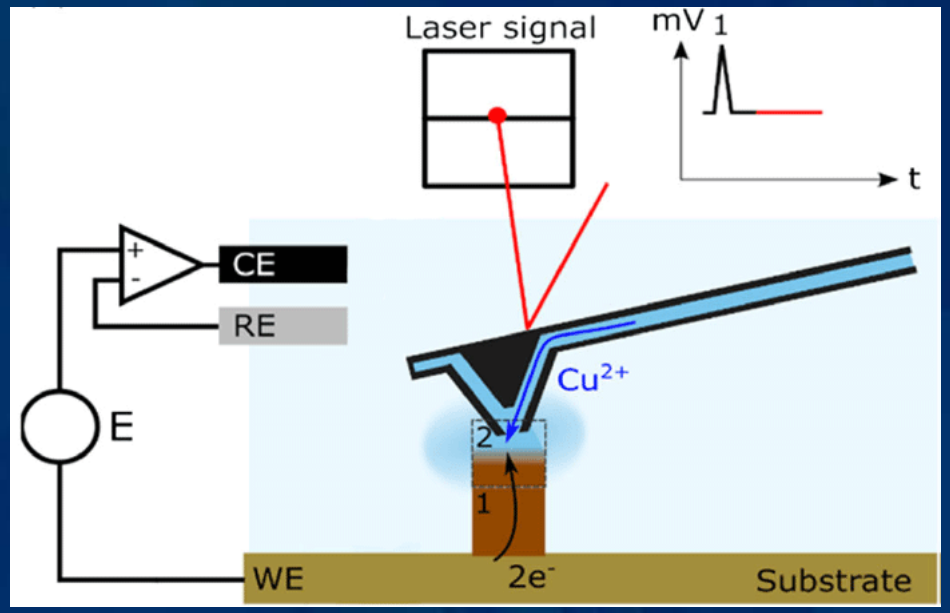
BACKUP SLIDES

μ3D printing process

- The metal printing is conducted within an electrochemical cell
- The ion ink is delivered via a microchannel inside the cantilever
- Pressure controller regulates the air pressure propelling the electrolyte
- A potentiostat regulates the voltages required for deposition

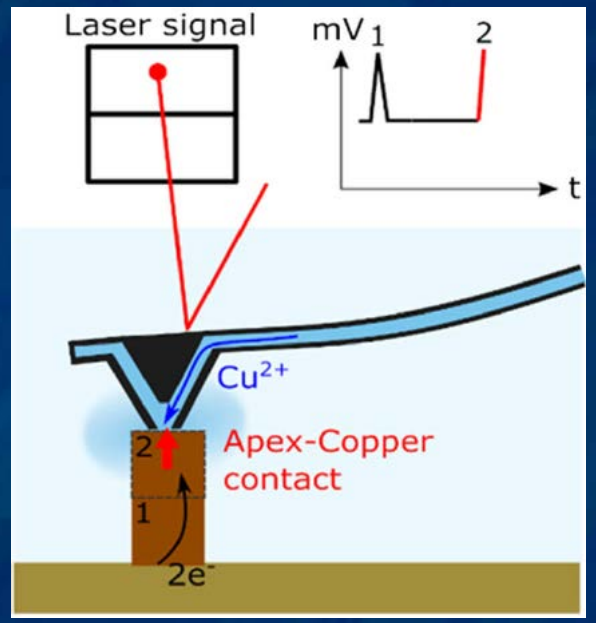


Voxel-based printing



Stationary phase:

- **Probe dispenses the metallic ions**
- **Metal growth occurs at the working electrode**
- **The metallic deposit reaches the tip aperture**



Ercolano *et al.*,
Adv. Eng. Mater. 2019

Dynamic phase:

- **When deposit reaches tip → trigger**
- **A voxel is completed, retract tip**
- **Height of the voxel is now known**

Space transformer materials

- PCB FR
- µPCB
- Silicon
- Membrane (polyimide)

Silicon Photonic On-Wafer Test

S.L Tan, W.L Sio
CompoundTek
C.L Lou, B.B Lim
STAr Technologies, Inc.

4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

Overview

- **About CompoundTek and STAr Technologies**
- **Need for Silicon Photonics (SiPh) Wafer Test**
- **Silicon Photonics Wafer Test Solution**
  - Prober Layout and DUT Layout
  - Types of Optical Coupling
  - GRnR Results
  - Typical SiPh Test Items
  - Video Demostration
- **Summary**

Our Commitment

Deliver leading edge Open-Source silicon photonics platform

Accelerate time-to-market

Founded by Industry Experts.

"Virtual fab business model" with proprietary technology

- **2017** Operations began with patented manufacturing technology running in our fab partner
- **> 20 Commercial Customers** in 9 different countries are served by our cutting-edge SiPh foundry capabilities
- **>25 International** leading Research Institutes/ Universities are a part of our global SiPh ecosystem
- **70 provisional filing/know-how in FY20** forms our large IP bank, capabilities are heavily promoted via media/press (22 releases, FY20) for differentiated branding
- **1st globally embarking on a 8" & 12" agnostic SiPh** commercial testing hub

News.

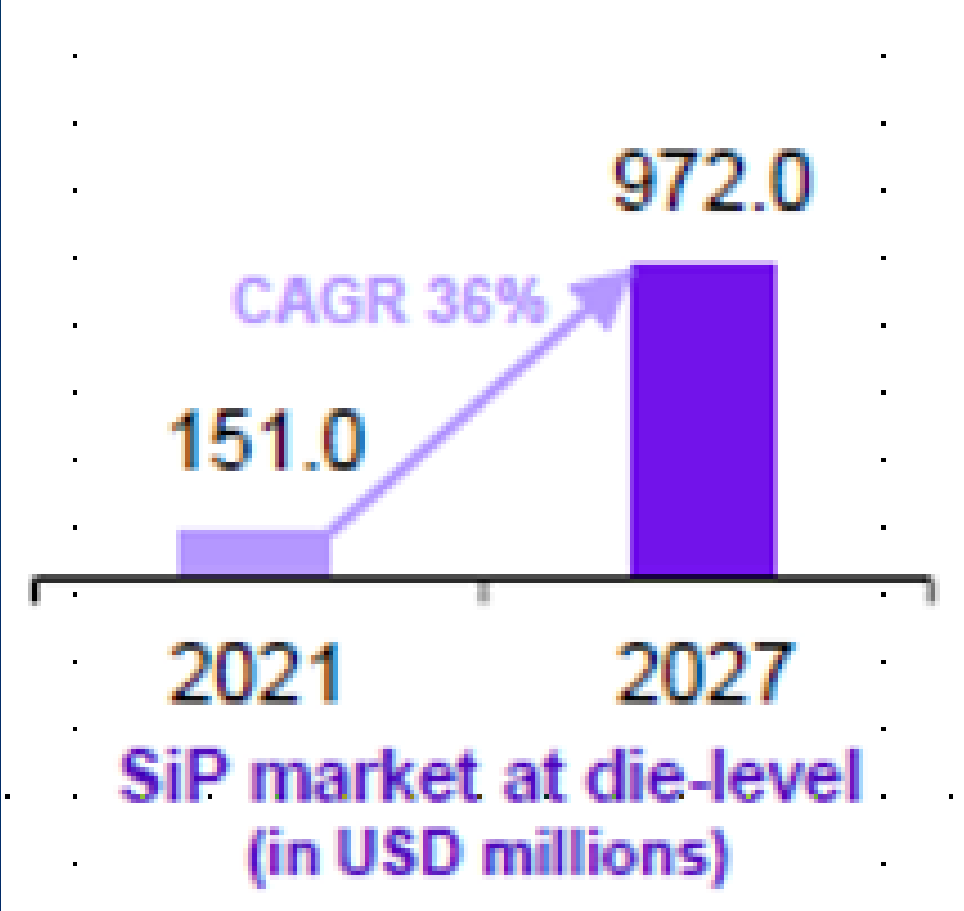
Asia's 1st SiPh Foundry Agnostic Wafer Test Hub.

Testing Centre of Excellence Operation

- Backed by CompoundTek's strategic partnerships with leading industry test equipment players (prober and instruments)
- 8" and 12" & O and C band ready
- Ideal for EO components, 400Gbit/s and higher
- State-Of-The-Art equipment (up to 67GHz LCA for e.g)
- Powered by in-House proprietary proven test executives
- Patented software coding with AI, big data analytic, up to 40% throughput improvement vs market benchmark
- Managed by team with proven track record

STAr Technologies Overview

SiPh Market Size



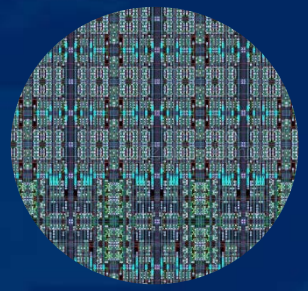
- **Increase predominantly driven by**
  - Data Communication such as transceivers,
  - Photonics Processing Applications
  - Smart Sensors such as LiDar
  - Consumer health applications, such as silicon photonics based biosensors in wearables

Source: (1) McKinsey: Imperatives for photonics companies in the next wave of growth (Jan 23)
(2) Yole: Silicon Photonics: To SOI and beyond (Aug 22); Yole: Silicon Photonics 2021 Market Technology report

SiPh Wafer Test Challenges

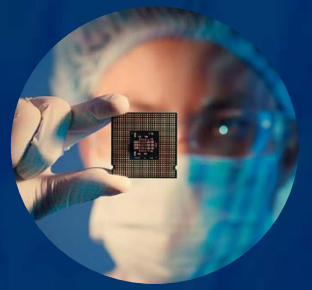
High technical complexity required

- Optics Testing unknown to existing OSATs
- Complex hardware/prober design for both Optical & Electrical test.
- High precision alignment of <1um a must, for optical light coupling in/out of Device-under-Test (DUT).
- No cost effective wafer test with edge coupling solution in market
  - Test done at vertical light coupling but actual application is edge coupling, mismatch between test & actual application can limit test coverage



Special layout rules and guidelines

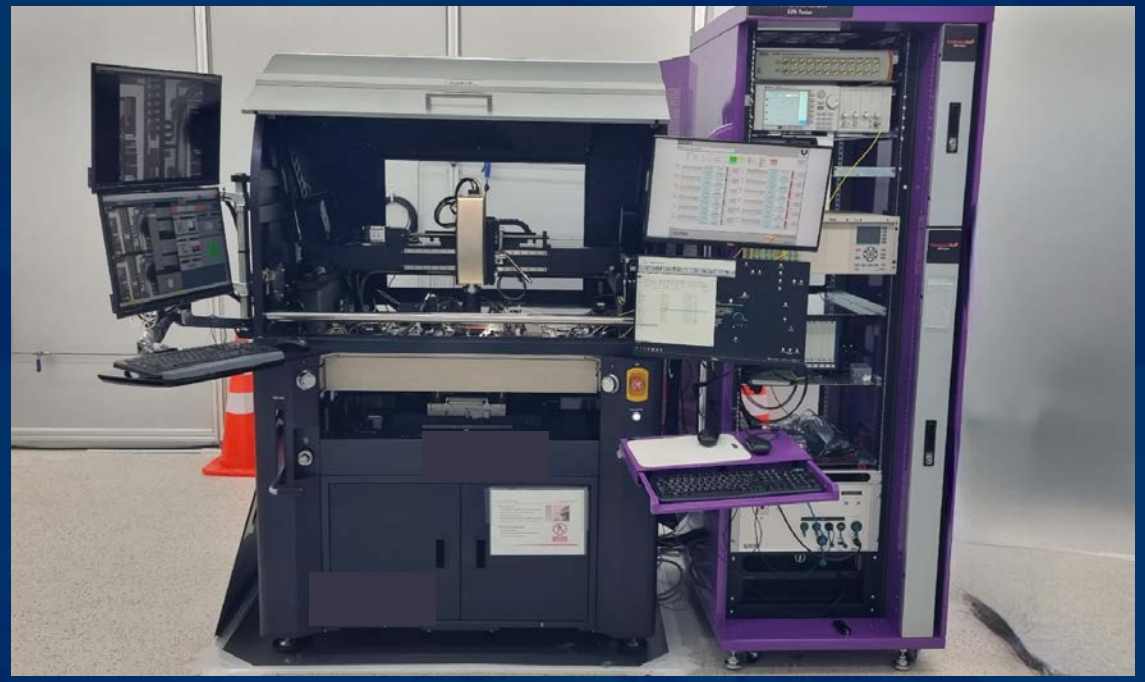
- Recommend for new products to ensure Design for Testability
- Enforced during design phase. Designer to layout optical grating and electrical pads according to guidelines to ensure testability



Long test time, high test costs

- Long alignment time needed for optical coupling. Fast and repeatable optical coupling needed to ensure cost effective production testing

SiPh Wafer Test Solution



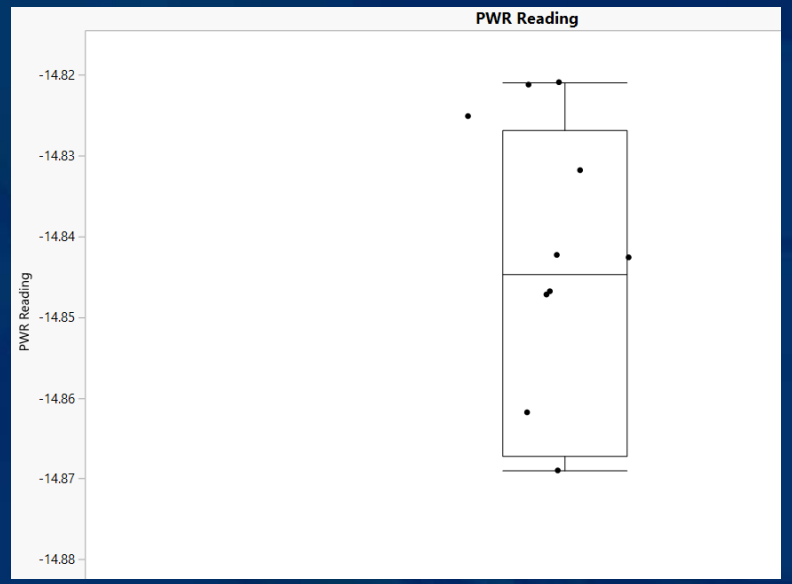
- 8”/12” wafer compatible.
- Vertical Coupling and Edge Coupling fiber array.
  - CompoundTek Edge Coupling fiber array design coupled with STAr’s Patented Edge Coupling Alignment SiPh Solution
- Full O-band, C-Band and L-Band.
- Optical/electrical testing/RF Testing
- Suitable for mass volume production & cost-effective testing.

STAr SPT System Overview

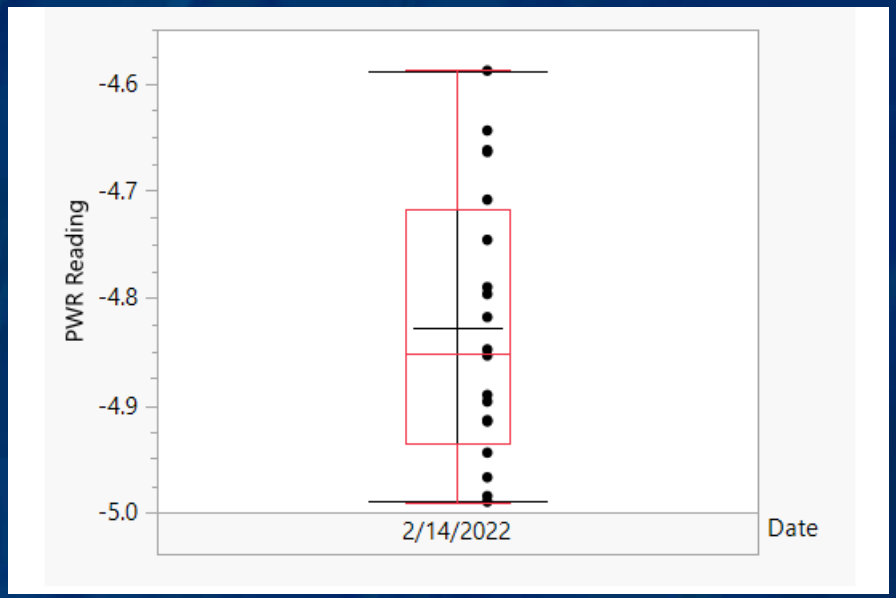
- **Objectives**
  - To provide a cost effective semi-automated or full automation wafer-level test system for characterization and acceptance tests of silicon-photonics devices
- **System Capabilities**
  - Characterization & Technology Development
  - WAT/E-tests/Inline PCM
    - All E-tests parameters including process monitor control, device parameter test, statistical process control, etc.
    - Optical components for process control and monitor

Optical Coupling GRnR Results

Vertical Coupling GR&R



Edge Coupling GR&R

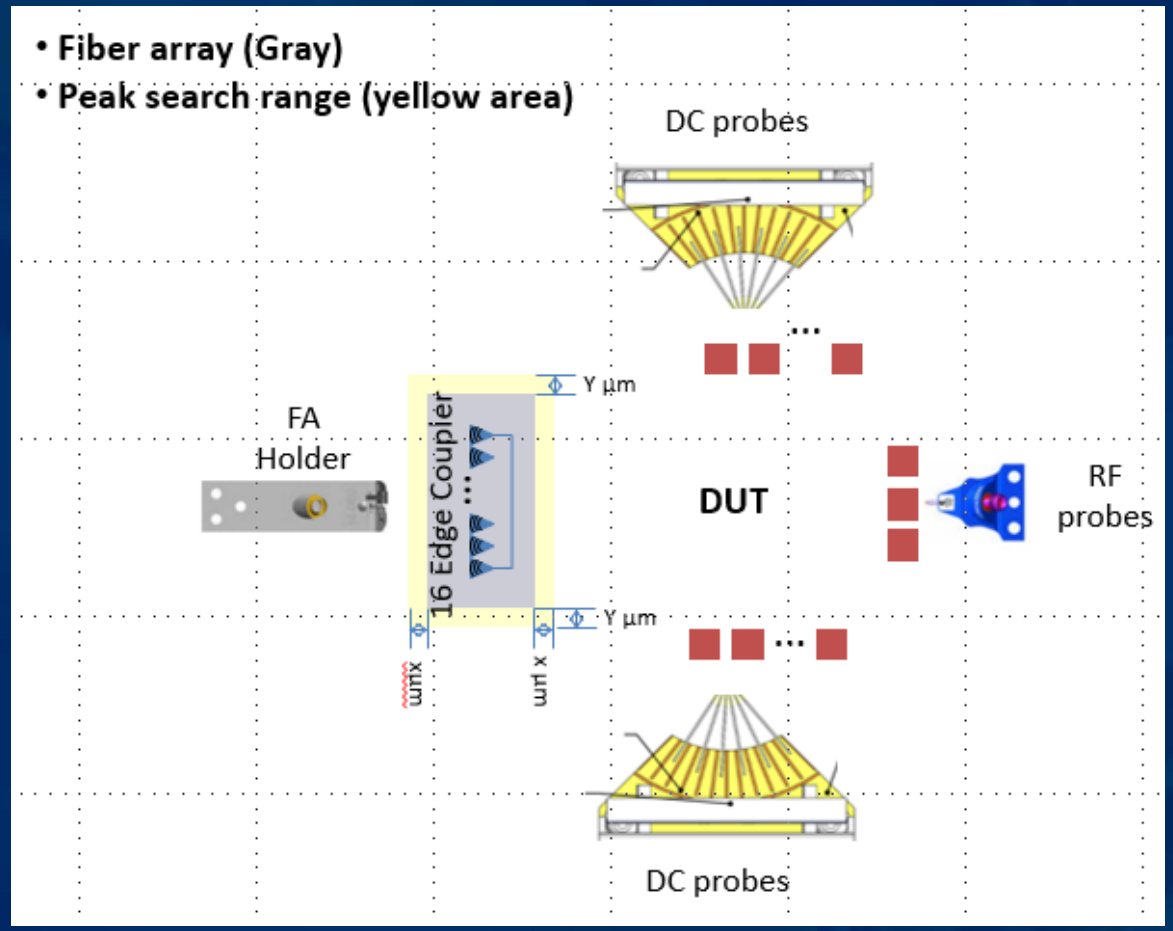


Vertical Coupling GRnR: 0.06 dBm

Edge Coupling GRnR: 0.17 dBm

Worse GRnR at edge coupling due to more stringent precision needed for edge coupling compared to vertical coupling

Test Configuration

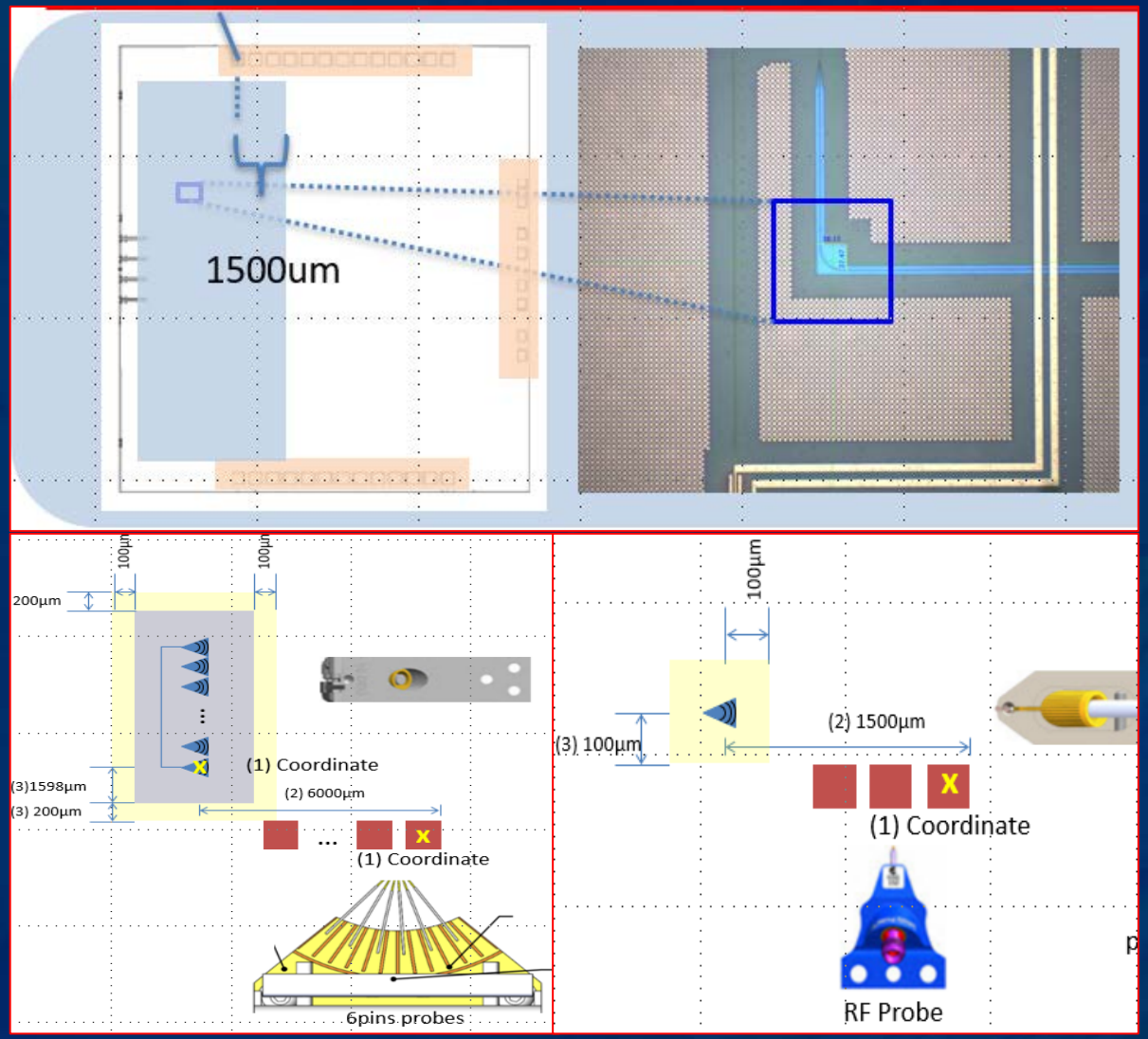


Types of IO	Orientation
Optical Edge Couplers	West
Electrical Pads (DC/RF)	North/South/ East

Flexible orientation possible by rotating the wafer

- **O-band and C-band.**
- **Trench Width: ≥ 80 µm (zero change of existing layout).**
- **Trench Depth: : ≥ 40 µm**
- **Number of Edge Couplers: 16.**
  - **Customization of edge fiber array possible for edge couplers ≥ 16.**
- **Edge Coupler Pitch: 127/250 µm.**
  - **Edge Couplers on same side of die.**
- **Electrical Pad (DC and RF) size: 80 x 80 µm (recommended)**
  - **Pitch 100 µm.**
  - **RF Pads configuration GSG, GSGSG.**

Design Rule Layout



- **CompoundTek wafer test design rule layout for both vertical and edge coupling available to customers during chip design to ensure wafer can be tested after Fab out**
  - Consists of keep out area for pads, edge couplers/vertical gratings
  - Dimensions and design of deep trench

Typical SiPh Wafer Test Items

Electrical Test

- Photodiode Dark Current
- Optical Modulator terminator, VOA, heater etc active structure IV (resistance) measurement.

Optical Test

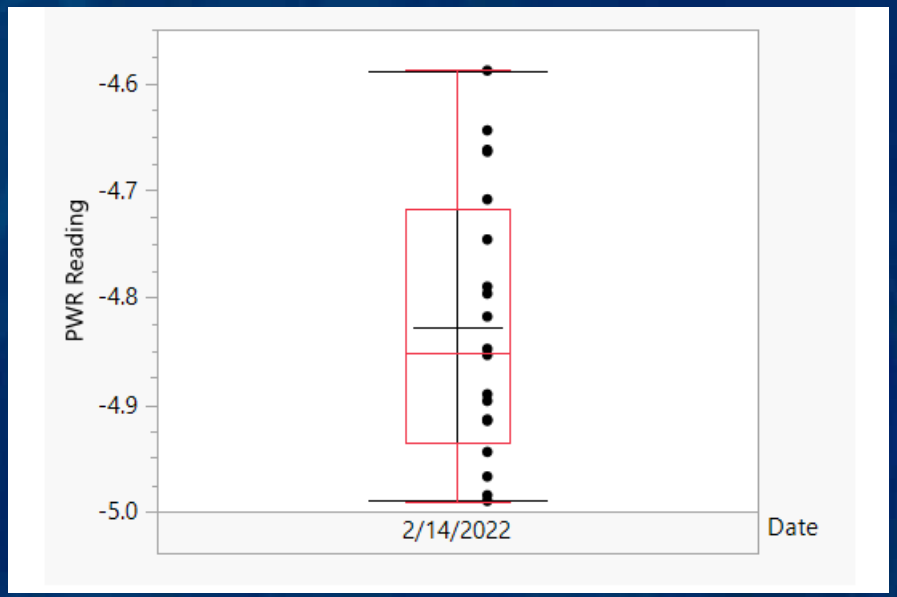
- Passive device parameter including IL, PDL, WDL etc
- Waveguide Propagation Loss
- Tap Coupler Coupling Strength

Opto-Electrical Test

- Photodiode Responsivity
- Photodiode Bandwidth
- Modulator Extinction Ratio
- Modulator Bandwidth

SiPh Wafer Optical Edge Coupling

On-wafer fiber array edge coupling on CompoundTek's Gen#1 suspended edge coupler



Edge Coupling Performance

Trench Top Width	> 80µm (No change in layout)
Coupling Loss	~4.8 dB/facet (Depending on MFD mismatch)
Std Deviation	0.17dB

Integration with LCA for Bandwidth Measurement

Capable to perform Edge Coupling + Optical Bandwidth Measurements

No significant bandwidth difference as compared to customer diced chip measurement

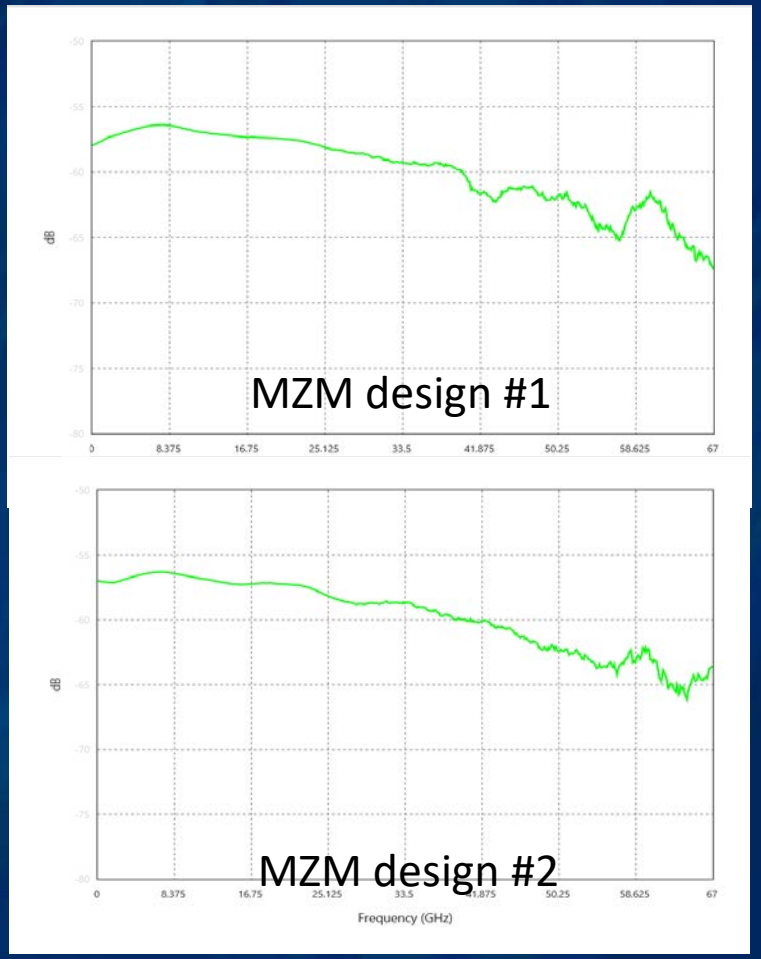
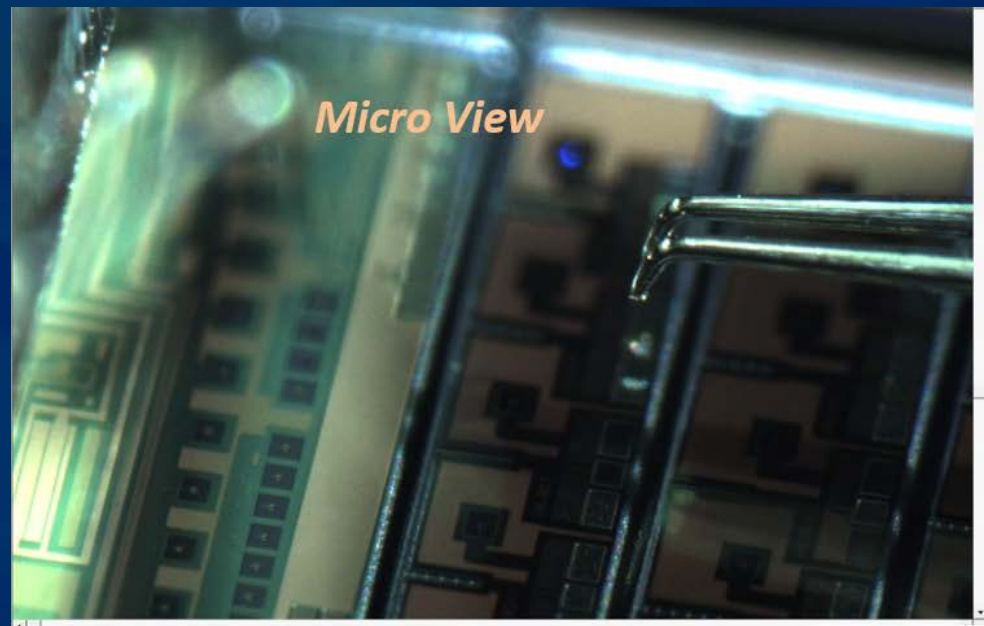
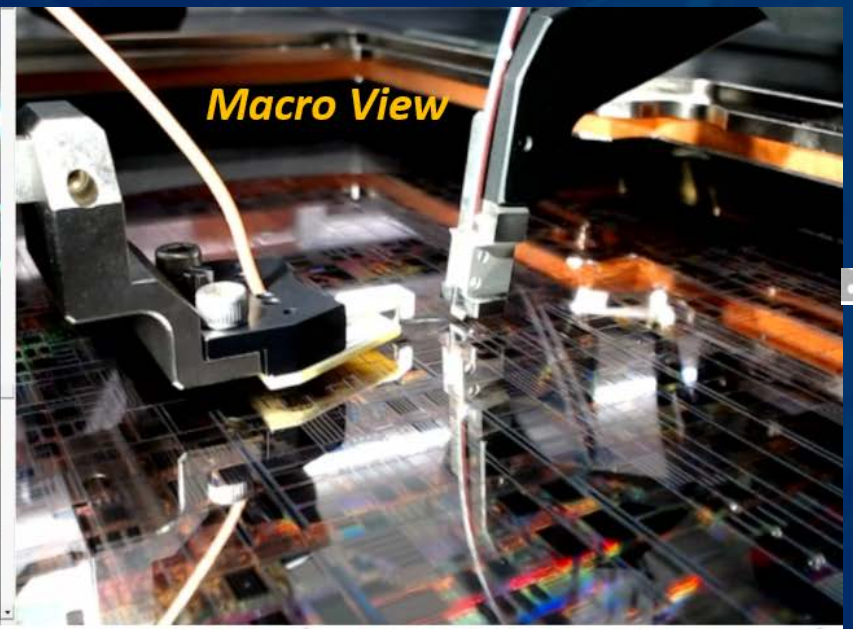
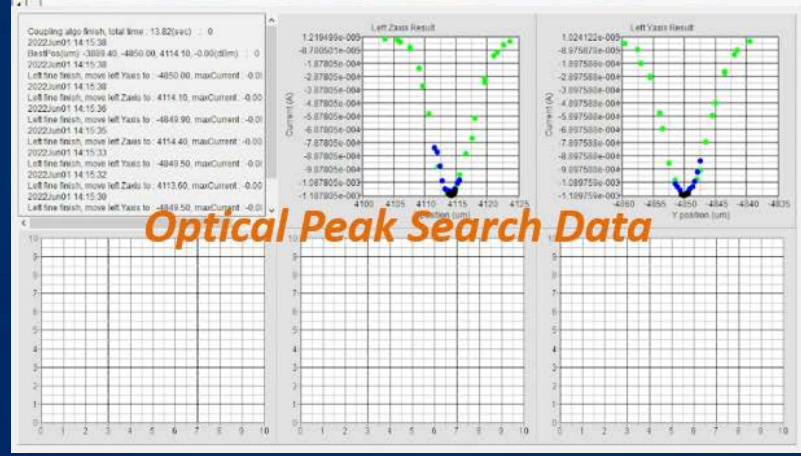
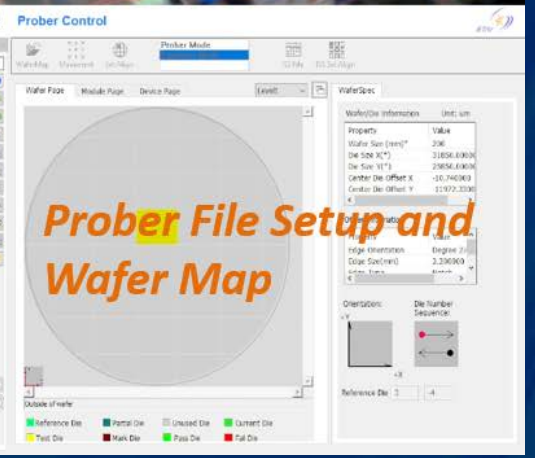


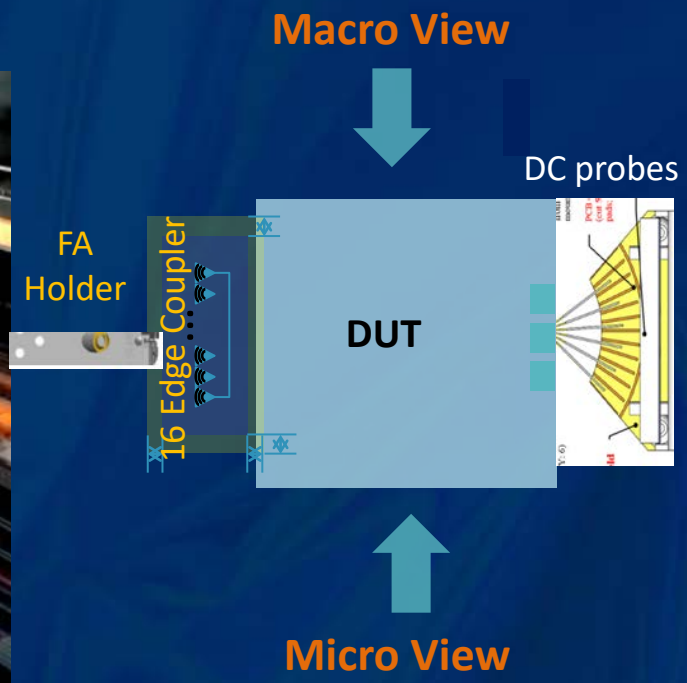
Photo Diode Test Video











Video Demo on Edge coupling OE Testing on PD. 2 dies tested in video

1) **Optical Input at West**
2) **Electrical probes at East**

Edge Coupling Performance

Key Features		
1.	Coupling Loss	CT average between 4 to 5 dB per facet
2.	GRnR	Excellent GRnR, 0.17dB @ 1 sigma
3.	Trench Width	> 85 um
4.	Trench Depth	> 40 um
5.	Coupler Pitch	127 um/250 um

Enable fast yield and performance feedback on wafers by up to 3 months compared to chip level test. Saving up to a year for full product development cycle (assuming 4 iterations)

Summary

- **Need for SiPh wafer test solution to address market needs as SiPh volume ramps up in the next 5 years**
- **SiPh Wafer Test solution with both vertical and edge coupling designed for high volume wafer test.**
  - CompoundTek Wafer edge coupling fiber array coupled with STAr Technologies wafer prober solution
- **Solution proven with customer production SiPh wafers.**
  - Optical Passive Test
  - Opto-electrical Test
  - High Speed Bandwidth test

Probe Card Market Dynamics and Cost of Test Analysis

Panchami Phadke
TechInsights

4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

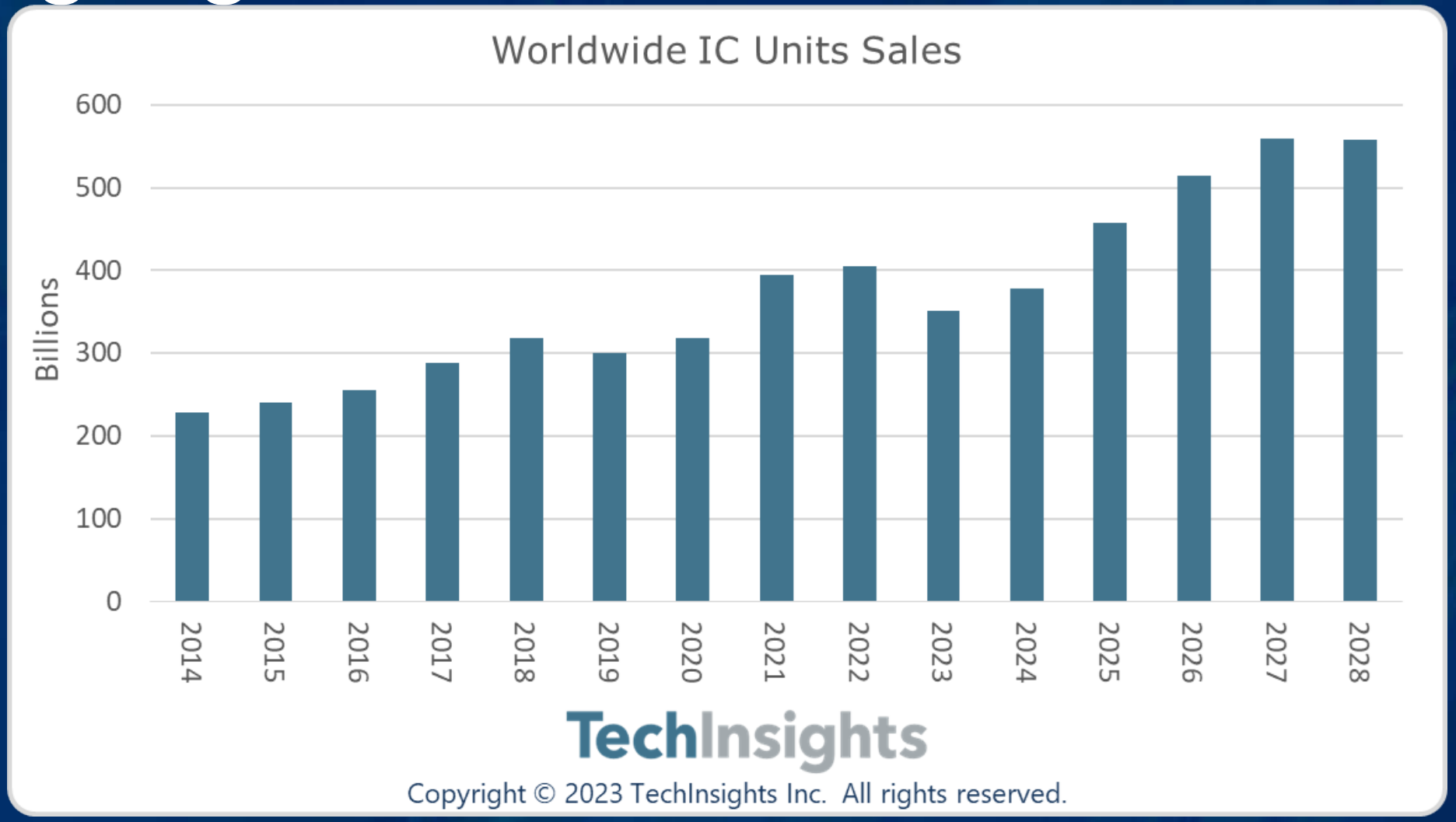
Overview

- Highlights of Semiconductor Market
- Global Probe Card Market
- Probe Cards by Device Type and Applications
- Probe Card Suppliers
- Probe Card Regional Data
- Semiconductor Test Market
- Cost of Test
- Conclusion

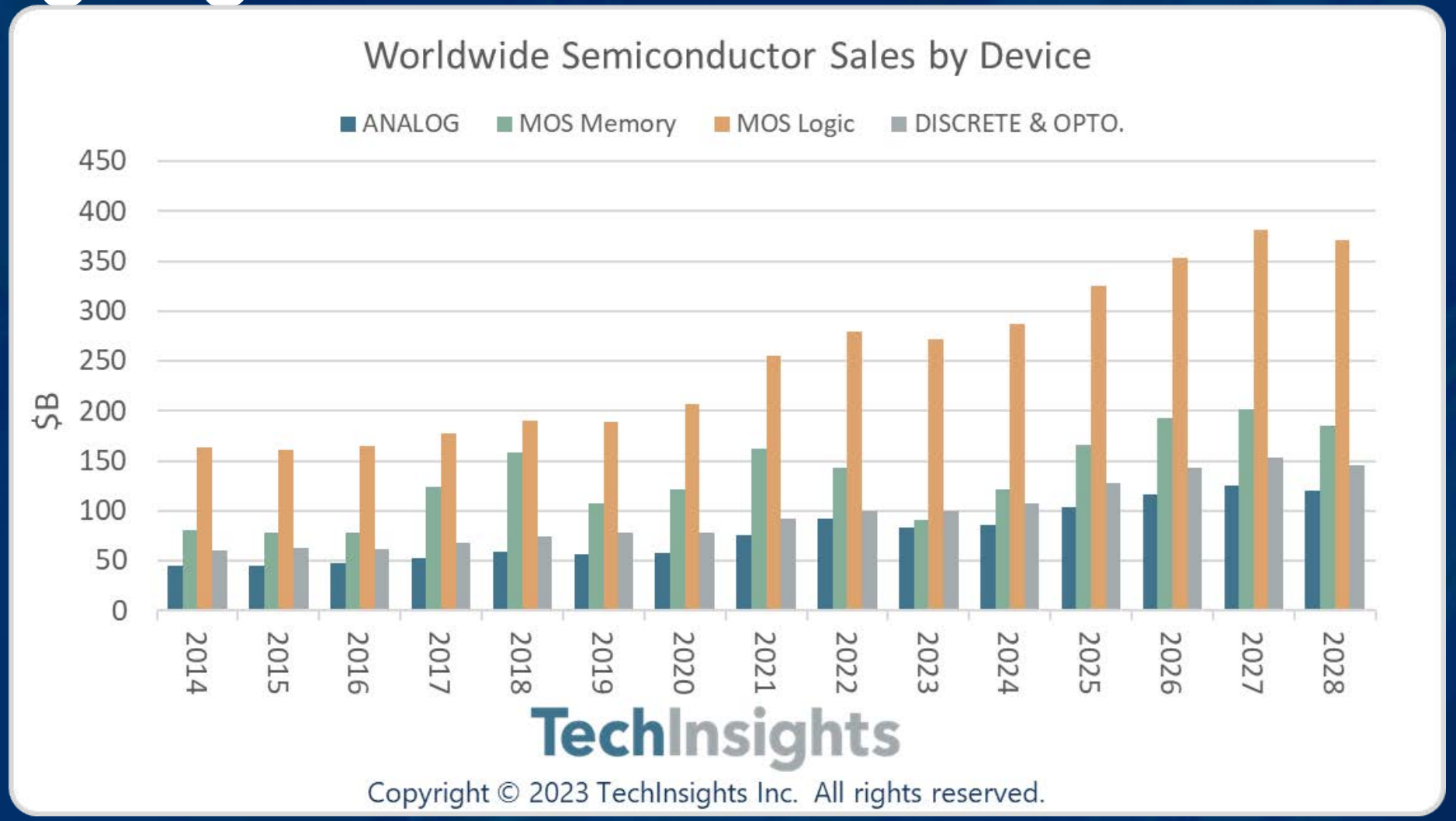
Highlights of Semiconductor Market

TechInsights' Current Forecast										
Forecast as of September 2023:	Q1 2023	Q2 2023	Q3 2023	Q4 2023	2023	Q1 2024	Q2 2024	Q3 2024	Q4 2024	2024
Semi Equipment ($B):	$ 34.8	$ 32.3	$ 32.0	$ 31.4	$ 130.5	$ 32.4	$ 32.9	$ 34.7	$ 35.3	$ 135.2
Sequential Change	-1.2%	-7.2%	-1.0%	-1.8%	-4.9%	3.0%	1.6%	5.5%	1.7%	3.7%
Capacity Utilization:	76.9%	73.7%	75.1%	74.3%	75.0%	78.3%	86.5%	90.1%	84.2%	85.0%
ICs ($B):	$ 102.4	$ 107.9	$ 115.3	$ 120.1	$ 445.7	$ 117.3	$ 120.0	$ 126.1	$ 130.8	$ 494.1
Sequential Change	-8.7%	5.4%	6.9%	4.2%	-13.3%	-2.4%	2.3%	5.1%	3.8%	10.9%
IC Units (BU):	86.9	89.2	85.8	89.1	351.0	86.1	90.9	97.5	104.2	378.6
Sequential Change	-9.7%	2.6%	-3.8%	3.9%	-13.3%	-3.4%	5.5%	7.2%	6.9%	7.9%
Electronics ($B) :	$ 600.5	$ 557.9	$ 597.1	$ 727.8	$ 2,483	$ 610.3	$ 583.2	$ 630.7	$ 779.0	$ 2,603
Sequential Change	-13.5%	-7.1%	7.0%	21.9%	-2.8%	-16.1%	-4.4%	8.1%	23.5%	4.8%

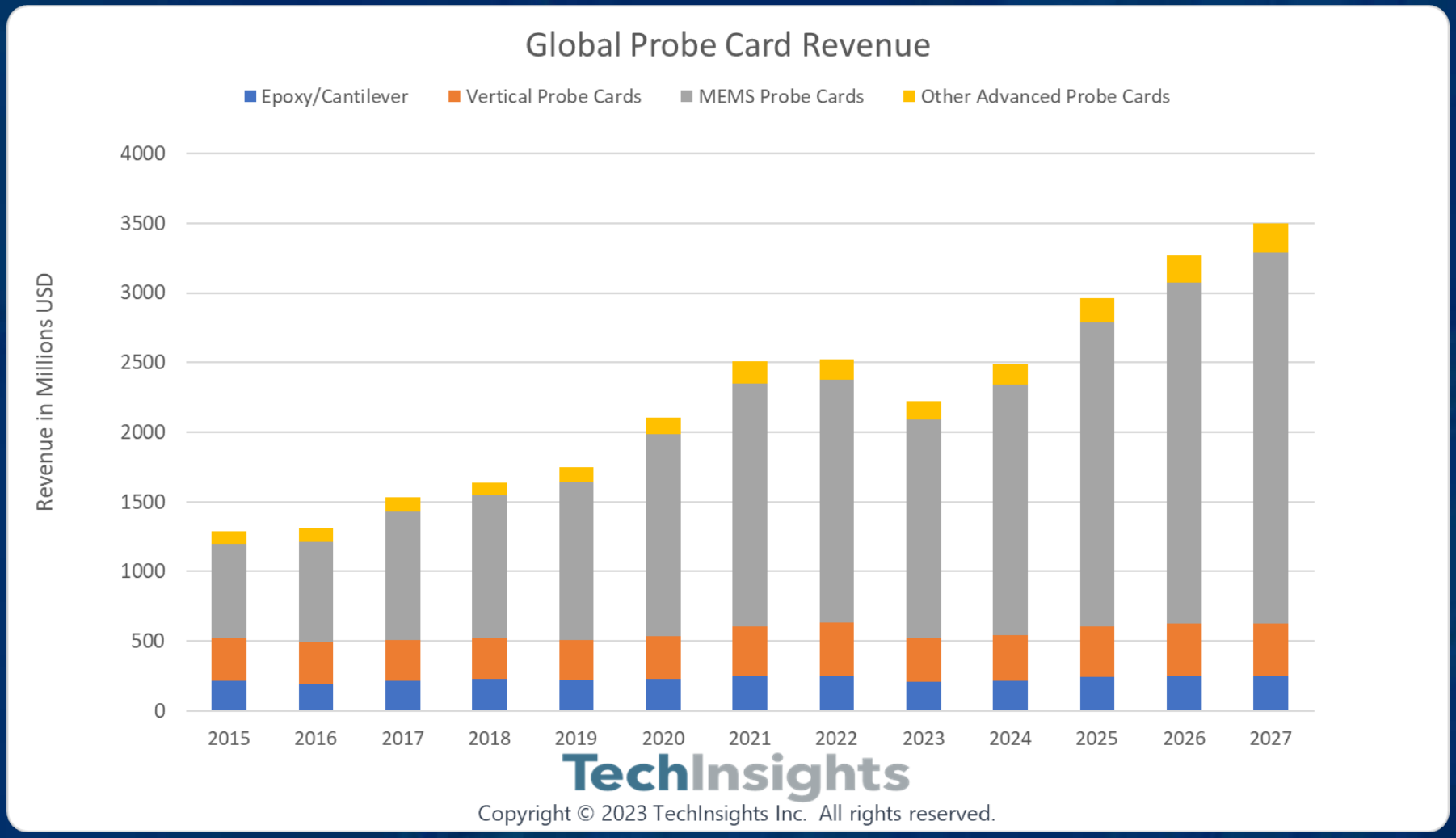
Highlights of Semiconductor Market



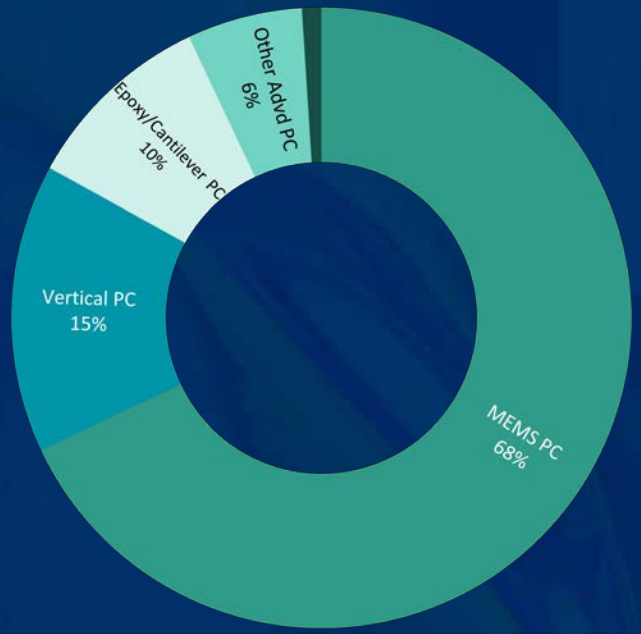
Highlights of Semiconductor Market

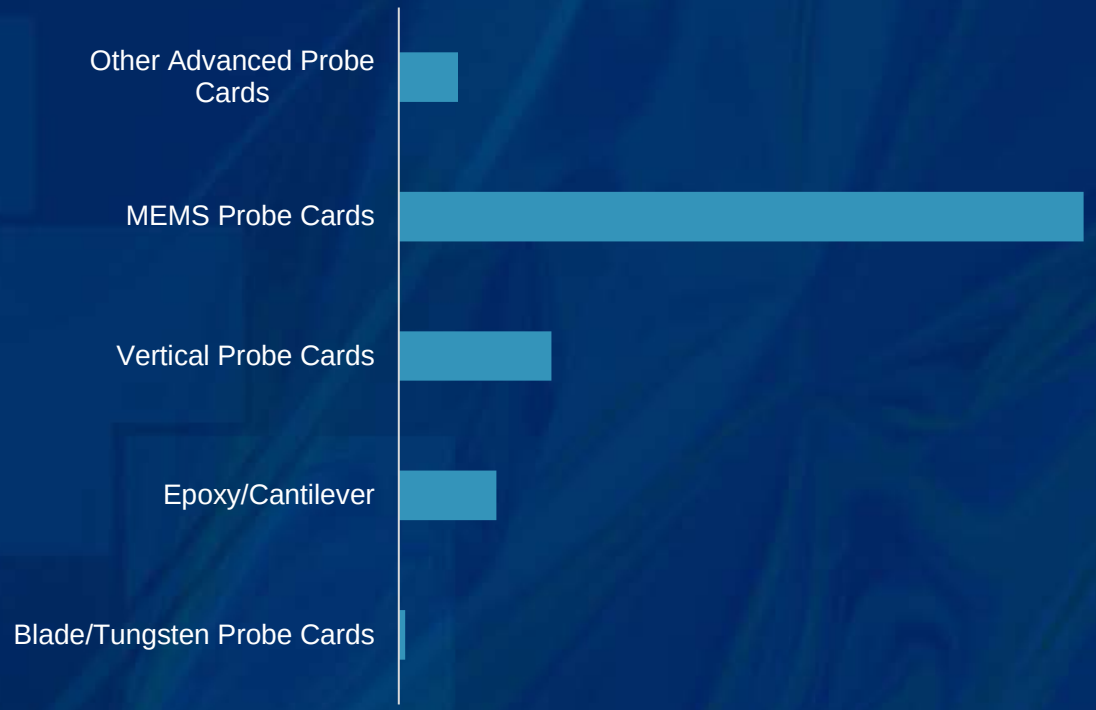


Global Probe Card Market

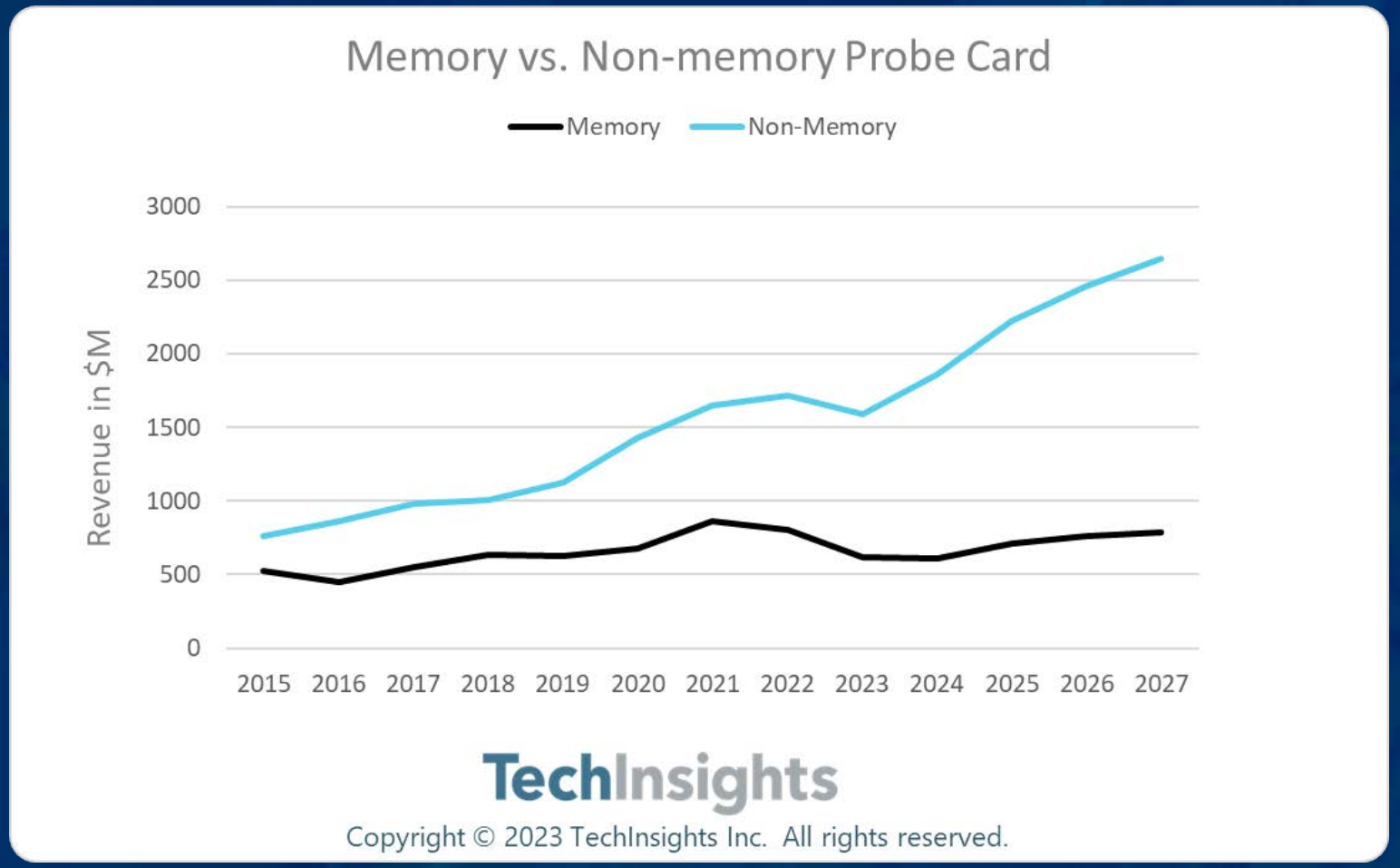


Probe Card Market 2022

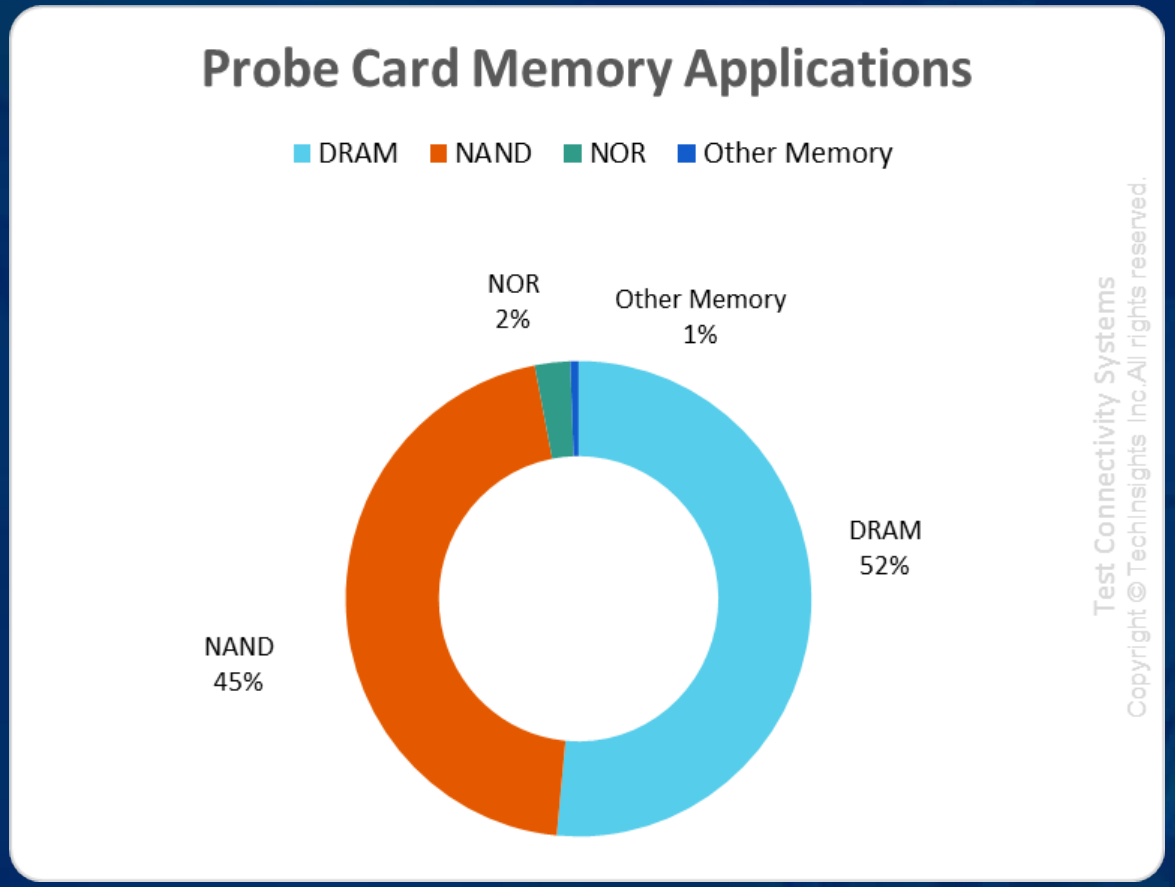


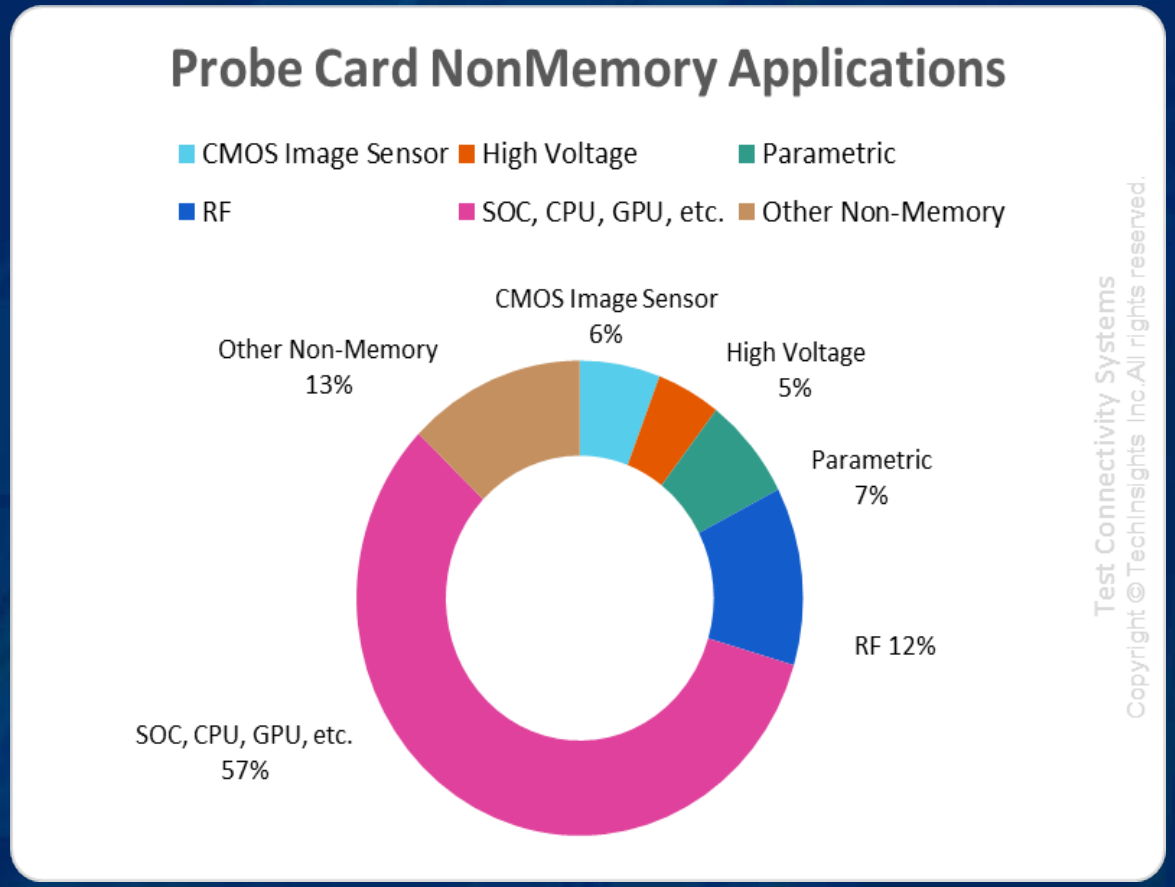


Probe Cards by Device Type



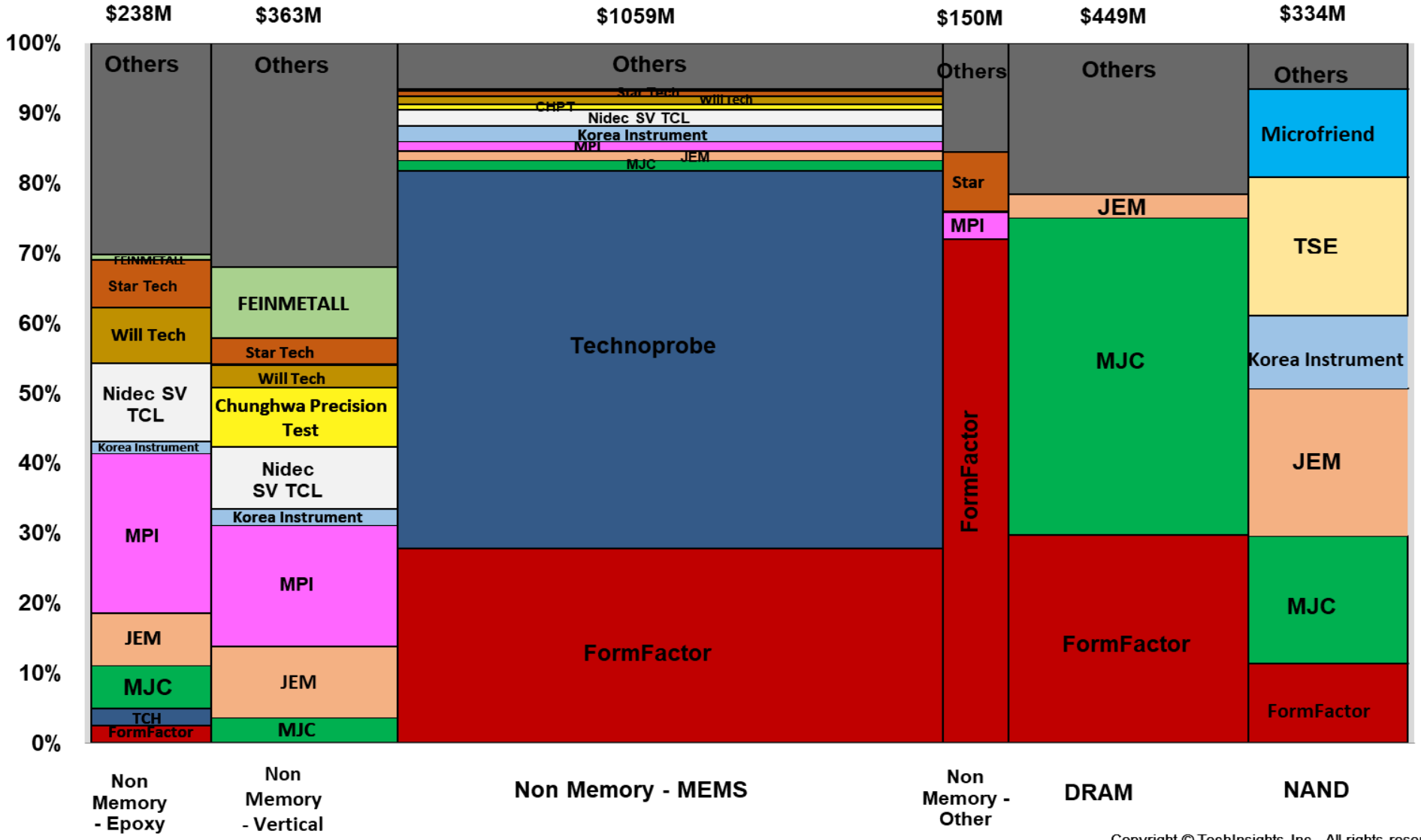
Probe Cards by Application



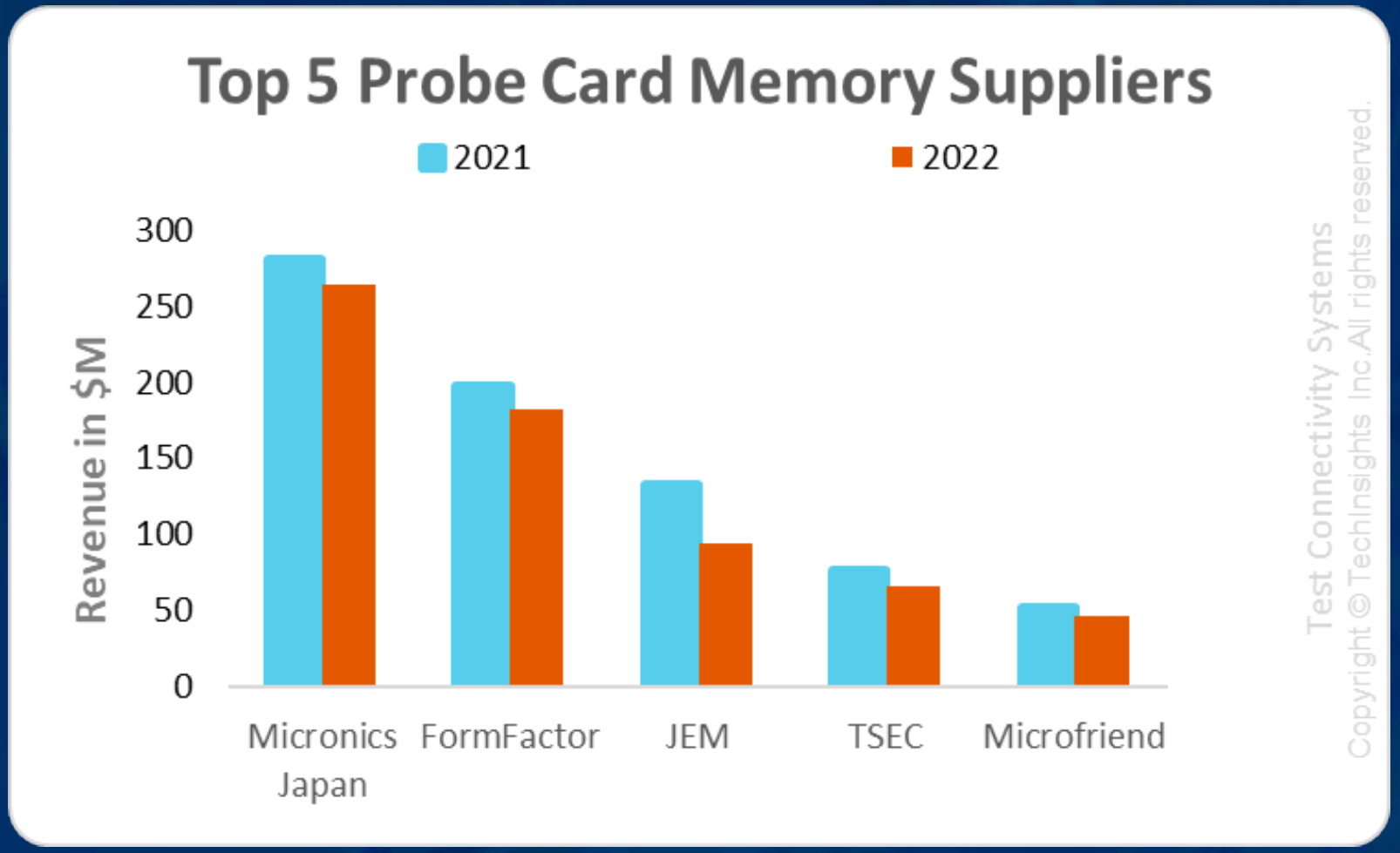


Probe Card Competitive Landscape

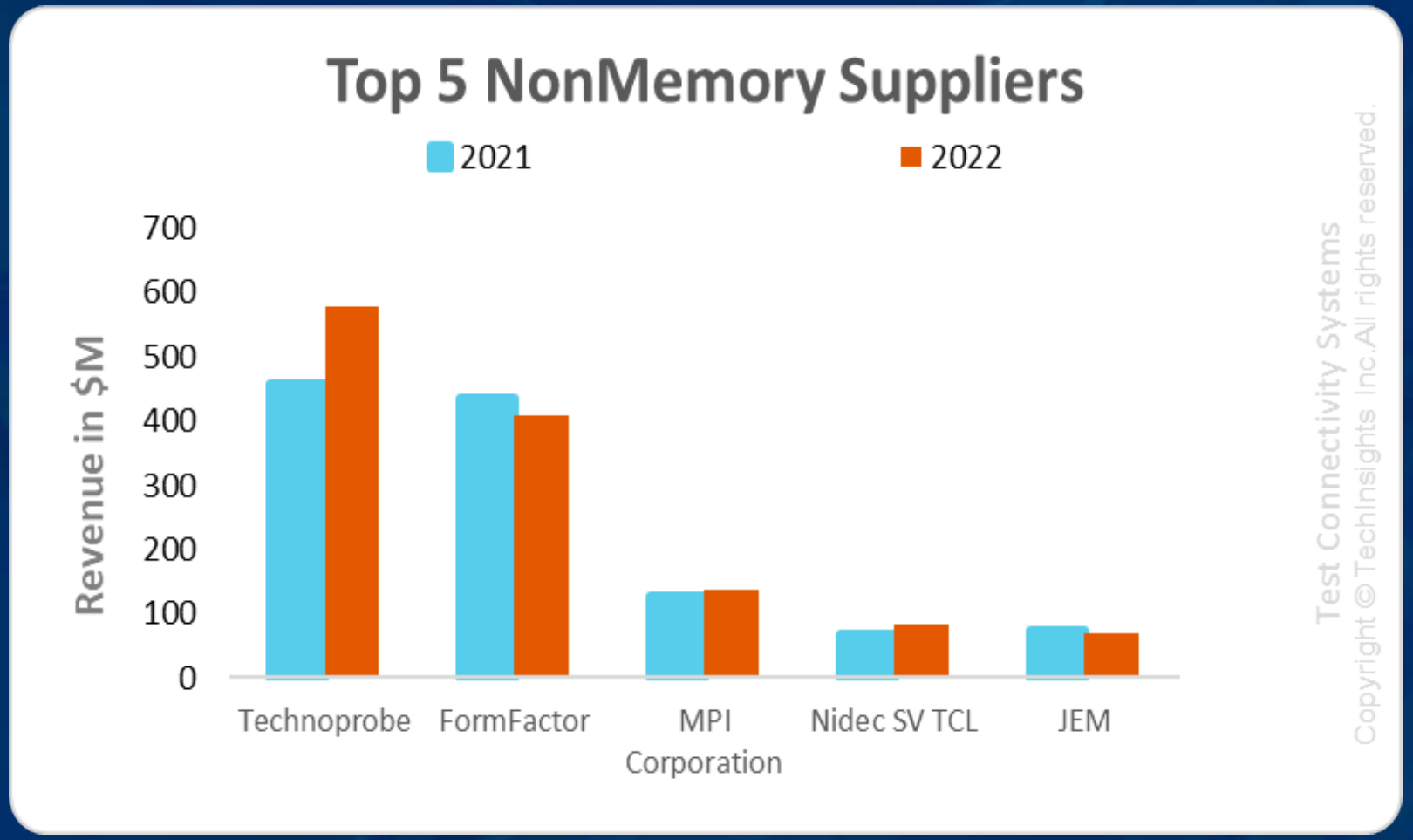
2022 Sizing and Market Shares



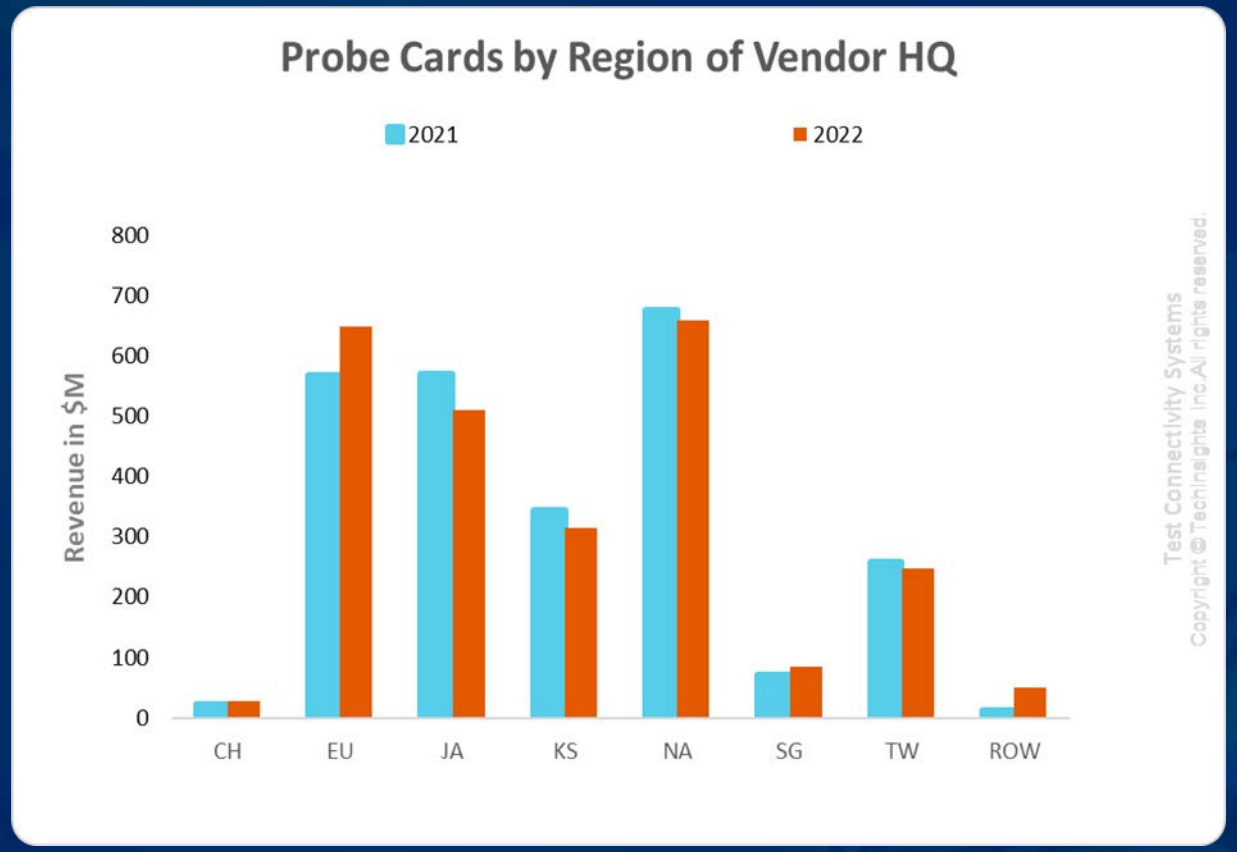
Probe Card Top Memory Suppliers

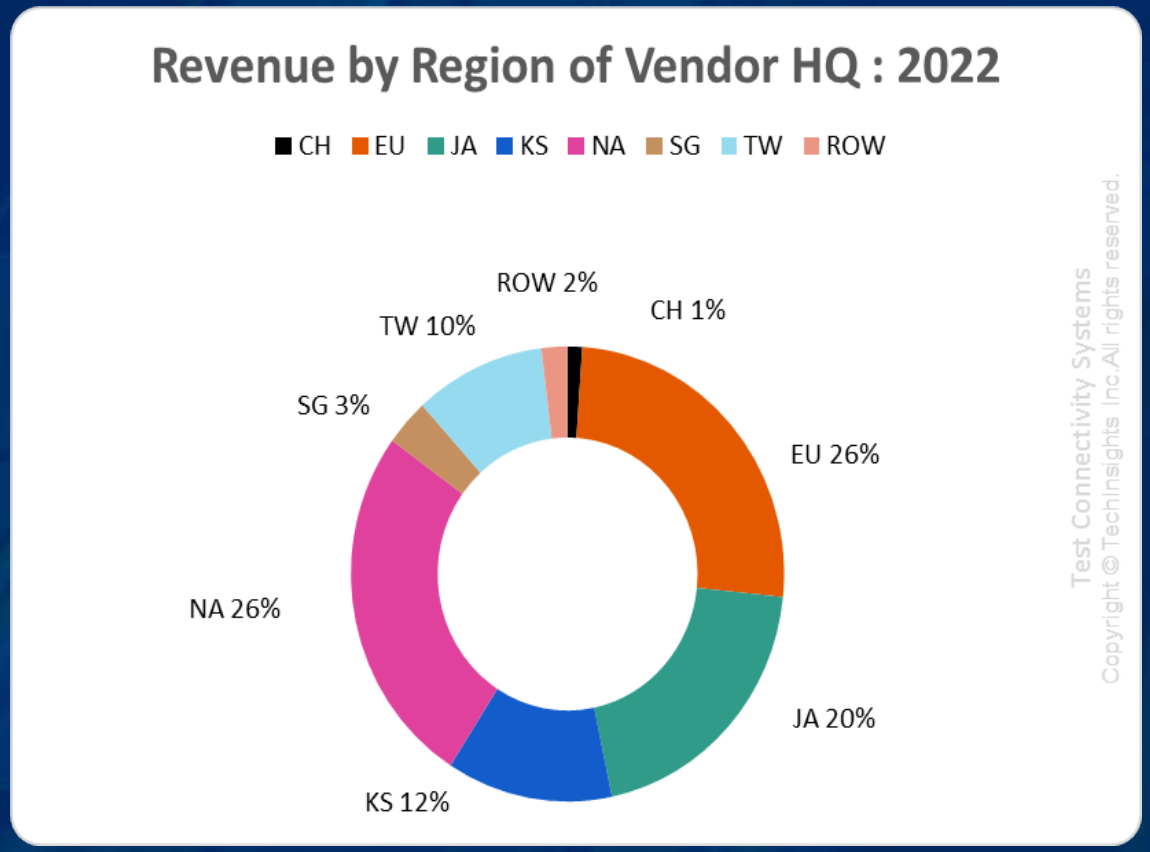


Probe Card Top Non-Memory Suppliers



Probe Cards by Region of Vendor HQ



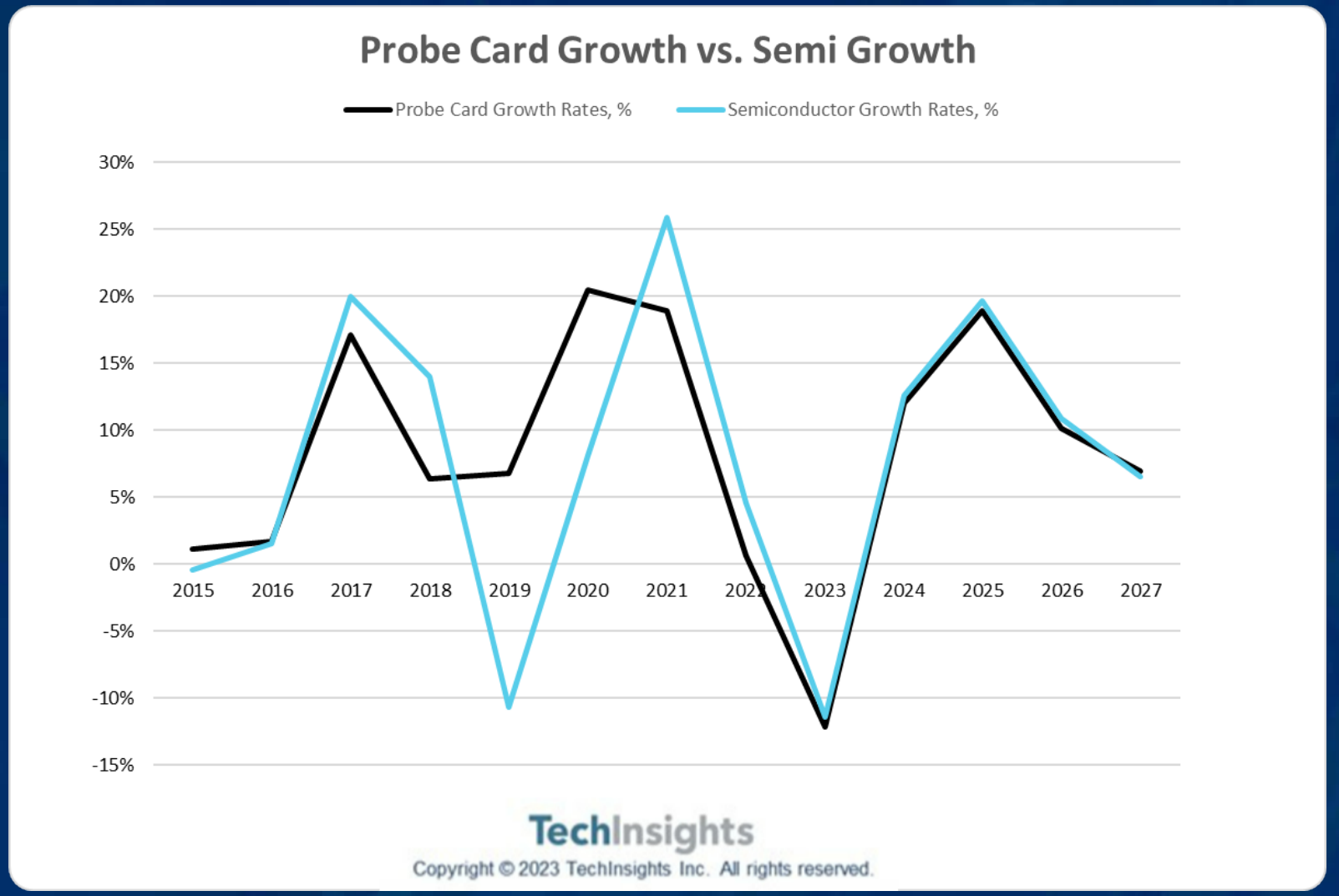


Taiwan Regional Sales by Vendor HQ

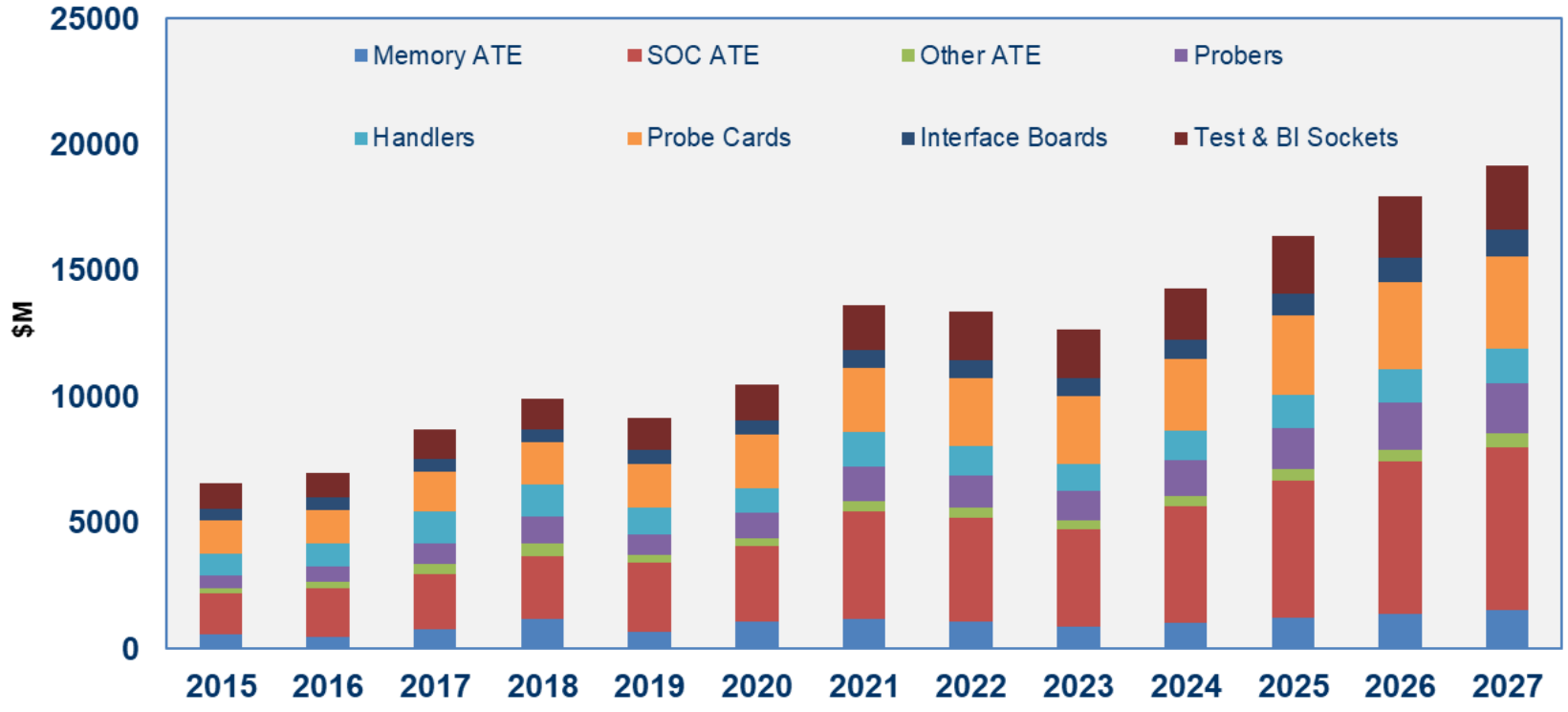
Taiwanese Vendors Epoxy–Cantilever Probe Cards Regional Performance, $M		
Region	2021	2022
CH	23.02	19.80
EU	0.19	0.16
JA	0.91	0.93
KS	0.61	0.81
NA	0.34	0.29
SG	2.68	2.83
TW	57.62	53.31
ROW	0.15	0.13
Total	85.52	**78.26**

Taiwanese Vendors Advanced Probe Cards Regional Performance, $M		
Region	2021	2022
CH	15.47	27.06
EU	1.80	1.88
JA	0.90	1.04
KS	1.40	1.70
NA	27.82	22.55
SG	10.52	11.51
TW	105.76	96.83
ROW	3.64	5.84
Total	167.31	**168.41**

Probe Card Growth vs Semi Growth



Semiconductor Test Market

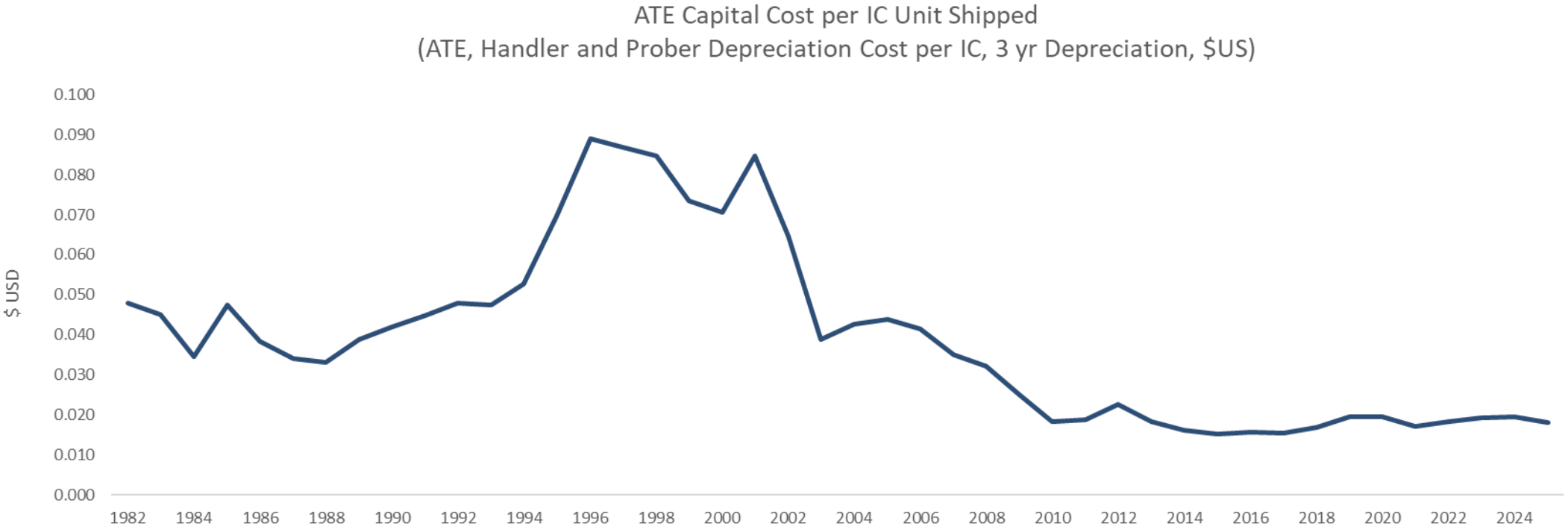


TechInsights

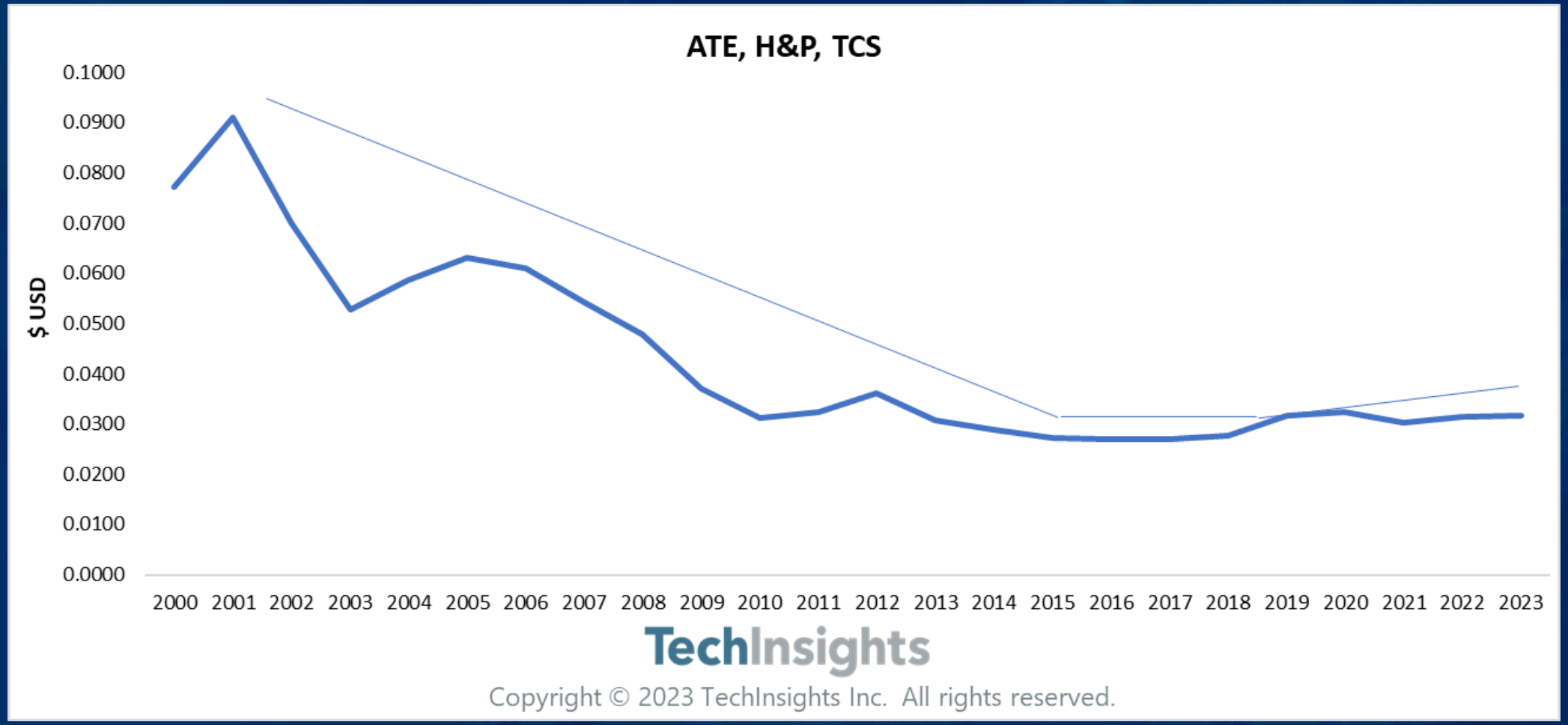
Semiconductor Test Market

- **Probe Cards, Test & Burn-in Sockets and Device Interface Board strong growth following the Semiconductor market**
- **Short term downgrade in TCS forecast, Potential for a decline in 2024**
- **Long term Socket growth of 6% until 2027**
  - Driven by non-memory
- **Long term Probe card growth of 8% until 2027**
  - MEMS, non-memory etc.
- **Long terms DIB growth of 7% until 2027**
- **ATE Market is expected to grow from $7B in 2022 to $7.6B in 2028 where memory has slower growth while Logic ATE market is growing rapidly**

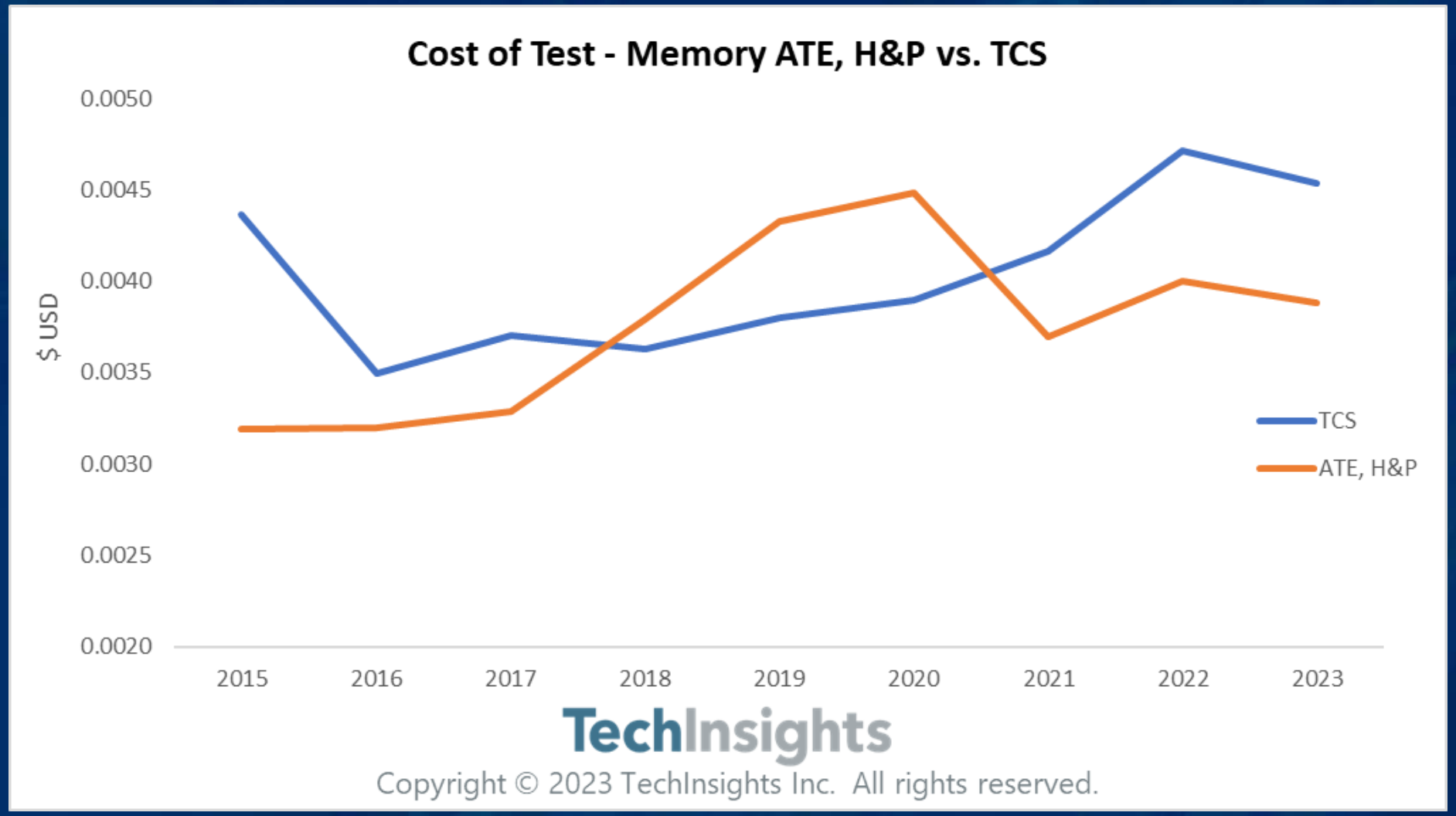
Overall Cost of Test View



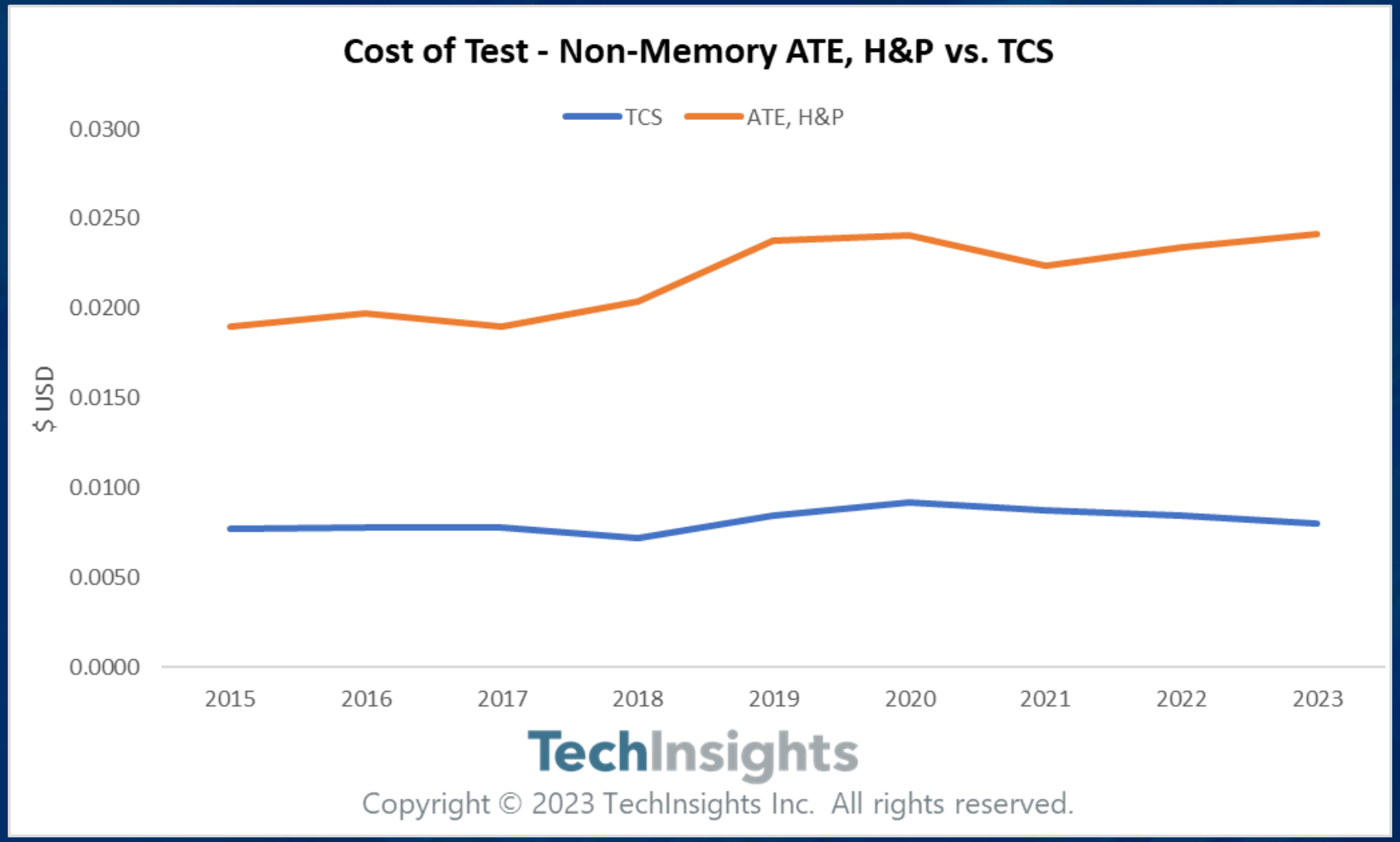
Cost of Test with ATE, H&P & TCS



Memory vs Non-Memory Cost of Test



Memory vs Non-Memory Cost of Test



Conclusion

- PC grew 1% in 2022 and expected to decline 5% in 2023
- DRAM expected to improve starting 2025
- COT has grown between 2 to 4% every year since 2017
- Decline in COT of both Memory & Non-Memory from 2012 to 2017
- Modest increase in Memory & Non-Memory COT since 2018
- Overall TCS costs are 2/3 of ATE, Handler and Probers market

Waveform Considerations on Shared Driver Signals

Shoichi MATSUO
Micron Memory Japan

Overview

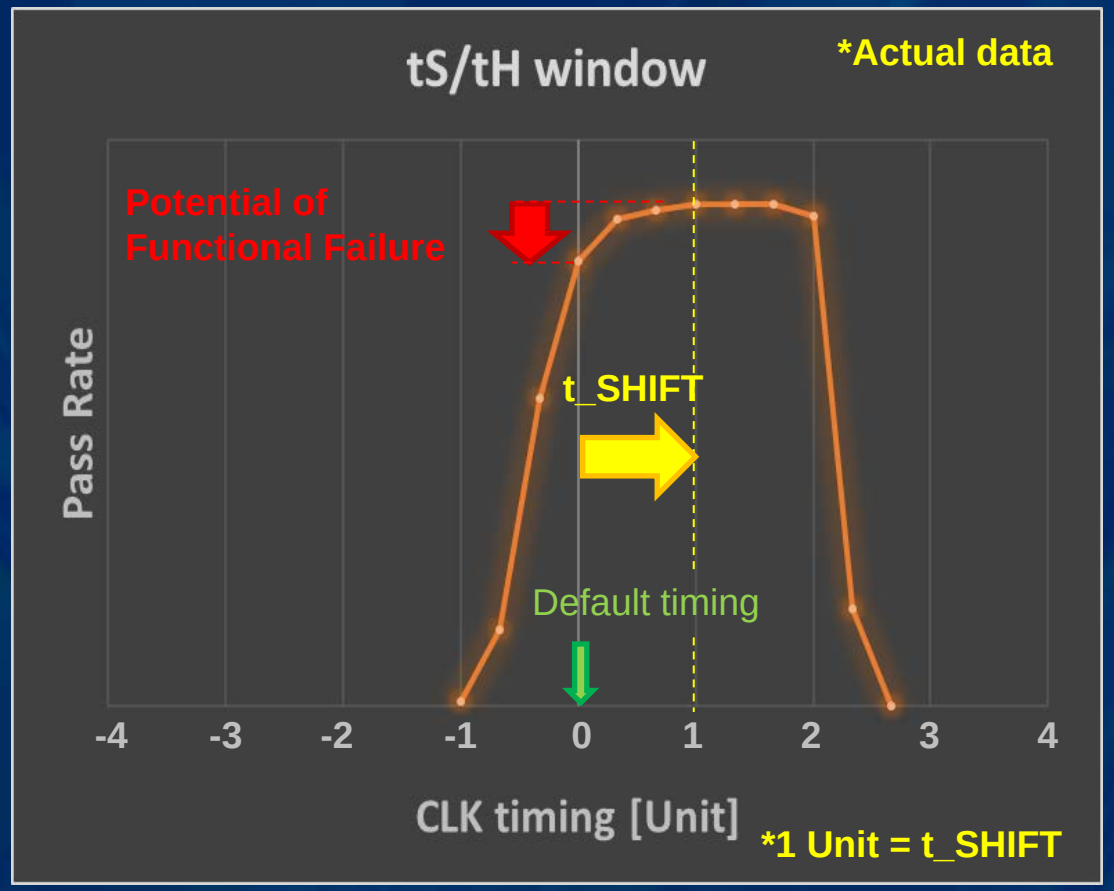
- Background
- Problem statement with real case examples
- Waveform simulation
- High frequency and KGD
- Ask of the industry
- Summary

Introductory Background

- Increasing parallelism by driver sharing can reduce test costs.
- Limited tester resources require high sharing of driver signals.
- Understanding & managing high sharing impacts is challenging.
- These challenges will be highlighted in this presentation.

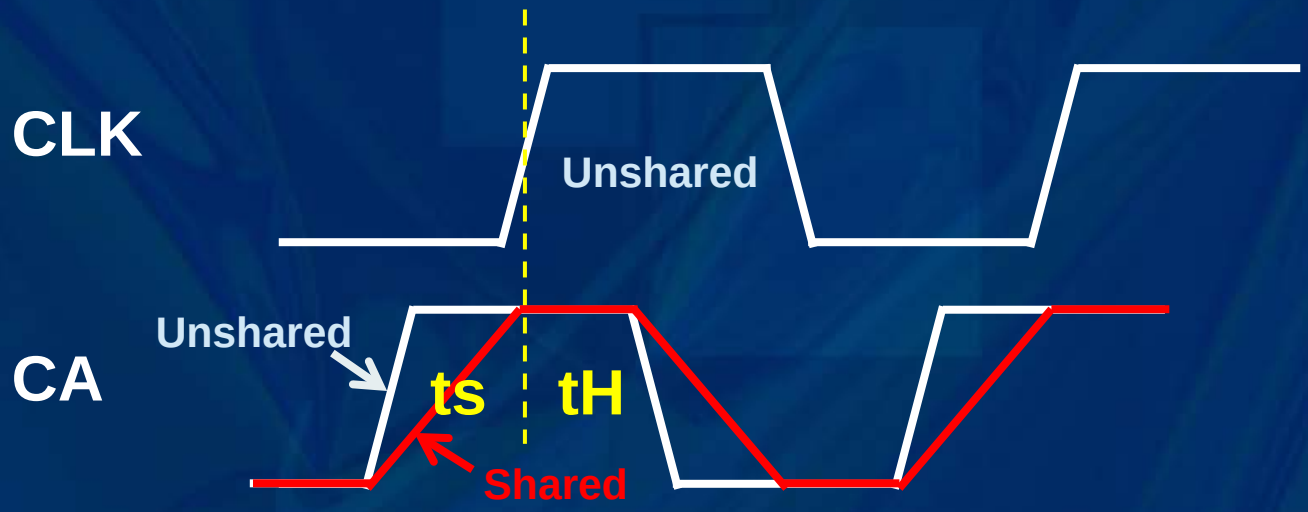
Problem Statement

- **During test program debugging functional failures observed.**
  - What caused tS/tH window between CLK vs. CA to shift?



Combination, Unshared & Shared Driver

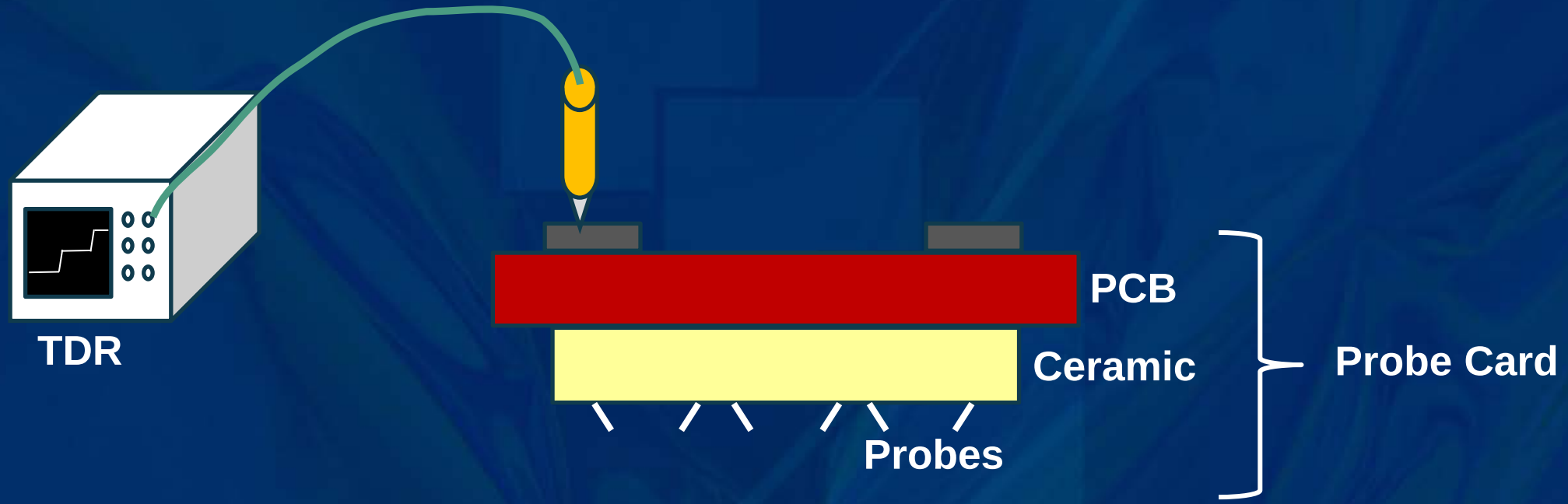
- In this case, both unshared and shared drivers were used. It was known that there was a timing delay between CLK & CA due to slower rise time on the shared CA driver.
  - CLK pin – Unshared
  - CA (Command / Address) pins – Shared



Compensating for Timing Delays

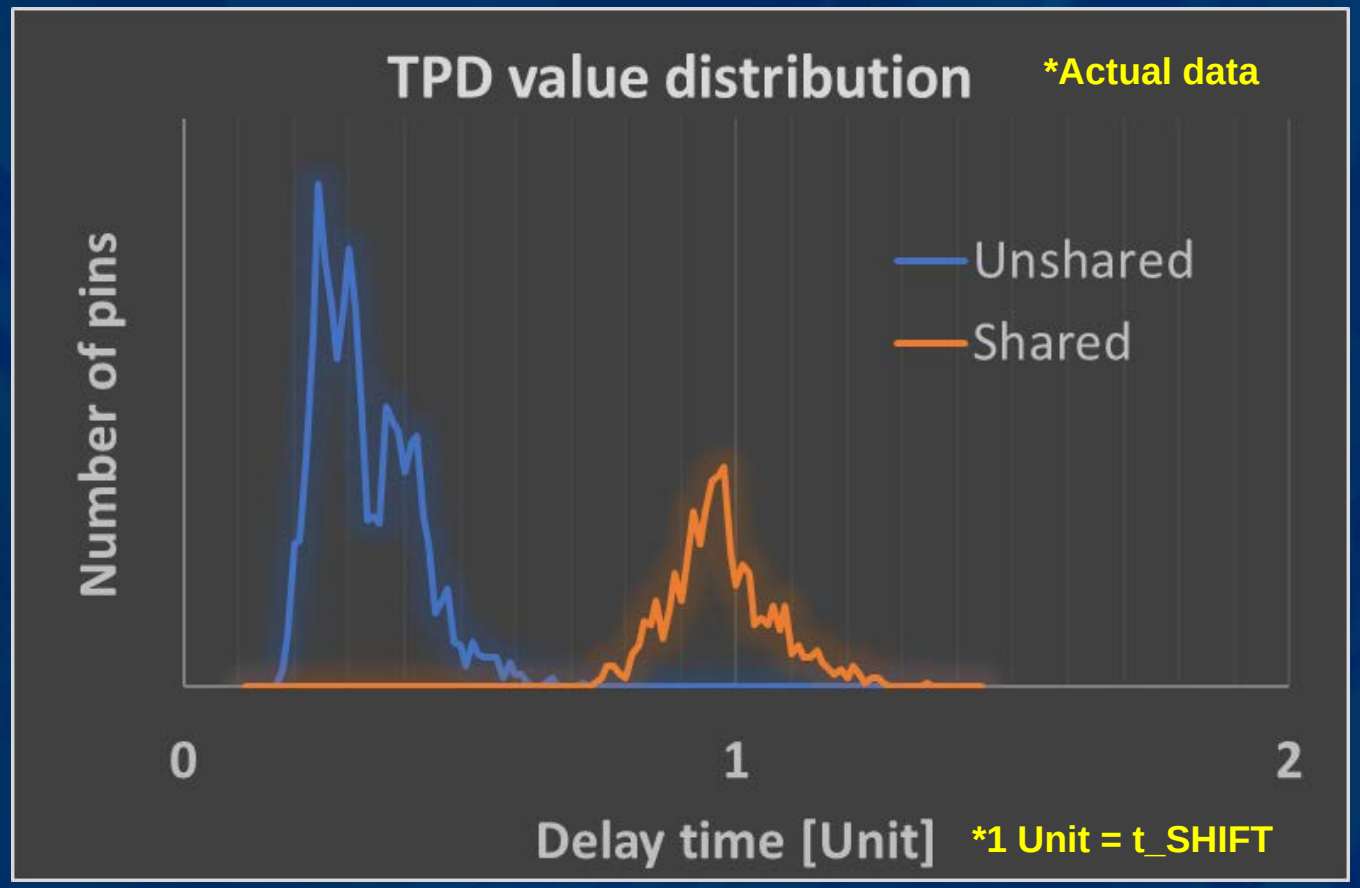
- **TPD value by TDR measurement can compensate timing delays.**

*TPD : Time Propagation Delay



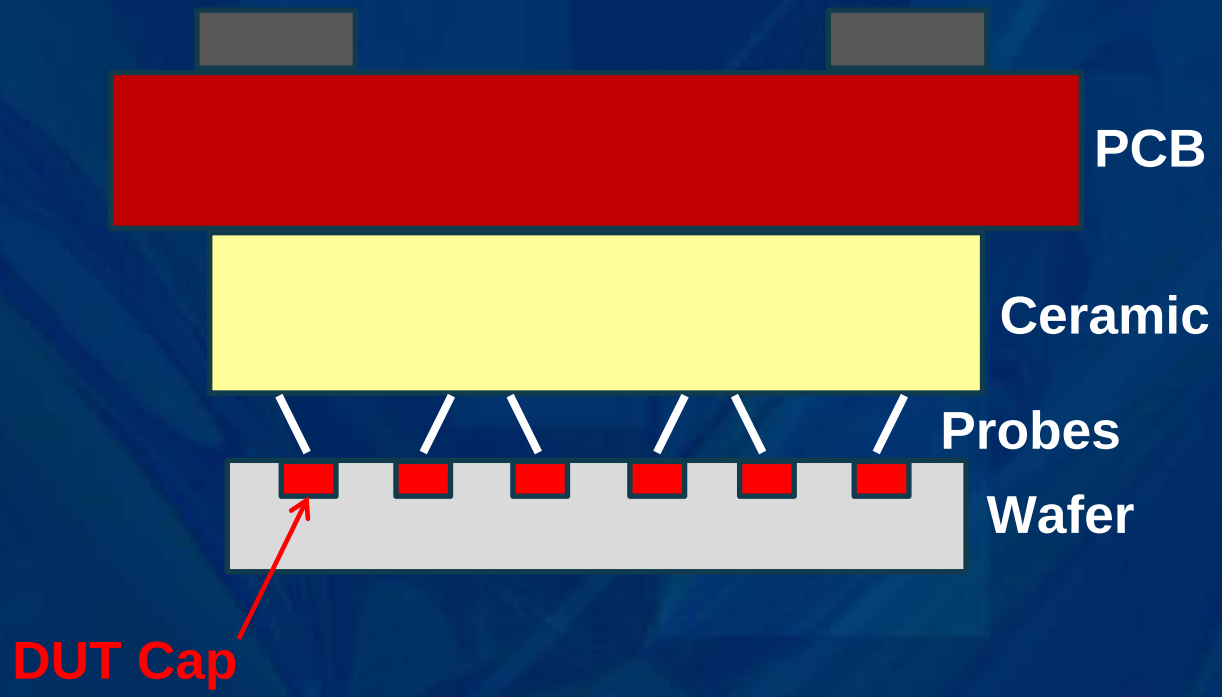
Distribution of Measured TPD Value

- **TPD values were implemented, functional fail still occurred.**
  - Any other parameters missed in design?



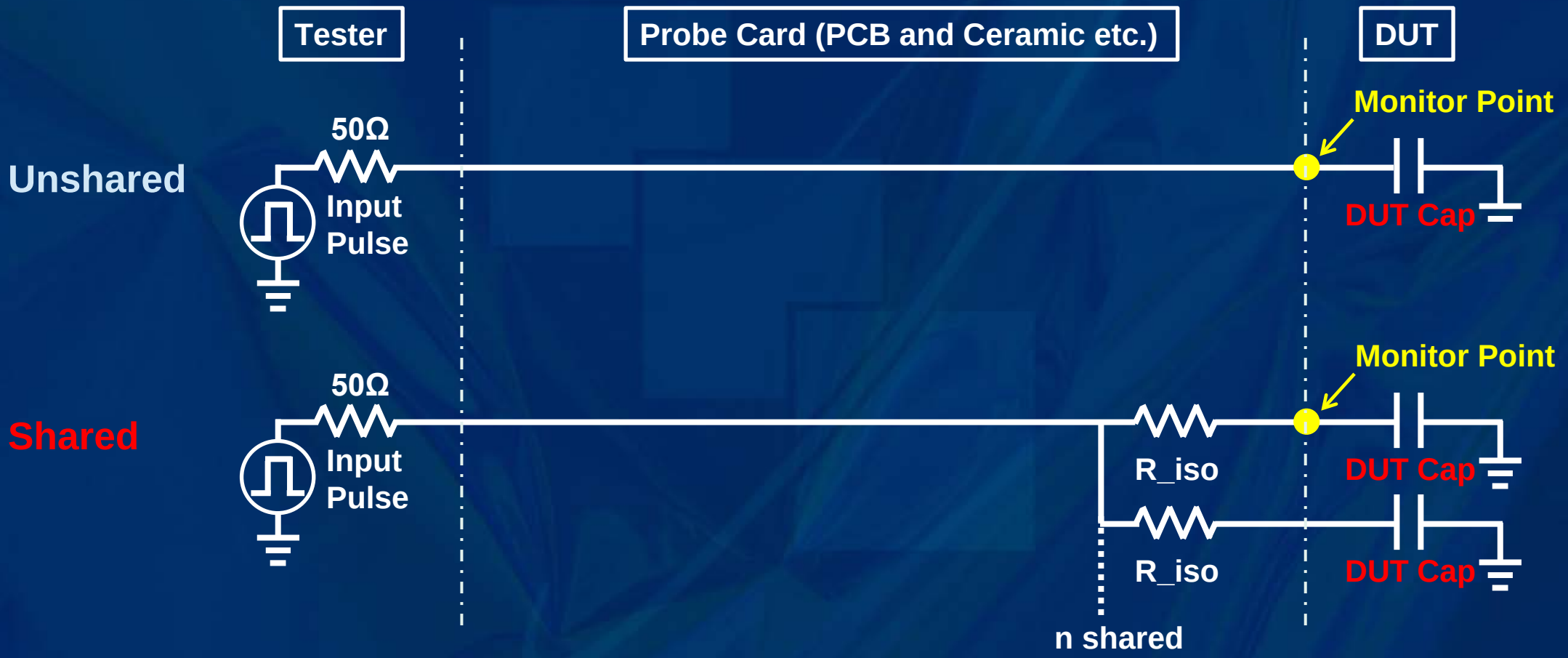
Missing Parameters

- **What if the input capacitor on the device pads were missed?**



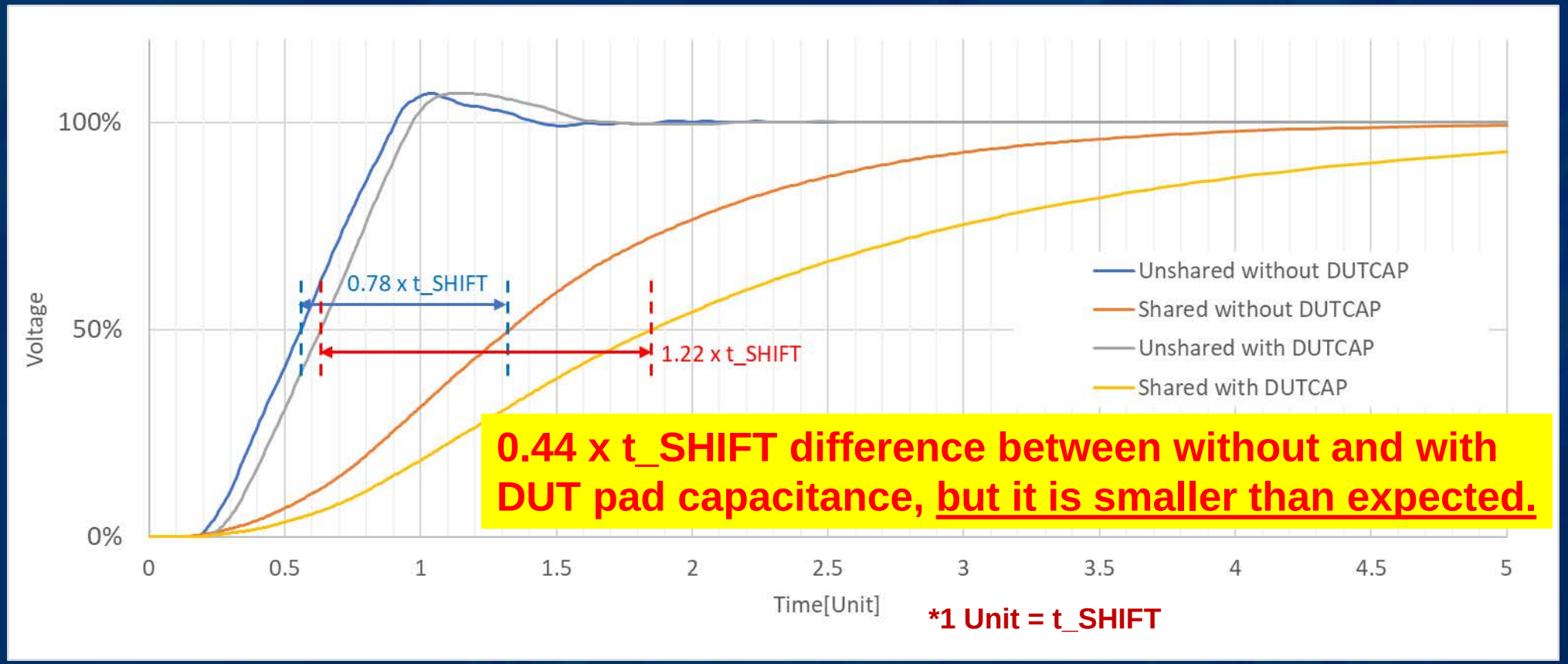
Waveform simulation (1)

- **Simulation model**



Waveform simulation (2)

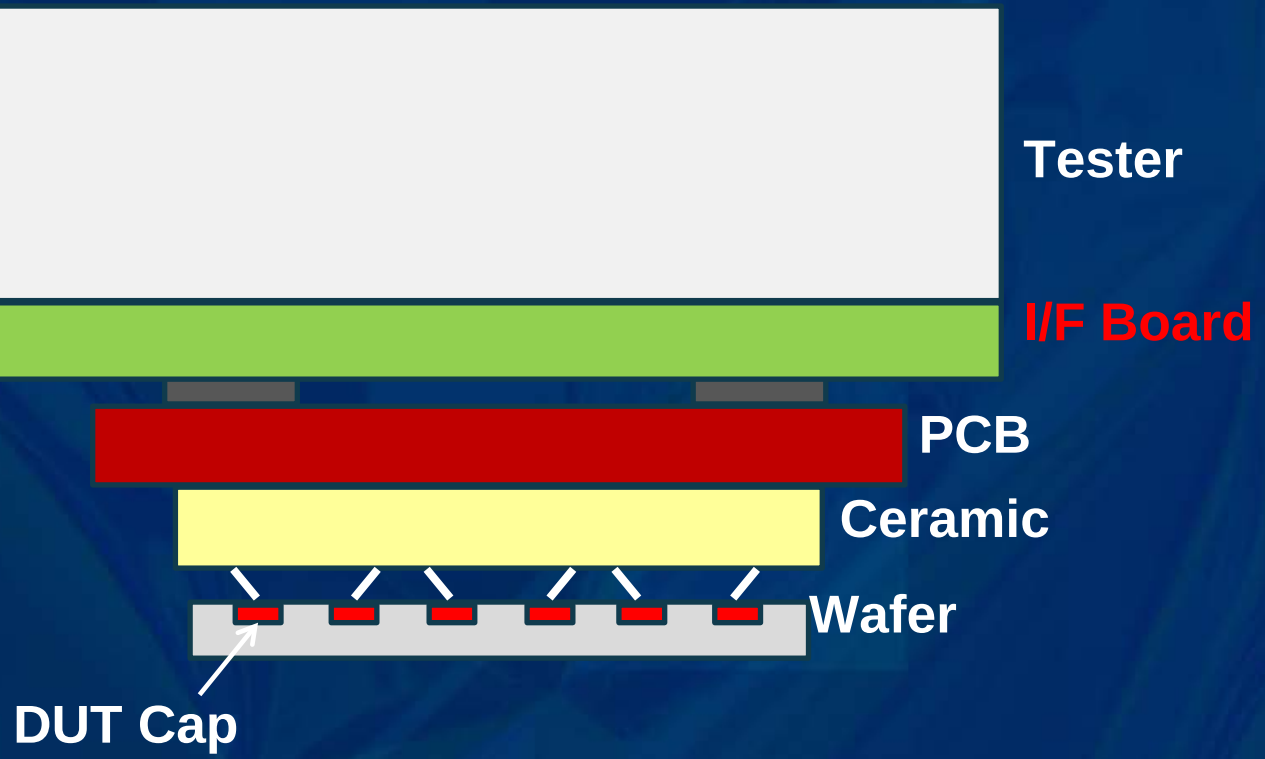
- **Difference between without & with DUT pad capacitance**



- **Other missing parameters?**

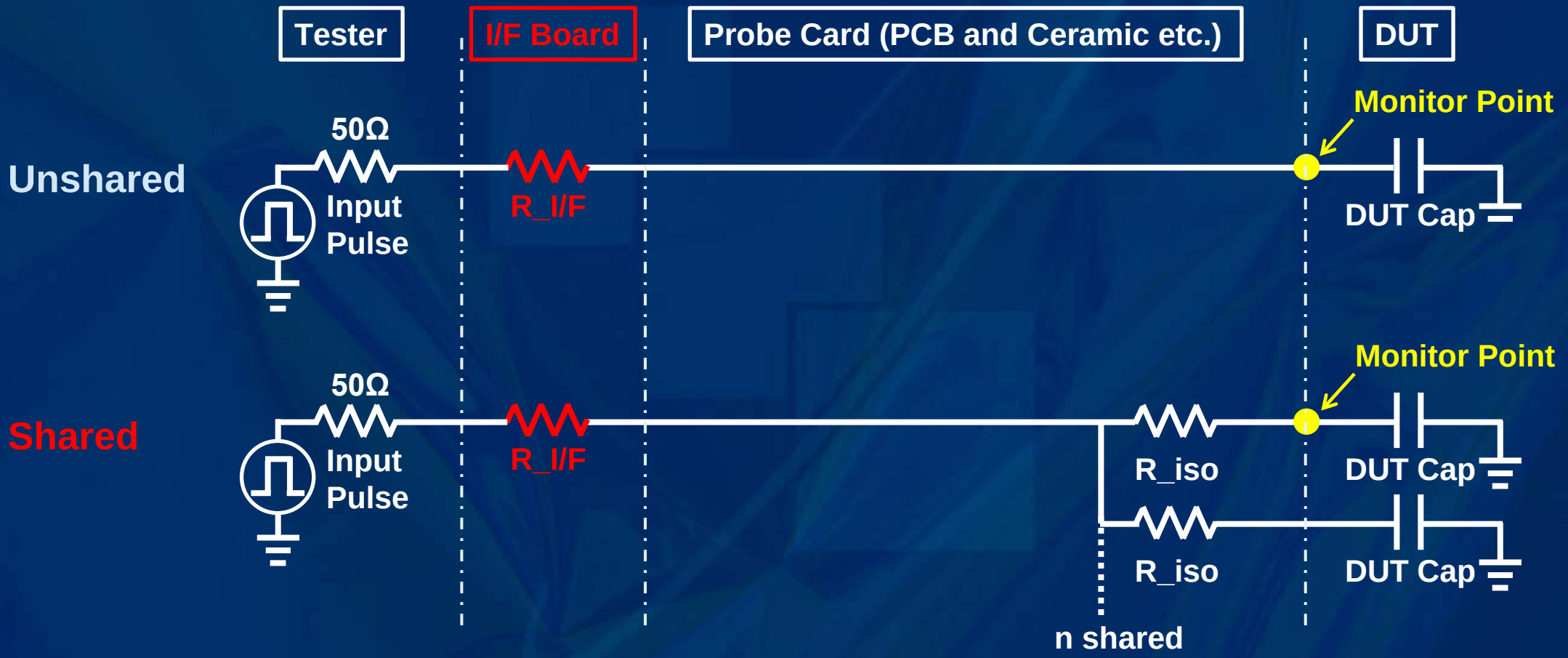
Another Missed parameter

- **What if resistance of the I/F Board was missed in simulations?**



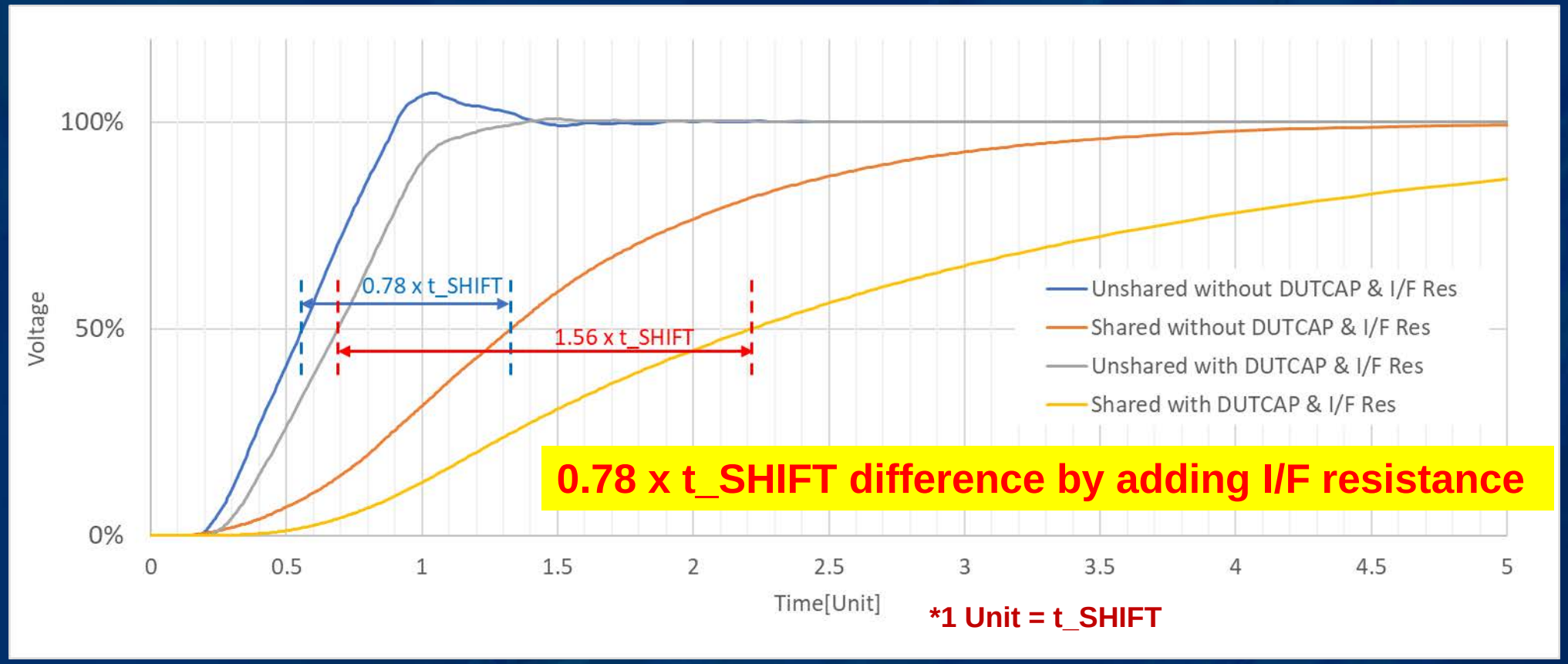
Waveform simulation (3)

- **Simulation model (2)**



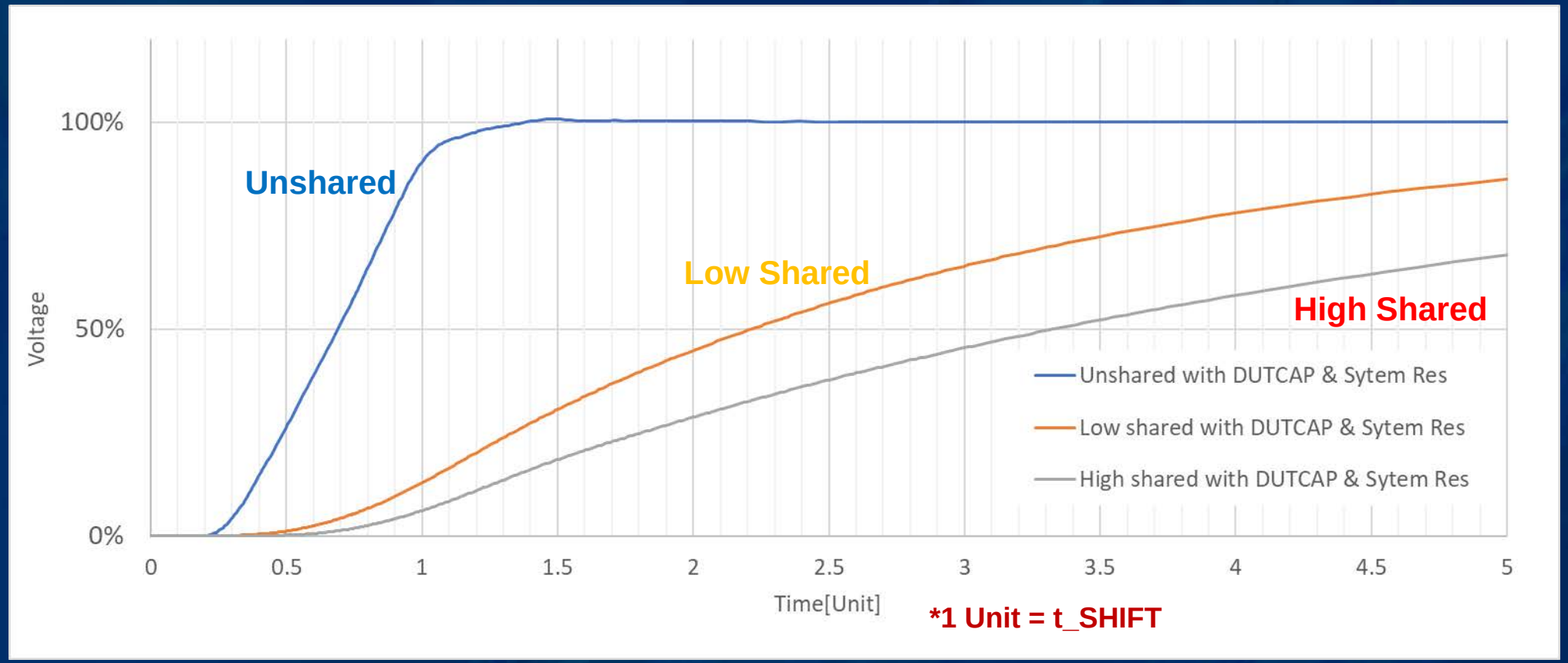
Waveform simulation (4)

- **Adding an additional resistance from the I/F board**



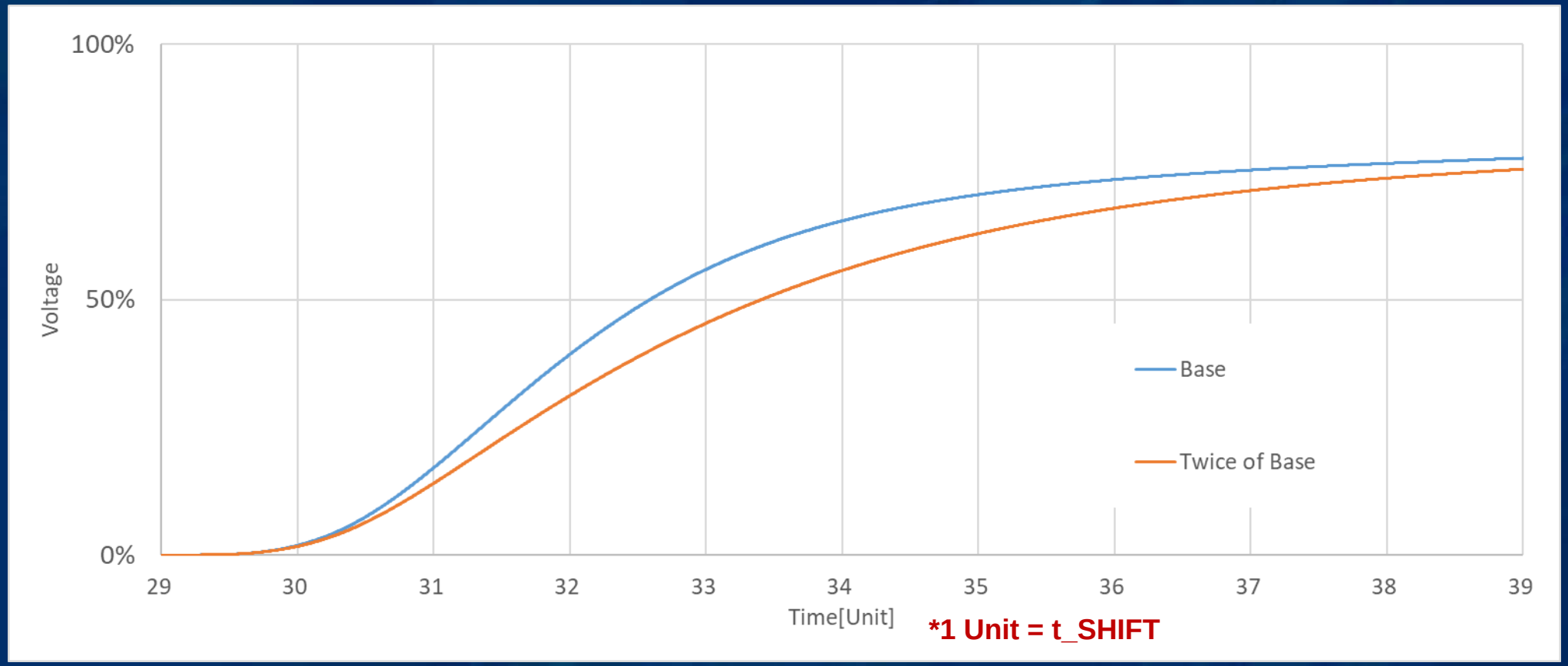
Waveform simulation (5)

- **Dependency on number of shared drivers**



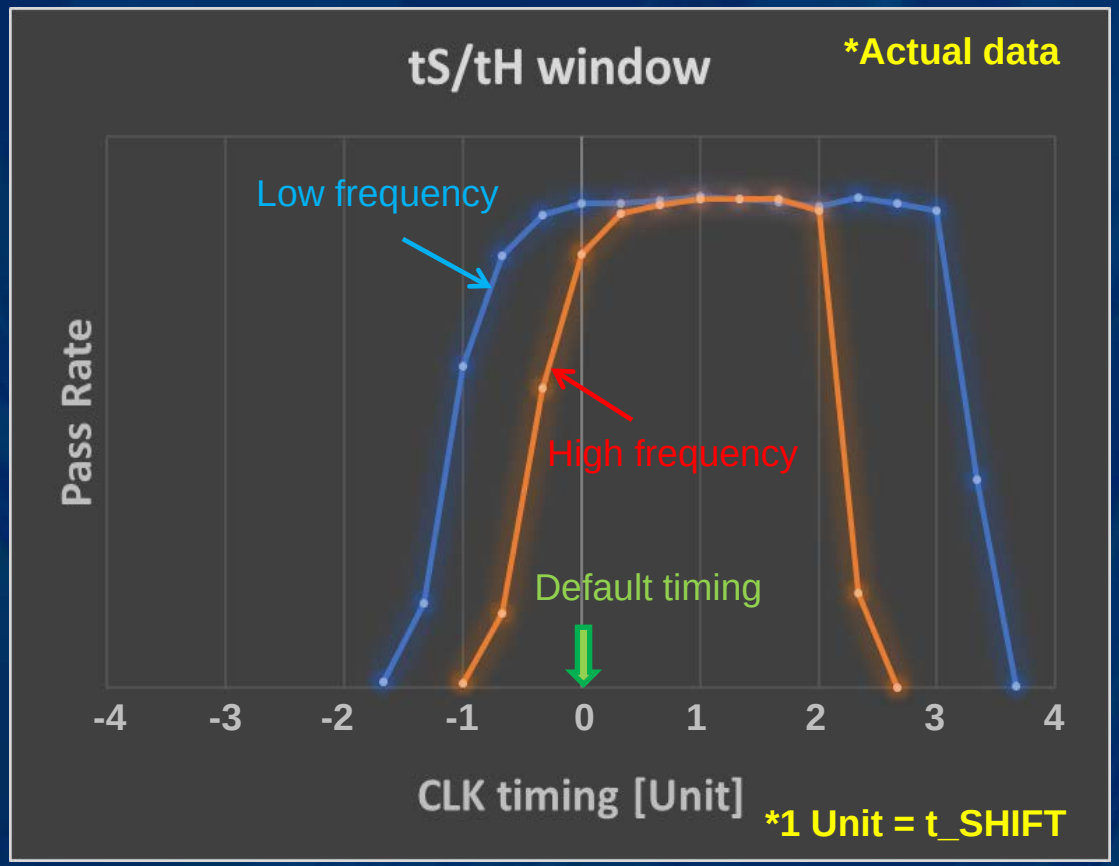
Waveform simulation (6)

- **Changing wiring capacitance on the probe card**



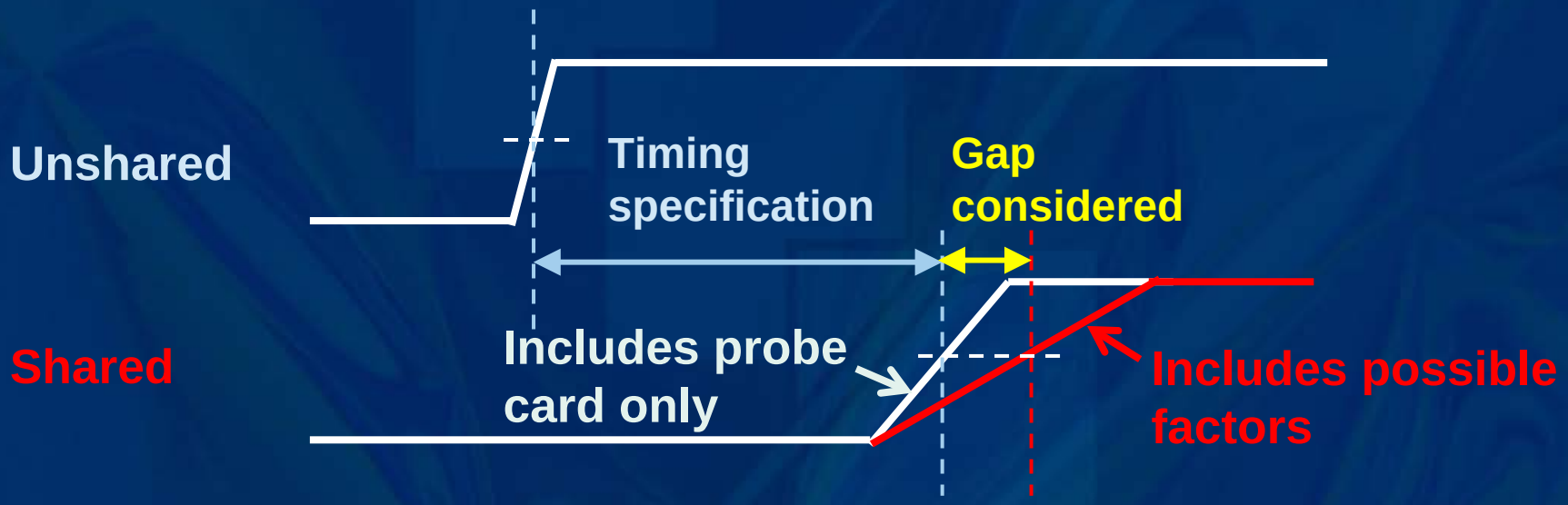
High Frequency Functional Testing

- **High test frequency reduces test time but narrows tS/tH window.**
  - Overcoming shifted tS/tH window (shared & unshared signal).



Used Case Known Good Die (KGD)

- **As KGD timing specification is guaranteed by wafer test, the shared/unshared phenomena must be accounted for during test.**



Ask of Probe Card Industry

- **Lowering the value & variation of capacitance & resistance of trace lines helps to keep test conditions equally between Duts.**
- **Micron is asking Probe Card supplies to help in this area**

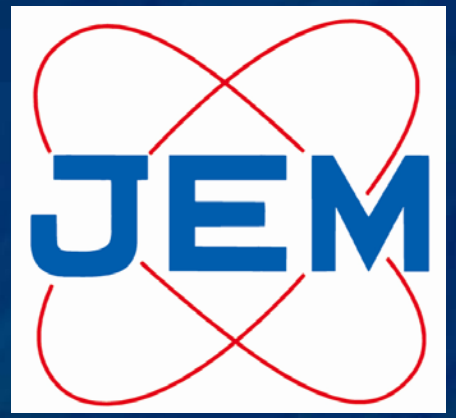
$$\tau = (R_{CARD} + R_{ISO} + R_{SYSTEM}) \times (C_{CARD} + C_{DUTCAP} + C_{SYSTEM})$$

Summary

- Factors other than probe card can change a tester's waveform.
- Micron considers the whole ATE test cell system during design.
- Probe Card trace to trace difference in capacitance, resistance, shared & unshared is an area for Probe Card Suppliers to help.

Acknowledgements

- **Special thanks to:**
  - **Micronics Japan Co., Ltd.:**
    - Yuki Kasai
    - Toshiyuki Kudo
  - **Japan Electronic Materials Corp.:**
    - Yuken Oishi
    - Tomonao Nakashima



HOW TO ALIGN 3D ICs FOR TESTING AT DIE LEVEL

Using AMT5000 & HBM as an Example

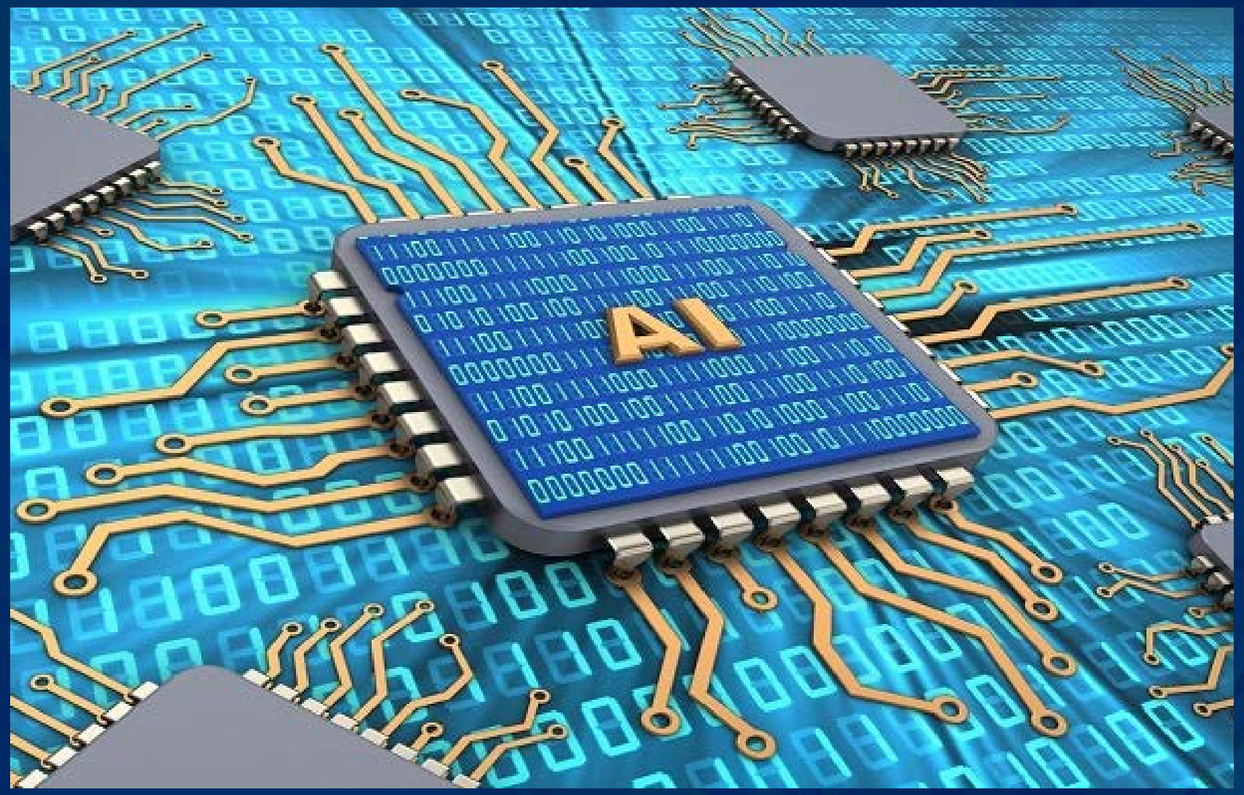
Calvin Park
Advanced Mechatronics Korea

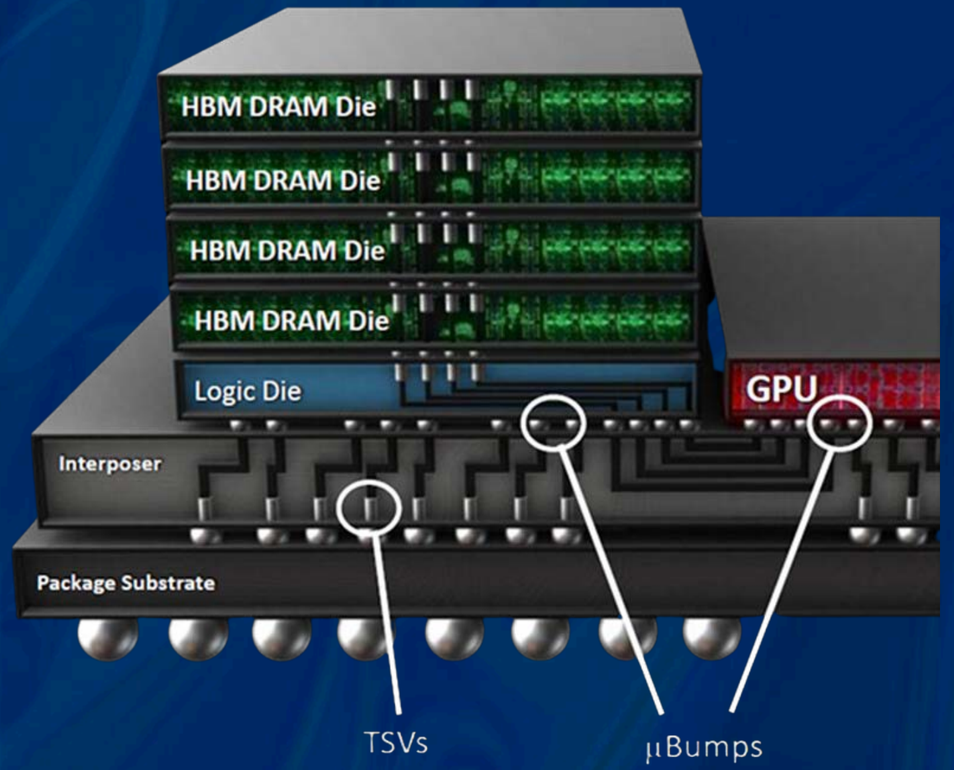
4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

Overview

- Advent of 3D “Stacked” ICs
- The Architecture of 3D ICs – HBM
- Current Testing Methods for HBM – Wafer Level Testing
- Importance of Die Level Testing
- Challenges in Testing HBMs at Die Level
- How to Perform Die Level Test for HBMs
- AMT5000 - Design Parameters & Considerations
- AMT 5000 Die Alignment Precision Measurement Method
- AMT 5000 Die Alignment Precision Test Result
- AMT5000 - Technical Capabilities
- Summary

Advent of 3D “Stacked” ICs



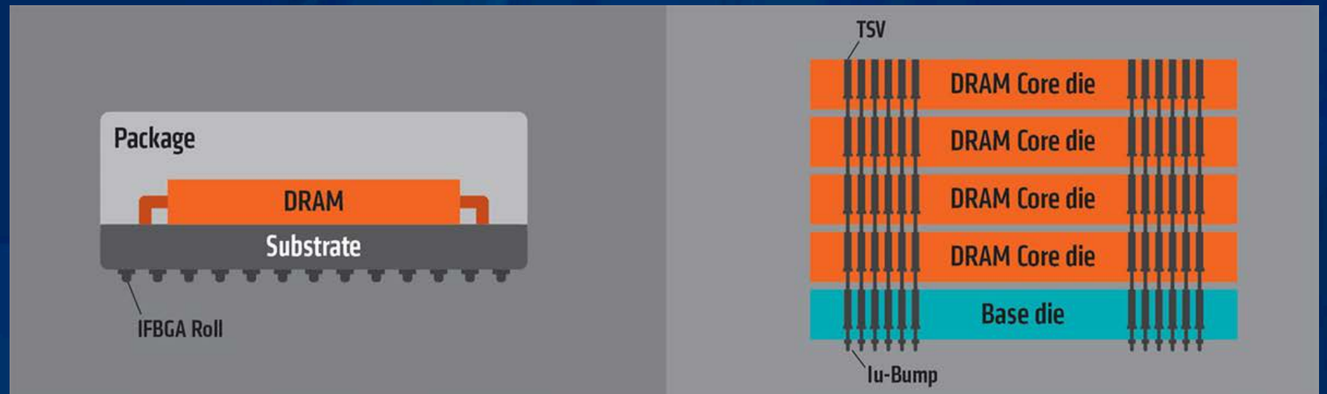


3D IC architecture is the new standard in memory chip design

An explosion of market demand for HBM chips – e.g., AI Accelerators

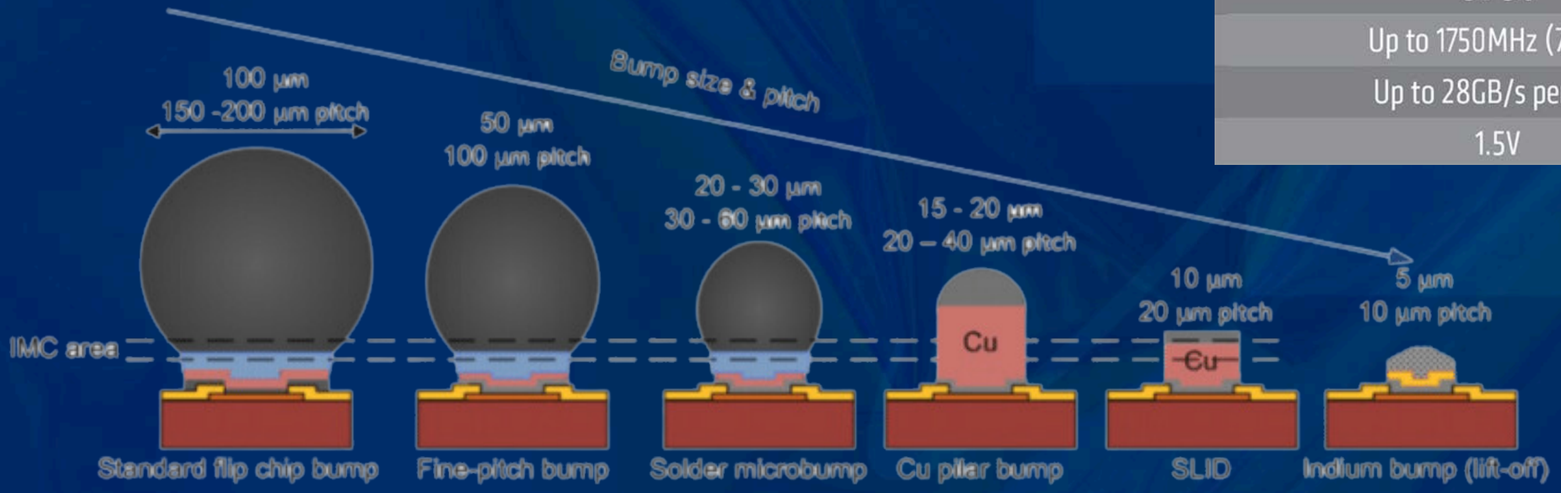
Architecture of 3D “Stacked” ICs - HBM

The “stacked” architecture necessitated ultra-fine pitch between I/O connectors.



GDDR5	Per Package	HBM
32-bit	Bus Width	1024-bit
Up to 1750MHz (7GBps)	Clock Speed	Up to 500MHz (1GBps)
Up to 28GB/s per chip	Bandwidth	>100GB/s per stack
1.5V	Voltage	1.3V

Declining size of the contact pads



32 I/O vs. 1024 I/O

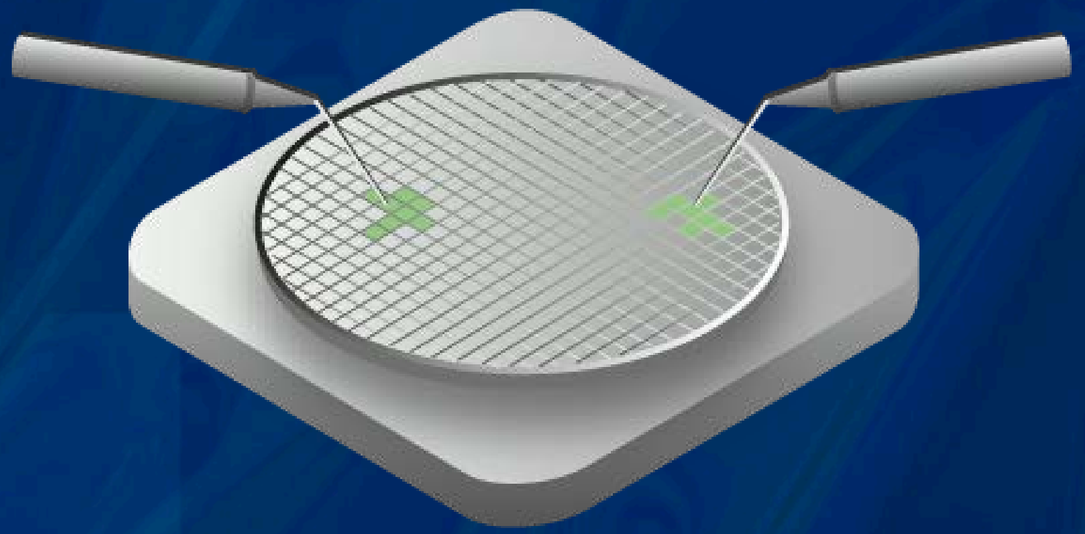
28GB vs. +100GB

Current Testing Methods for HBM

Wafer Level Probing

The small pitch between the bumps in HBM chips present a challenge for testing:

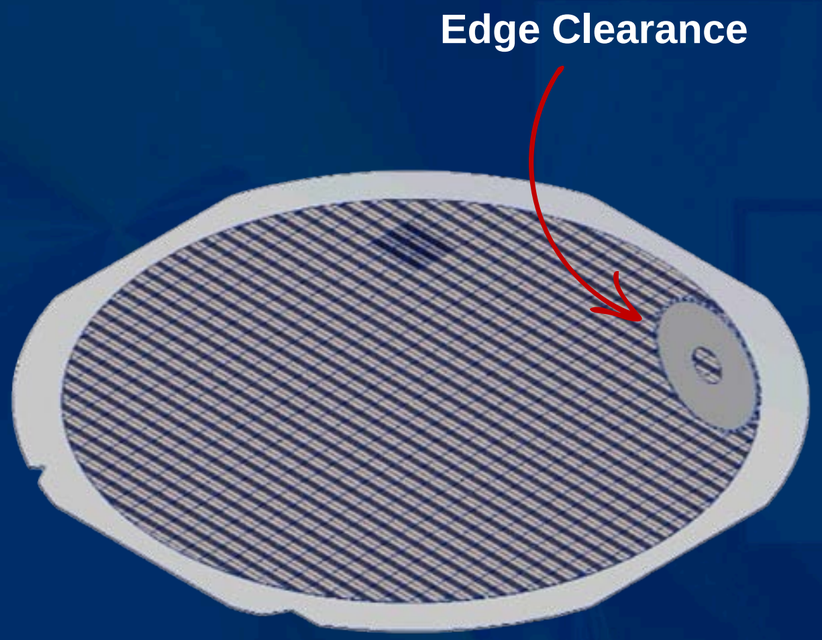
- **difficult access to individual bumps for testing**
- **increases the risk of crosstalk or interference between signals.**

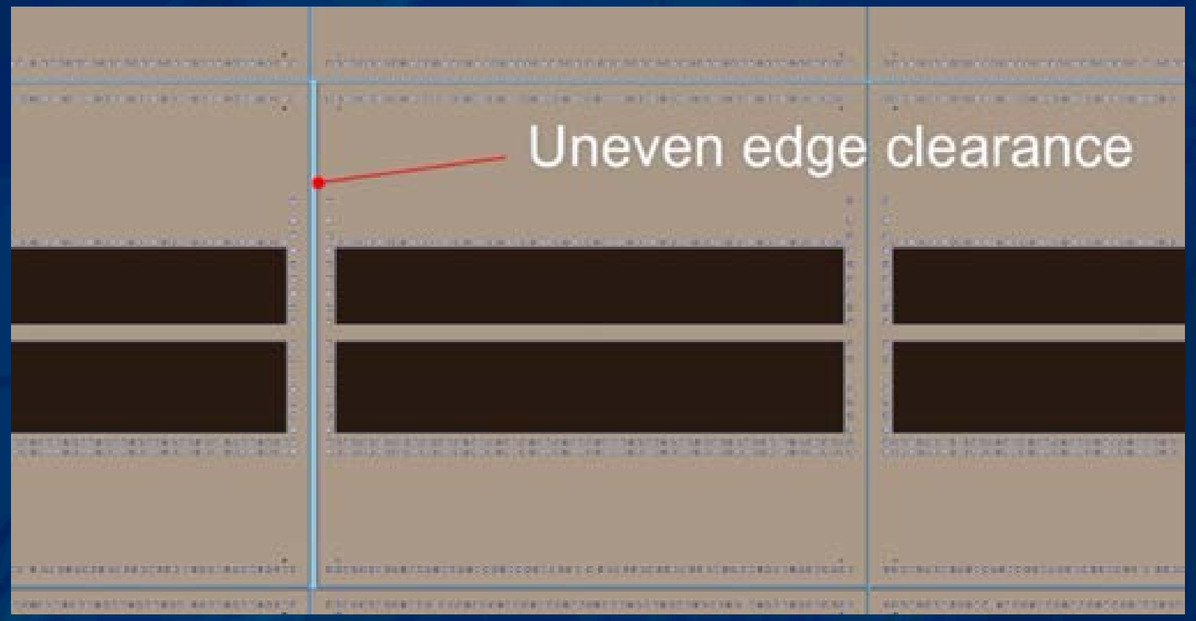


HBM chips are tested at the wafer level and shipped out without the final testing, increasing the risk of the final product being “scrapped”

Current Testing Methods for HBM

Wafer Level Probing

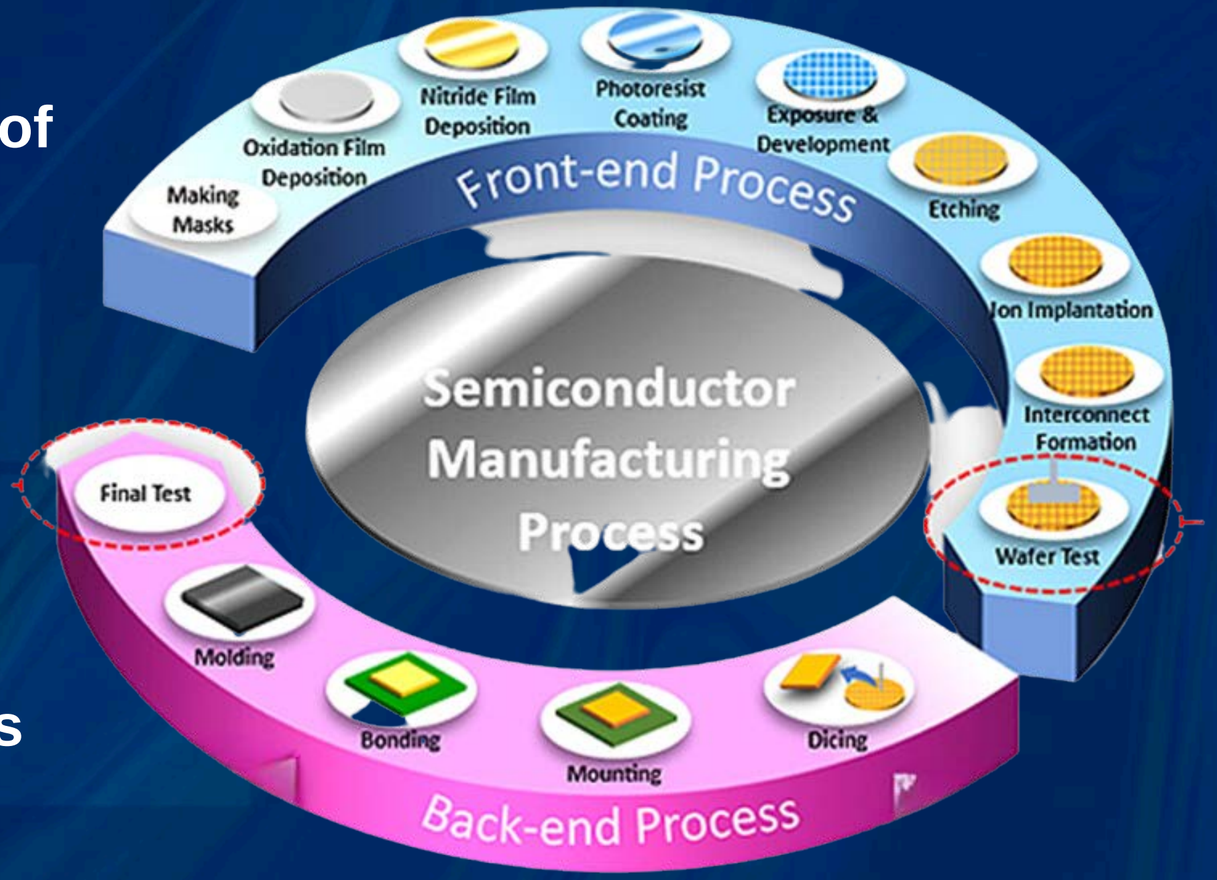




- **Sawing generated dust**
- **Cutting position errors**

Importance of Die Level Testing

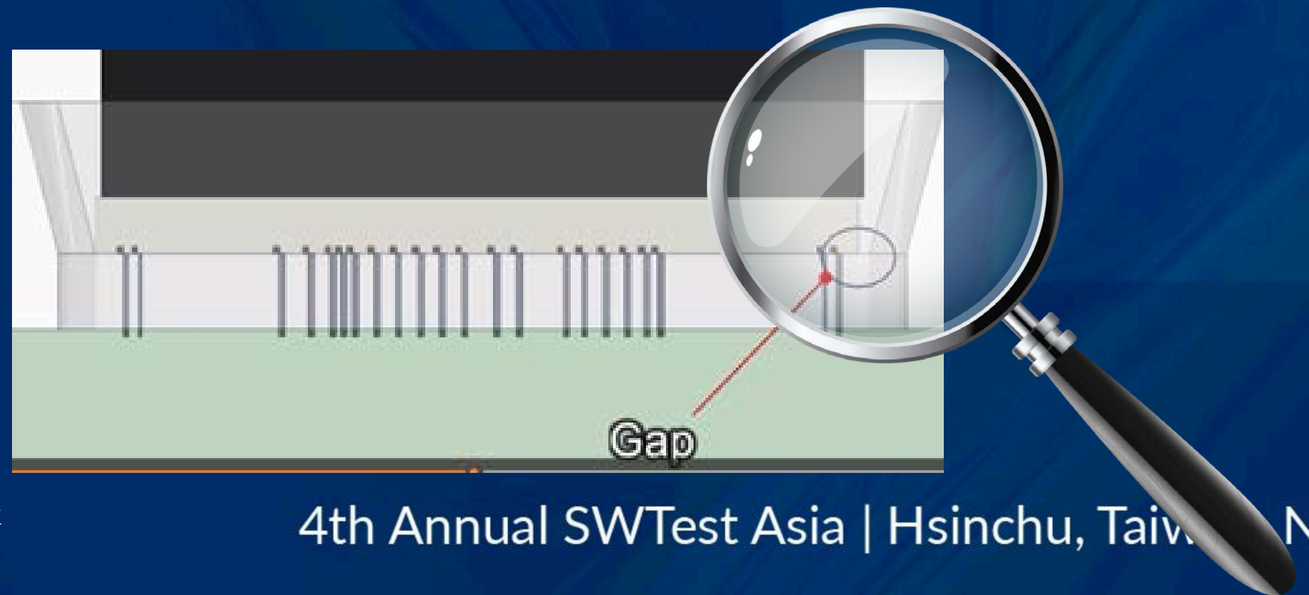
Robust KGSD testing safeguards the quality of semiconductor devices prior to packaging



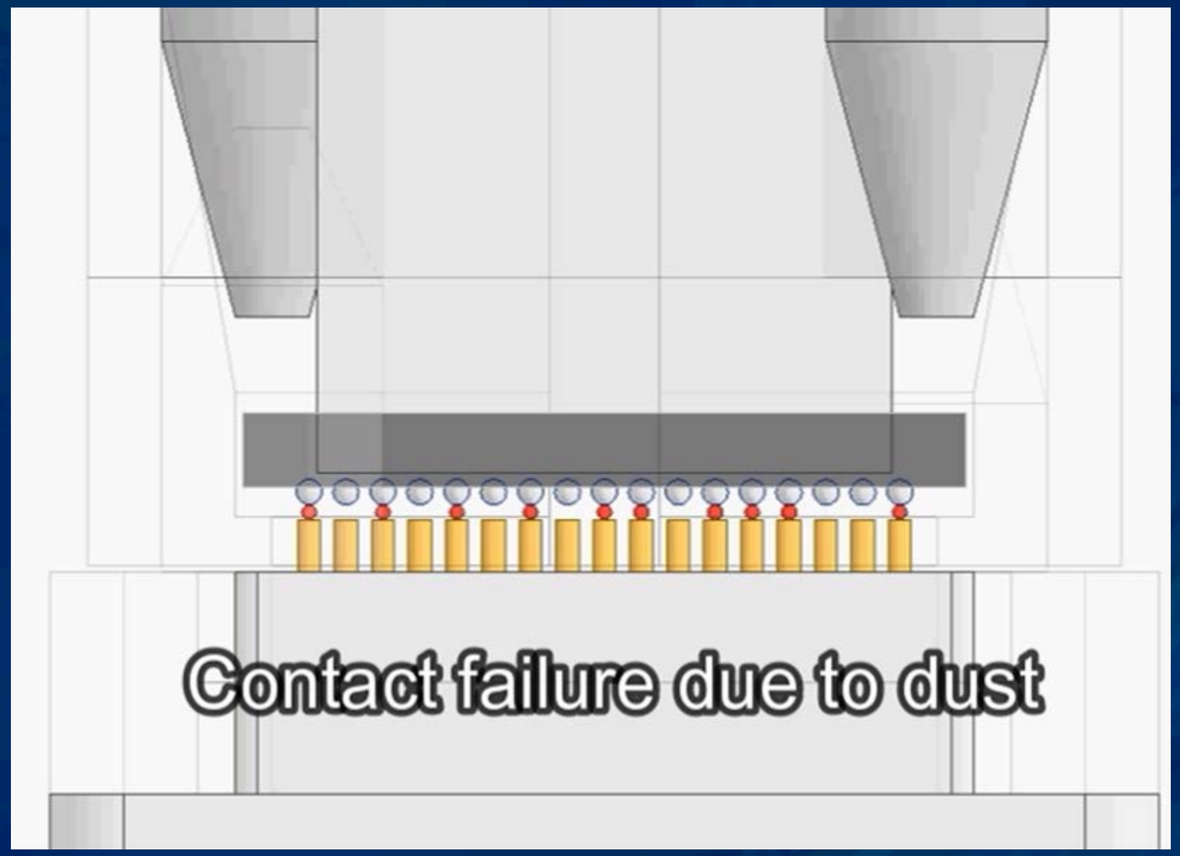
Post wafer sawing testing at die level ensures chip integrity, reduces rework, & minizes scraps

Challenges in Testing HBMs @ Die Level
Alignment Problem

- Testing requires test probes contacting I/O pins of the chips
- The small pitch between the bumps in HBM chips present a challenge for testing:
  - difficult access to individual bumps for testing
  - increases the risk of crosstalk or interference between signals.



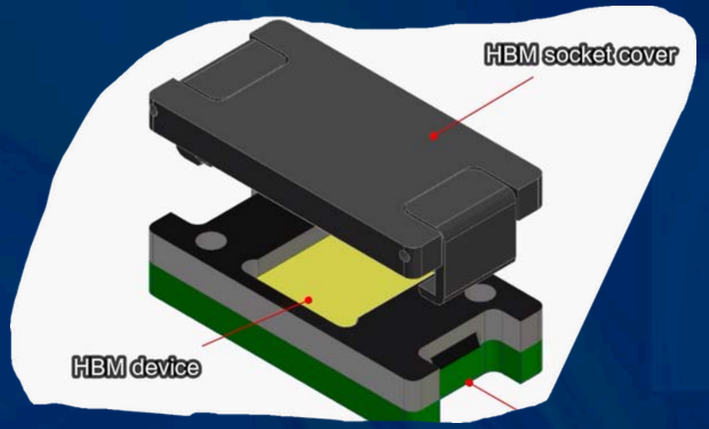
Challenges in Testing HBMs @ Die Level
Die Carrier Assisted Testing

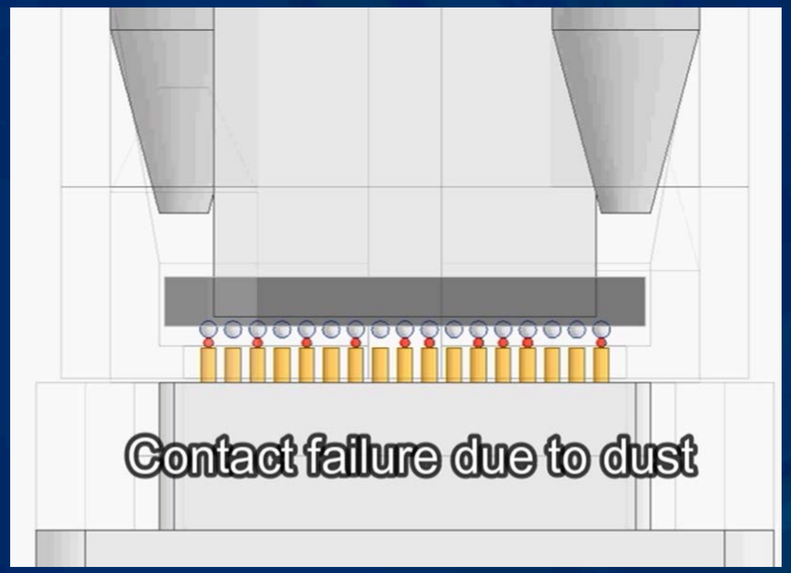


- Tri-temperature and electrical testing should be done after chip is “singulated” (i.e., cut from the wafer)
- The only alternative method of testing 3D chips at the die level is using a die-carrier, plastic housing for the chips
- Hot or Cold testing is difficult b/c die-carriers are heated or cooled in a temperature chamber- invariably introduces dust

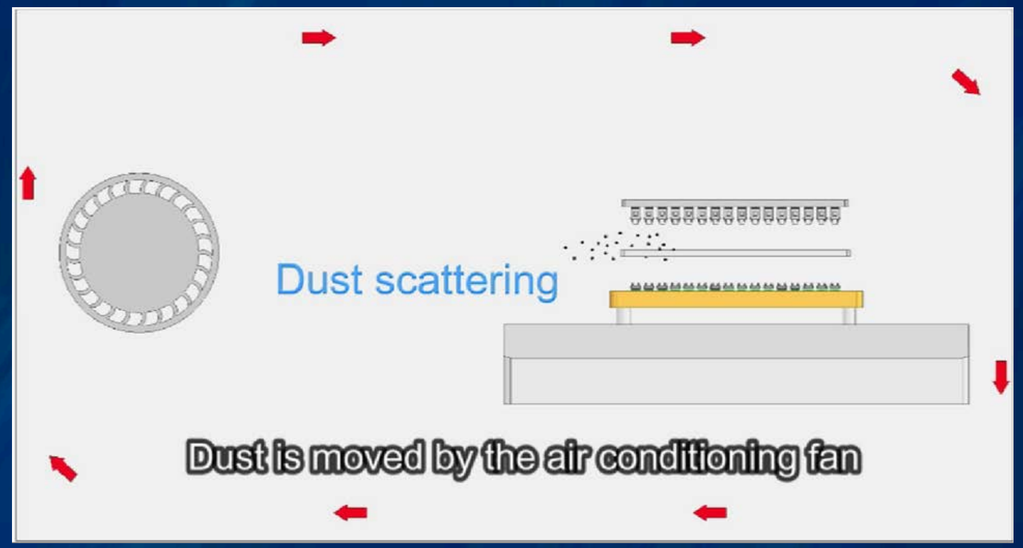
Challenges in Testing HBMs @ Die Level

Die Carrier Assisted Testing





Heating or Cooling Chamber



Hot or Cold testing is difficult b/c die-carriers are heated or cooled in a temperature chamber

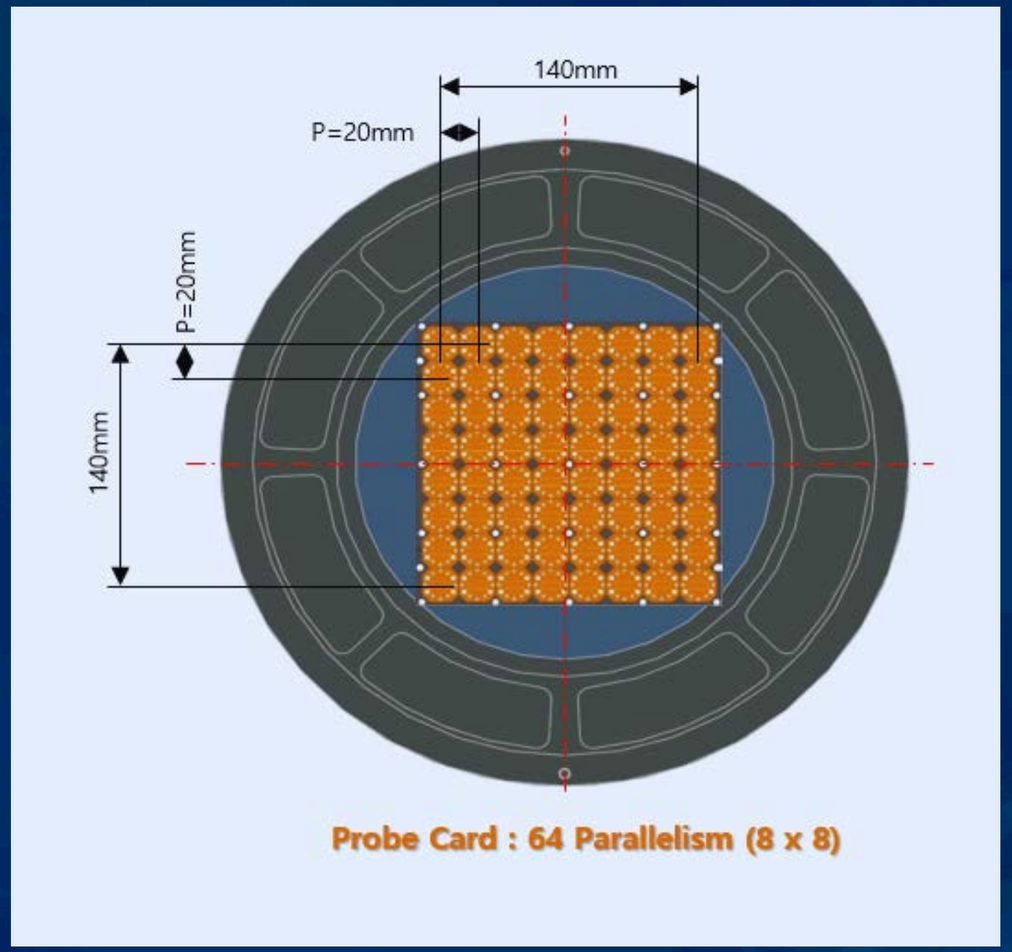
HOW TO PERFORM DIE LEVEL TEST FOR HBMs

Precision Engineering!

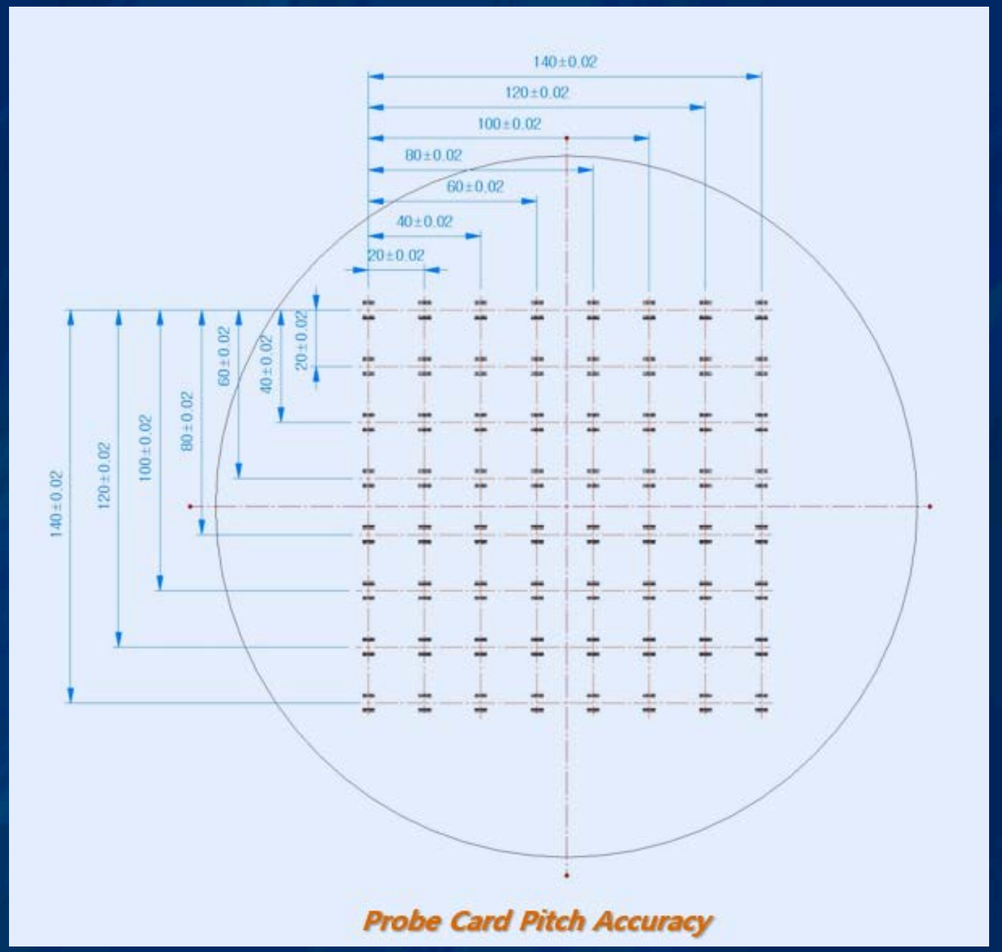
Ultra-Fine Alignment Accuracy

- **Fine Alignment: Precision probe positioning for the finest pitch size: +/- 5 micron alignment accuracy**
- **Thermal Control: Test temperature range of -45˚ C to 145˚ C**
- **High Parallelism: 64 parallel testing**
- **Versatile Device Type: HBM, BGA, WLCSP, MCP**
- **Compatibility with Existing Test Systems**

AMT5000 DESIGN CONSIDERATION & PARAMETERS

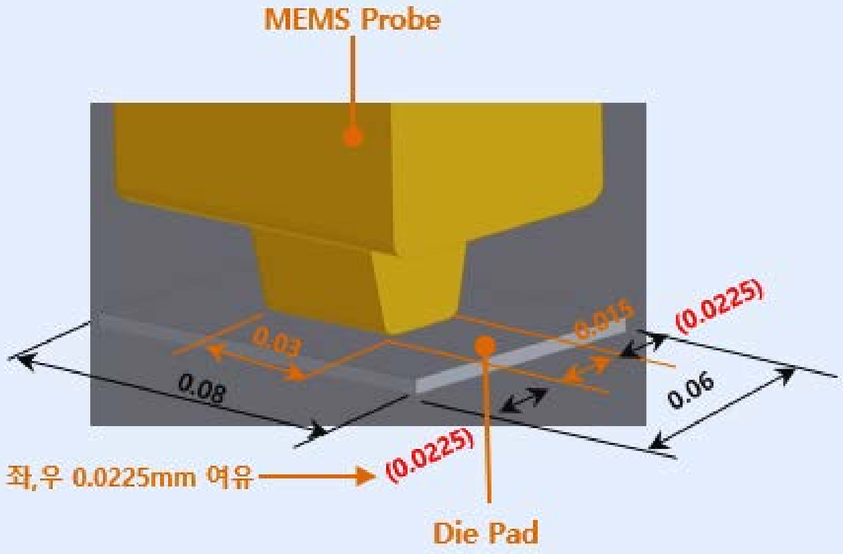


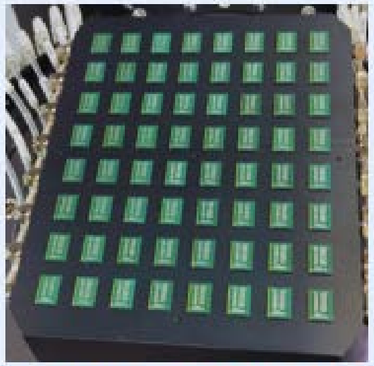
Probe Card : 64 Parallelism (8 x 8)



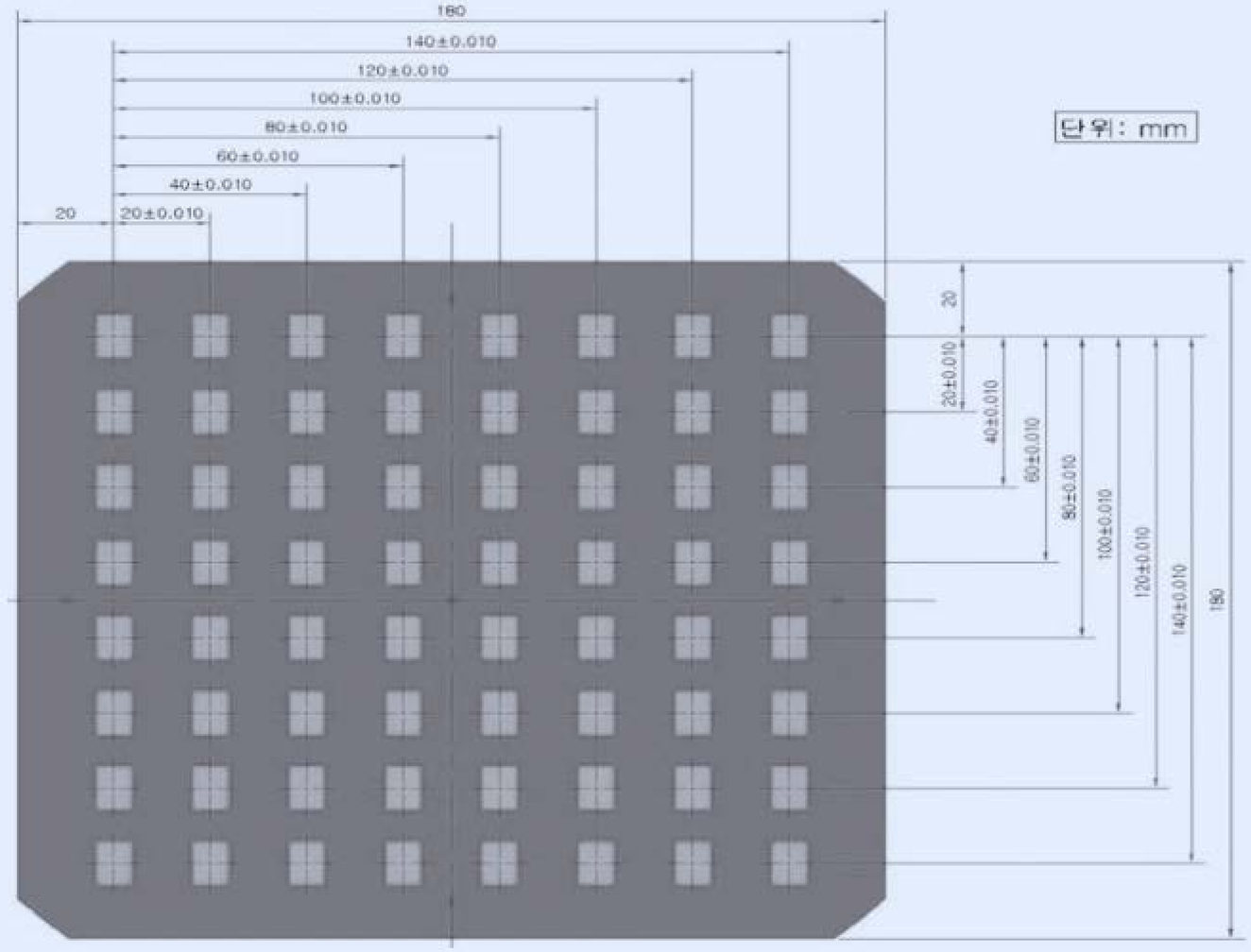
Probe Card Pitch Accuracy

AMT5000 DESIGN CONSIDERATION & PARAMETERS





Chuck Para : 64Para (8 x 8)

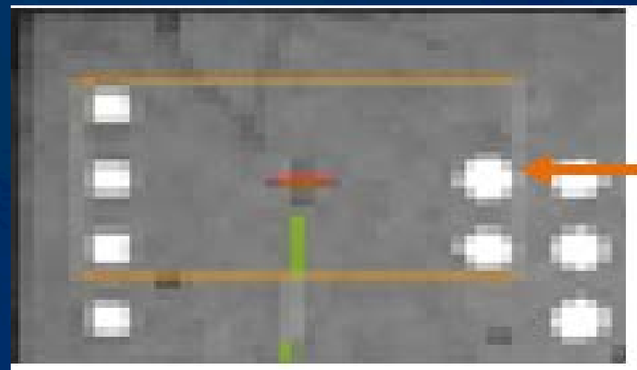


Die Alignment Accuracy

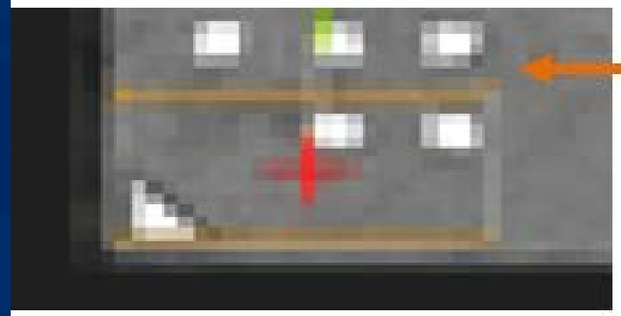
AMT 5000 DIE ALIGNMENT PRECISION MEASUREMENT METHOD

Reference Registatration	*Align the ball array of the initial material parallel to the centerline of the camera and register the upper-left and lower-left corners of the material as references for the pattern.*
Device Alignment	*Move the stage to each die position, conduct vision inspection, and compare the result data with the reference data to adjust the die position.* *Repeat this process to align all 64 dies.*
Measurement of Die Alignment	*Sequentially inspect all 64 dies using vision starting from the first material to calculate the positional error values compared to the reference data.*

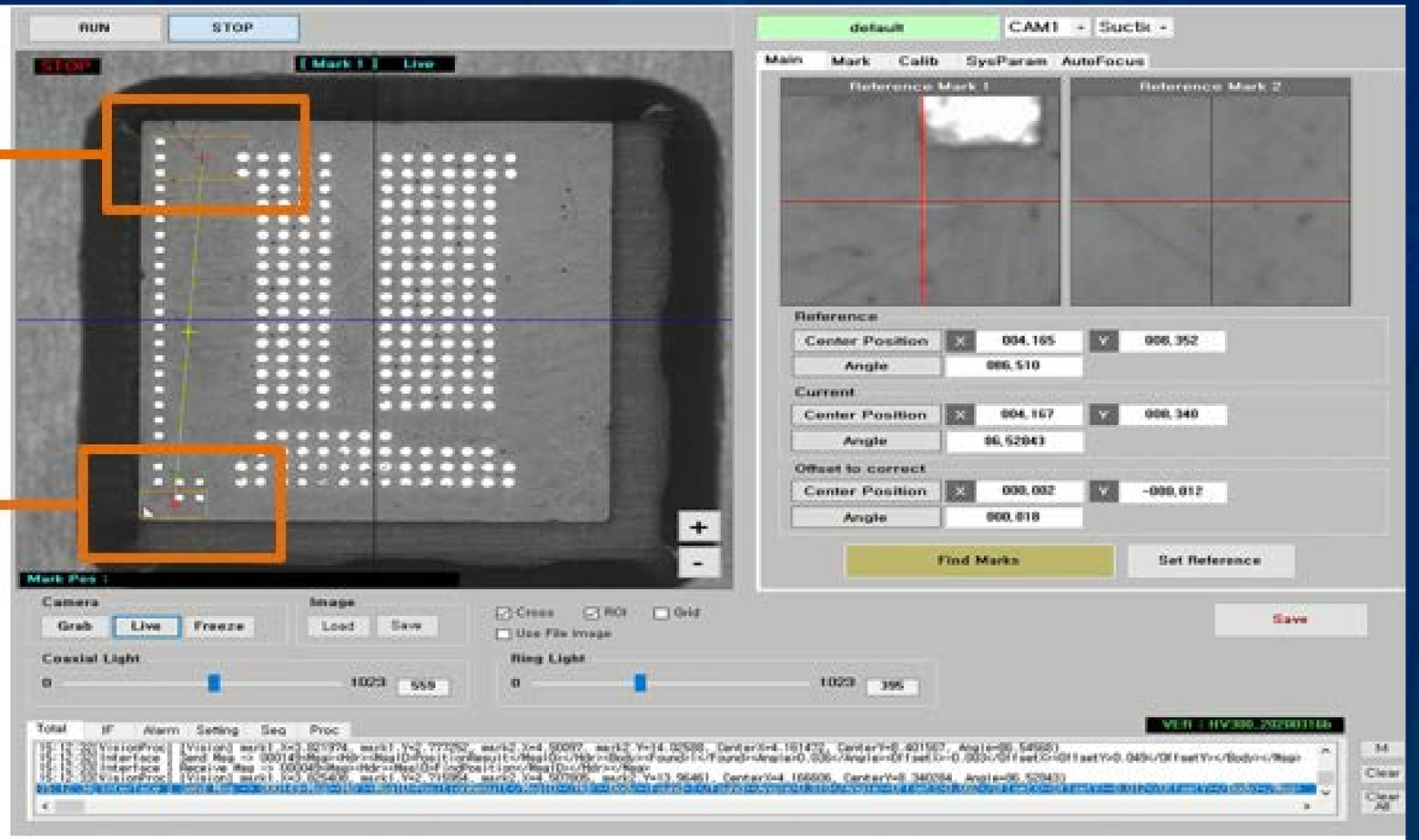
AMT 5000 DIE ALIGNMENT PRECISION MEASUREMENT METHOD



< Mark1 Image >



< Mark2 Image >



AMT 5000 DIE ALIGNMENT PRECISION TEST RESULTS

▶ [illegible] Alignment for Each Dual Stage Chip Alignment 64 Chips Completed, Position Value Measured with Vision (May 25, 2022)

▶ Chip Alignment Accuracy : ± 5㎛ (Head Base)

(Unit : mm)

Left Chuck	1		2		3		4		5		6		7		8	
	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y
1	0.003	0.000	0.003	-0.002	0.003	0.003	0.002	0.000	0.002	0.003	0.002	0.002	0.002	0.002	-0.003	0.003
2	0.005	0.002	0.005	0.002	0.002	0.003	0.003	0.000	0.002	0.002	0.002	0.002	0.000	0.002	0.000	0.000
3	0.005	0.002	0.003	0.005	0.002	0.000	0.005	-0.002	0.003	0.002	-0.002	0.003	0.005	0.002	0.002	0.002
4	0.000	0.002	0.002	0.003	0.003	0.002	0.005	0.003	0.003	0.002	0.002	0.003	0.002	0.003	-0.002	0.002
5	0.005	0.002	0.003	0.003	0.003	0.002	0.002	0.002	0.003	0.002	0.005	0.003	0.002	0.003	0.000	0.005
6	0.003	0.002	0.005	0.002	0.005	0.005	0.003	0.000	0.007	-0.002	0.002	0.005	0.005	0.002	0.002	0.003
7	0.005	0.005	0.002	0.003	0.000	0.002	0.002	0.000	0.005	0.003	0.002	0.002	0.003	0.000	0.000	0.000
8	0.002	0.003	0.002	0.003	-0.002	0.002	0.005	0.003	0.000	0.003	0.003	0.000	-0.002	0.002	0.003	0.000

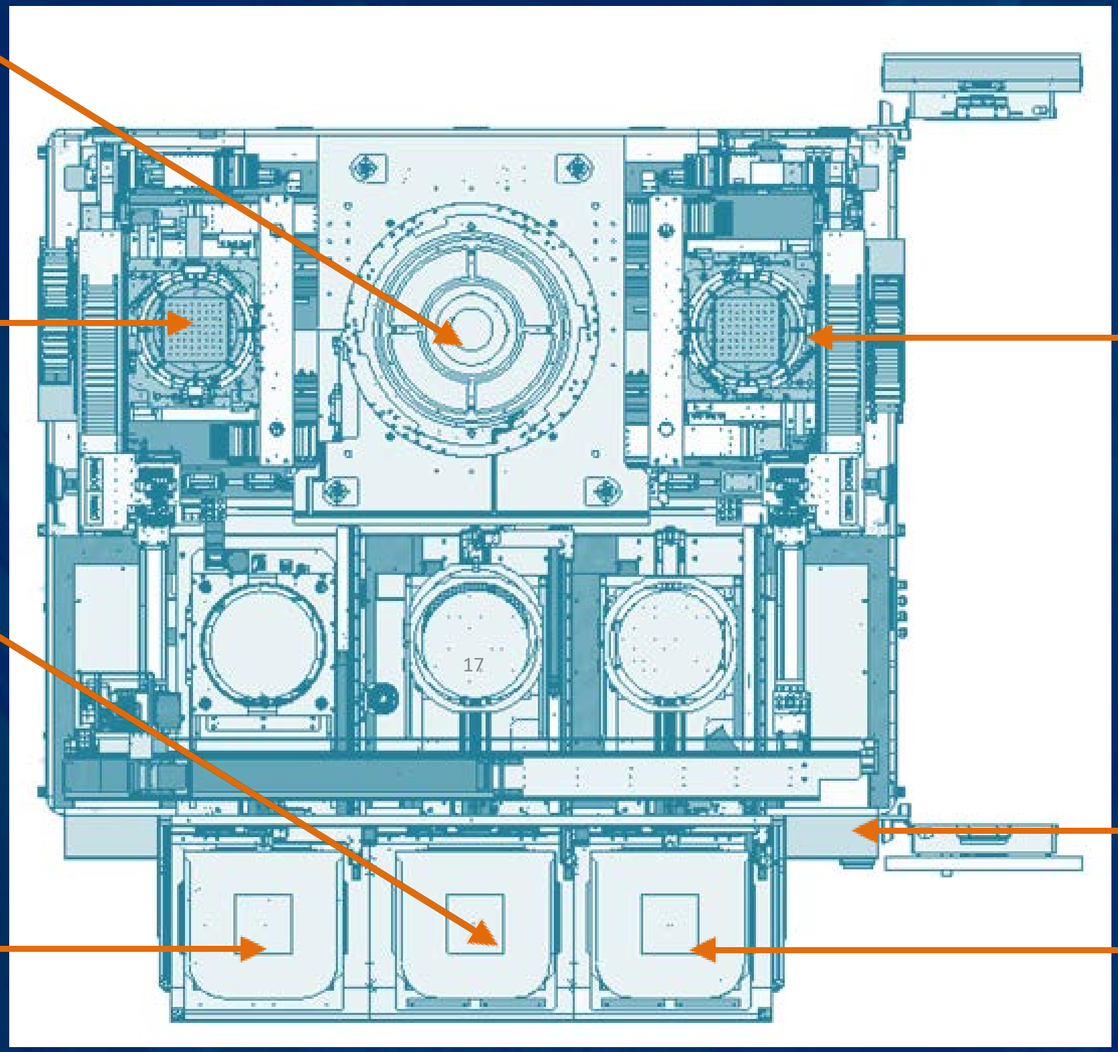
※ Measurement : X= -0.002 ~ +0.005 Y= -0.002 ~ +0.005

(Unit : mm)

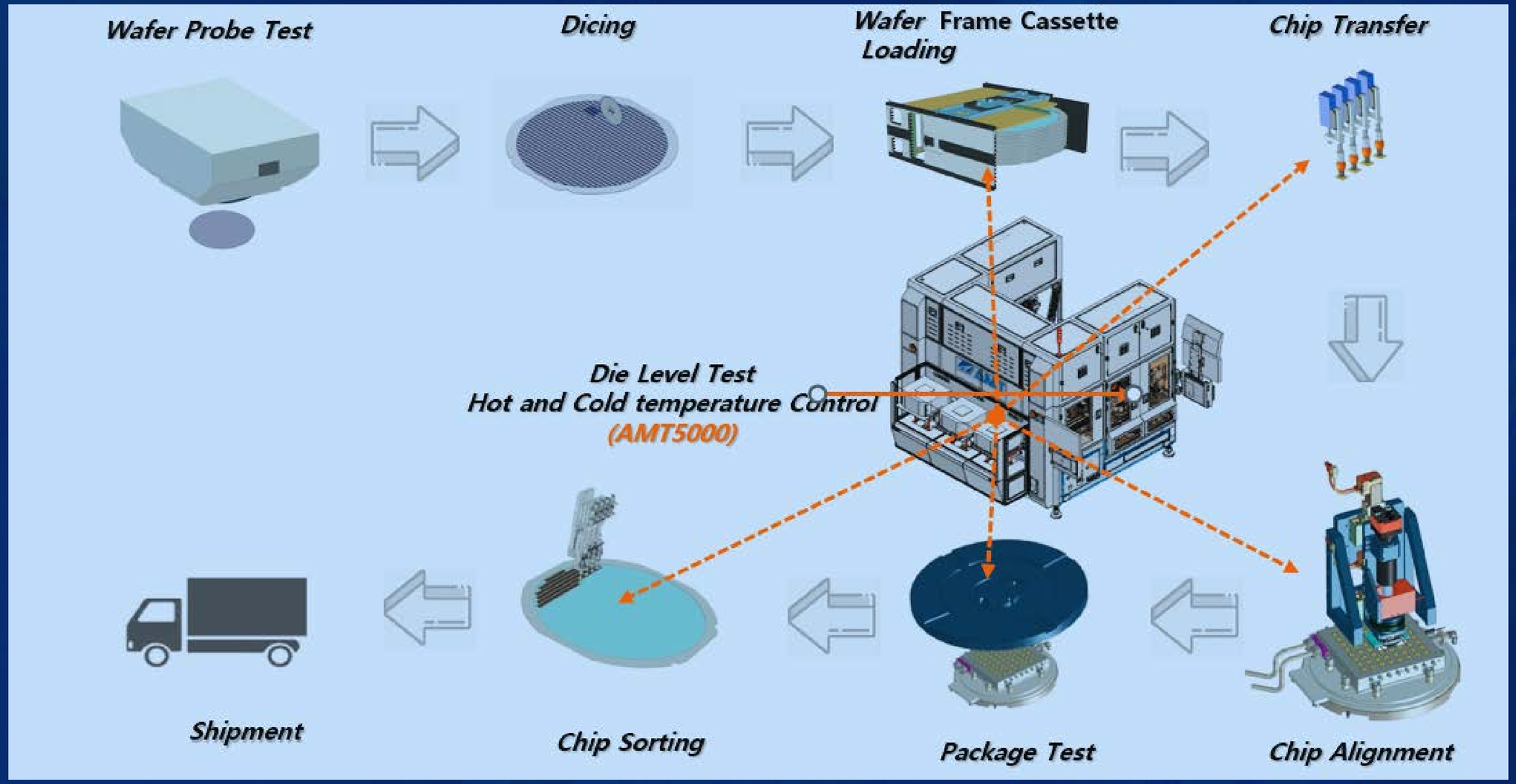
Right Chuck	1		2		3		4		5		6		7		8	
	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y
1	0.003	0.000	0.002	0.000	0.003	0.005	0.005	0.003	0.003	0.000	0.002	0.002	0.000	0.005	0.000	0.003
2	0.003	0.002	-0.002	0.005	-0.002	-0.002	0.003	-0.002	0.005	0.005	0.002	0.003	0.007	-0.002	0.005	-0.005
3	0.002	0.000	-0.002	0.000	0.007	-0.005	-0.003	-0.002	0.000	0.003	-0.002	-0.003	0.003	0.002	0.002	0.002
4	0.007	0.005	0.003	-0.002	0.005	0.000	0.007	0.003	0.003	0.000	-0.002	0.005	0.005	0.000	0.000	-0.002
5	0.007	0.005	0.005	0.000	0.002	-0.003	0.005	0.000	0.002	0.003	0.003	0.000	0.007	0.000	0.007	-0.002
6	0.003	0.003	0.000	-0.002	0.002	0.000	0.005	0.000	0.005	-0.003	0.007	0.000	0.003	0.002	0.003	0.003
7	0.003	0.002	0.002	0.002	0.003	-0.002	0.005	0.002	0.005	-0.002	0.003	-0.002	0.002	0.000	0.003	0.002
8	0.003	0.000	0.002	0.002	0.005	-0.003	0.007	-0.003	0.000	0.000	-0.002	-0.002	0.005	-0.002	0.003	0.002

※ Measurement : X= -0.003 ~ +0.005 Y= -0.005 ~ +0.005

AMT 5000 TECHNICAL CAPABILITIES



AMT 5000 TECHNICAL CAPABILITIES



AMT 5000 TECHNICAL CAPABILITIES

	Description	
Test Device	**Device Type**	**HBM**, BGA, CSP, MCP, POP, etc. Device Ball (Pad) Pitch: 120μm or above
UPH(64Para)	**Output**	711ea/Hr. (Index Time: 4Sec) ; Test Time = 320Sec
Loader & Un loader	**Wafer Ring Frame (Cassette or FOUP)**	**AMT5000** Loader One Place, Unloading Two Place (Good, Reject)
	JEDEC Tray (Stacker Type)	**AMT5400**
Test Site	**Probe Station**	Probe Card or Fine Pitch Hi-Fix Board
	Parallelism	64Para, Parallelization Scalable
	Dual Stage (X,Y,Z,θ)	Accuracy =±10μm Repeatability = ±2μm Resolution = 0.1μm Max Speed = 500mm/sec
	Loader /Un loader Picker (X,Y,Z)	Accuracy = ± 20μm Cycle Time = 1.2 sec Pick & Place Load = 1N ~ 2N 1 Head 4 Picker
	Chip Align & Vision (X,Y,Z,θ)	Accuracy = ± 0.5μm Alignment Tact Time = 320 sec/64para Chip Alignment Accuracy = ±5μm (Pad) Vision : Chip Align
	Hot & Cold Chuck (Dual)	-45°C~+145°C (±1°C)

More about AMT solutions can be seen here:

AMT HBM Test Handlerâ

- https://www.youtube.com/watch?v=hrxTY8dsUSE&t=20s
- https://www.youtube.com/watch?v=-CG8Am9uSJI
- https://www.donga.com/en/List/article/all/20230705/4268749/1

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KGD 56G PAM4 HIGH SPEED TESTING FOR DATA CENTER PRODUCT – SETUP STABILITY IMPROVEMENT AT WAFER SORT

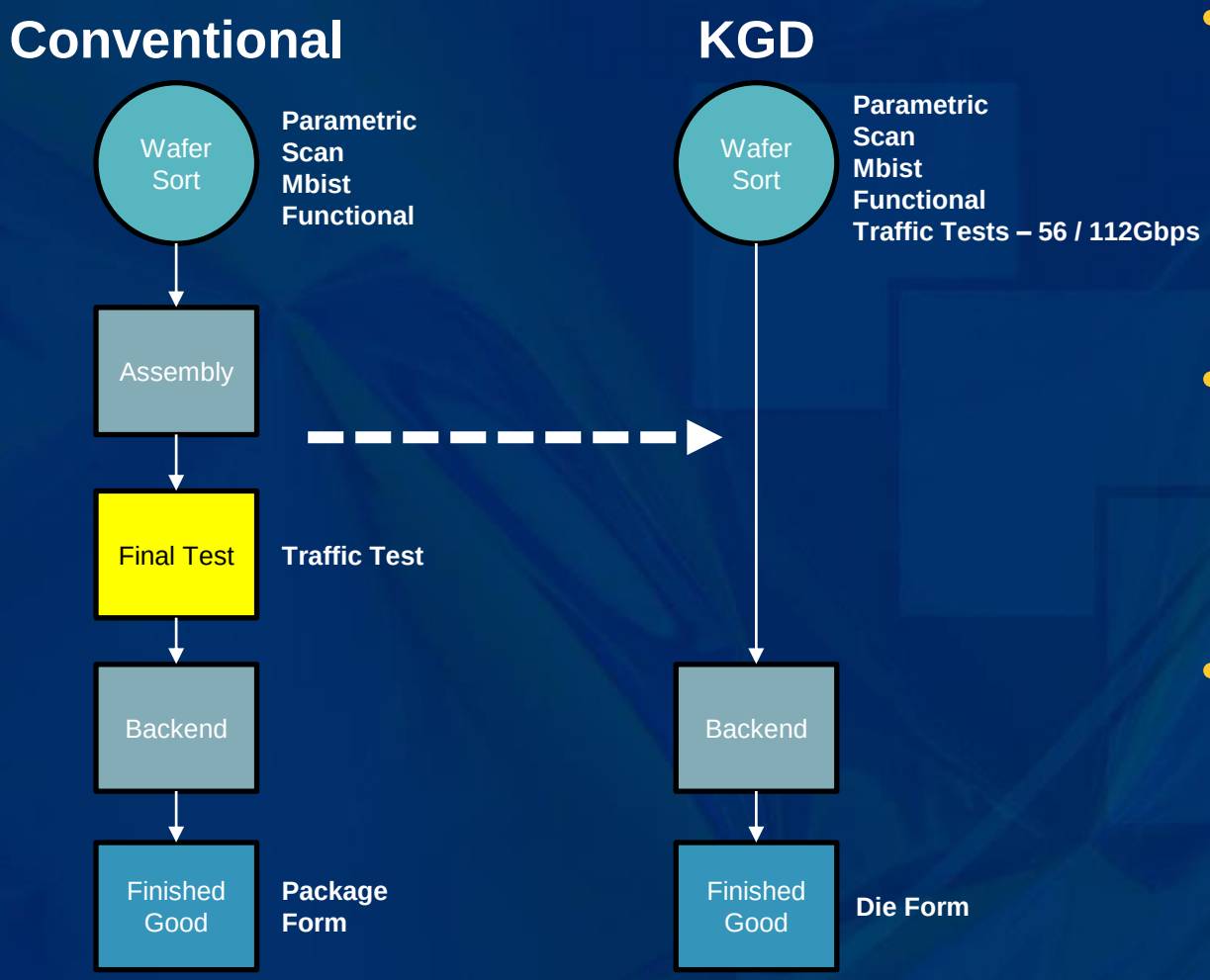
Wilson Yap
Principal Product Engineer
Marvell Technology Inc.

4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

Agenda

- Overview in Wafer Sort High Speed Testing
- KGD Testing Hardware Overview
- Manufacturing Issues and Challenges
- Resolutions and Results

Overview in WS High Speed KGD Testing



- KGD (Known Good Die) - a form factor that eliminates assembly cost; at the same time optimizes Chip on Board (COB) module assembly process
- The twinning solution (HSIO card cage + Multilane Module) was introduced to enable high speed testing in wafer sort
- Applicable to products that require high speed testing at wafer sort with limited external loopback testing capability

KGD Test Hardware Overview

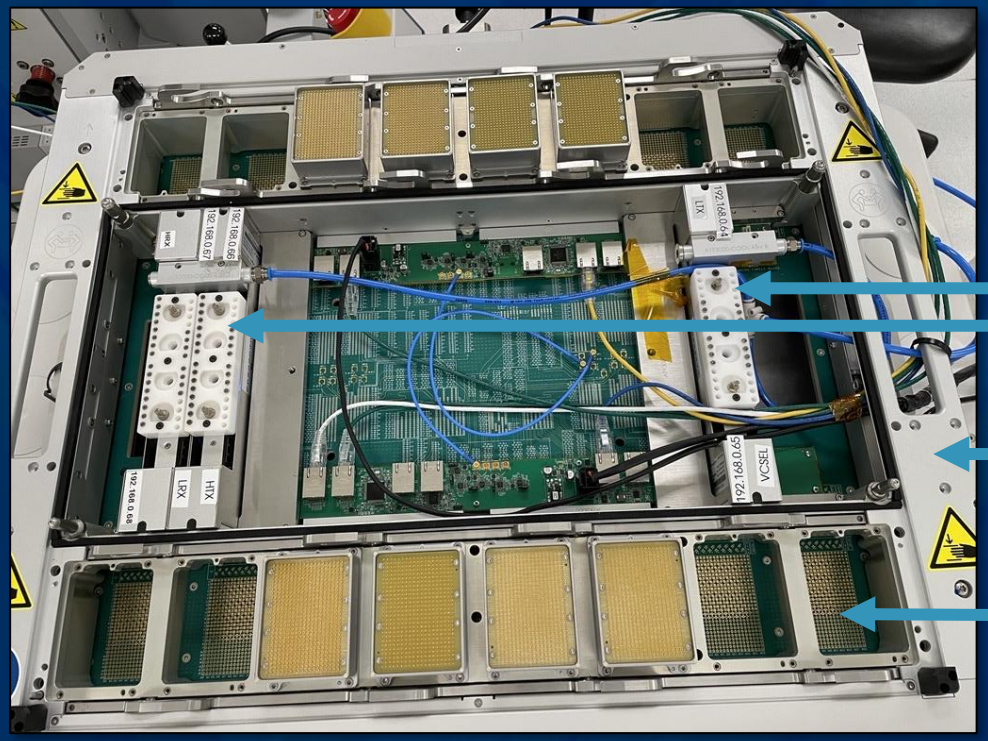
ATE
HP93K
PS1600

Prober

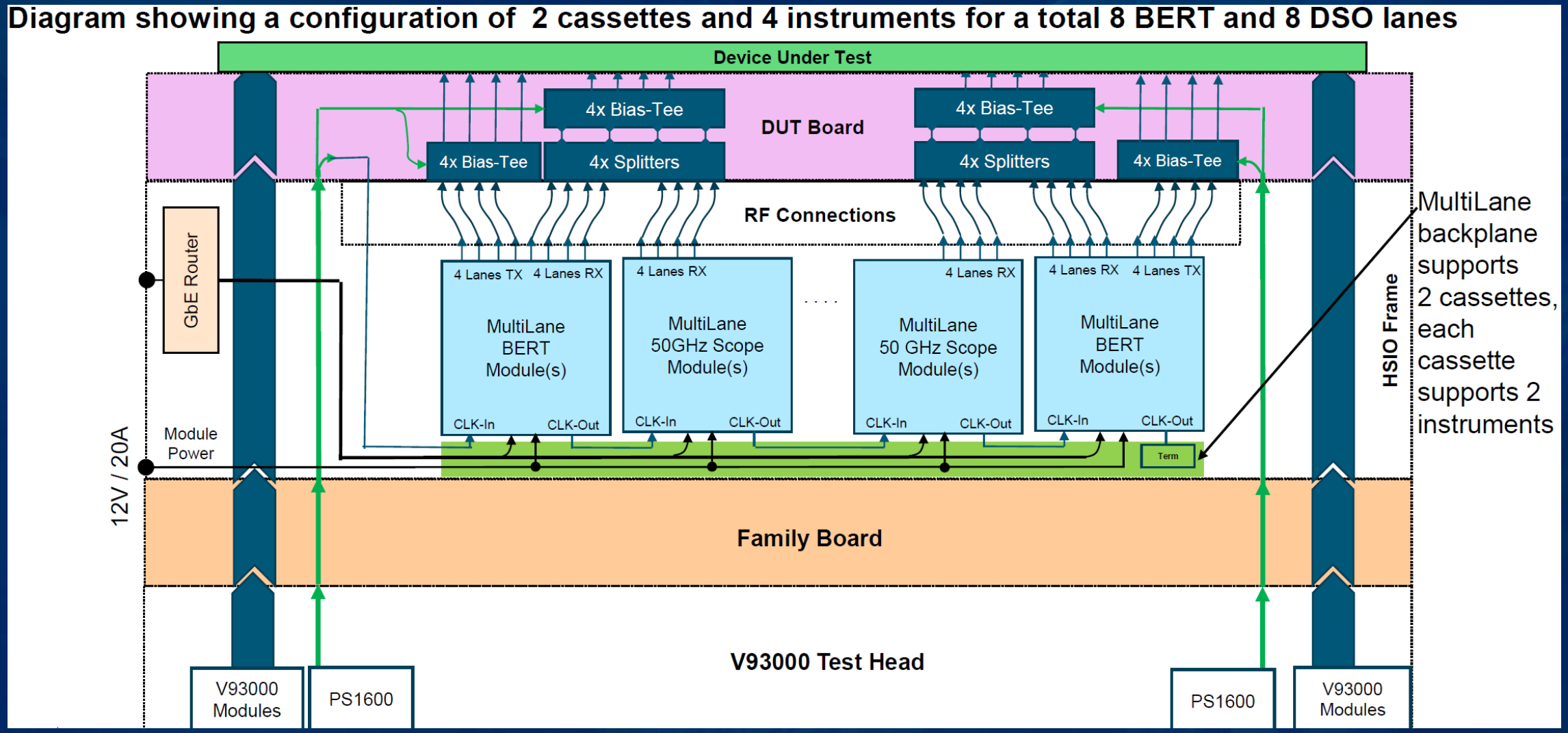
Twinning
Frame

Multilane
Modules

Probe Card



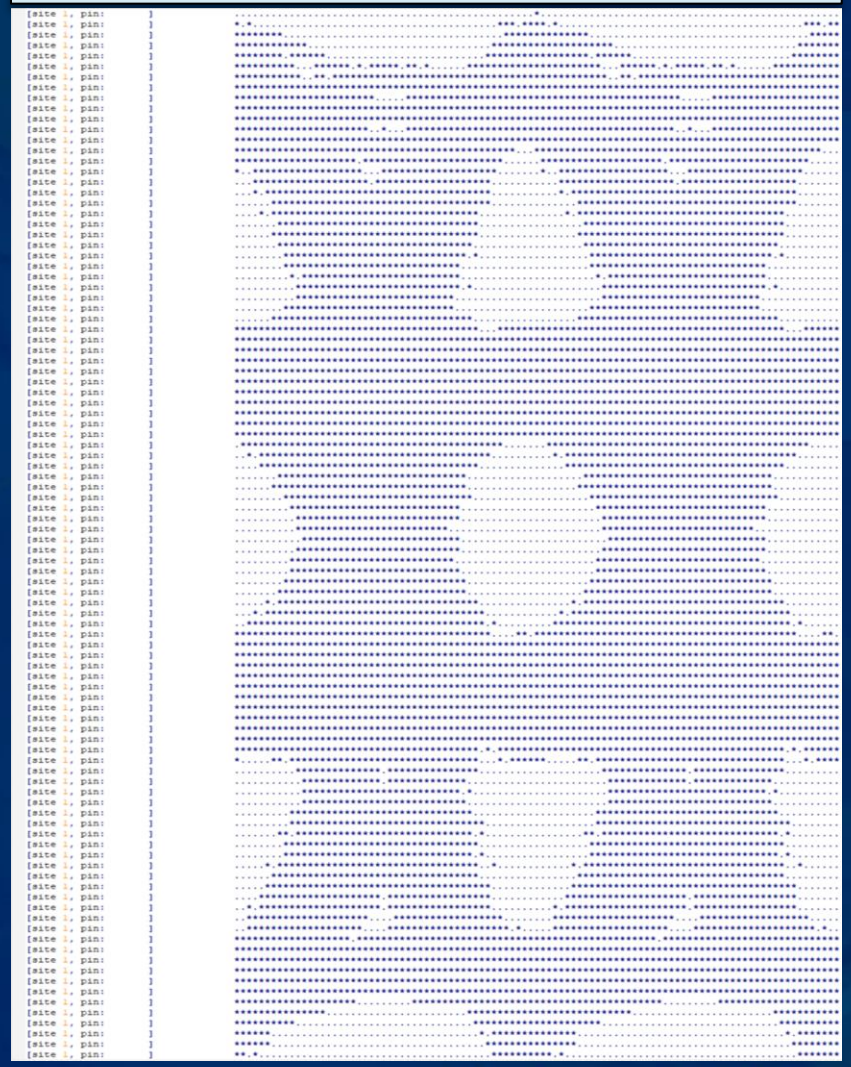
KGD High Speed Testing Configuration



Source: Advantest

ATE Output Sample

Example of Eye Diagram on ATE UI Report



Example of Output Format on ATE UI Window

```
[site 2, pin: '    '] Level2 (10)                    [mV]      :
[site 2, pin: '    '] Level3 (11)                    [mV]      :
[site 2, pin: '    '] Level1 (01)                    [mV]      :
[site 2, pin: '    '] Level0 (00)                    [mV]      :
[site 2, pin: '    '] Max                            [mV]      :
[site 2, pin: '    '] Min                            [mV]      :
[site 2, pin: '    '] Peak To Peak                   [mV]      :
[site 2, pin: '    '] Lower Eye Amplitude (AVlow)    [mV]      :
[site 2, pin: '    '] Middle Eye Amplitude (AVmid)   [mV]      :
[site 2, pin: '    '] Upper Eye Amplitude (AVupp)    [mV]      :
[site 2, pin: '    '] VEC                            [mV]      :
[site 2, pin: '    '] Lower Eye Height (Vlow)        [mV]      :
[site 2, pin: '    '] Lower Eye Top (VlowTop)        [mV]      :
[site 2, pin: '    '] Lower Eye Base (VlowBase)      [mV]      :
[site 2, pin: '    '] Middle Eye height (Vmid)       [mV]      :
[site 2, pin: '    '] Middle Eye Top (VmidTop)       [mV]      :
[site 2, pin: '    '] Middle Eye Base (VmidBase)     [mV]      :
[site 2, pin: '    '] Upper Eye Height (Vupp)        [mV]      :
[site 2, pin: '    '] Upper Eye Top (VuppTop)        [mV]      :
[site 2, pin: '    '] Upper Eye Base (VuppBase)      [mV]      :
[site 2, pin: '    '] Lower Eye Width (Hlow)         [ps]      :
[site 2, pin: '    '] Middle Eye Width (Hmid)        [ps]      :
[site 2, pin: '    '] Upper Eye Width (Hupp)         [ps]      :
[site 2, pin: '    '] Lower Eye skew (LowEyeSkew)    [ps]      :
[site 2, pin: '    '] Middle Eye skew (MidEyeSkew)   [ps]      :
[site 2, pin: '    '] Upper Eye skew (UpperEyeSkew)  [ps]      :
[site 2, pin: '    '] Vrms                           [mV]      :
```

- The communications between ATE and Multilane Modules were established via the LAN
- Customized library was used
- Measurement results were logged, and the eye diagram can be displayed over the UI window

Manufacturing Challenges – High Speed Sort

4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

Manufacturing Challenges – High Speed Sort

Setup Stability

Manufacturing Challenges – High Speed Sort

Setup Stability

Probe Card Technology

Manufacturing Challenges – High Speed Sort

Setup Stability

- Full system setup involves multiple vendors
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Probe Card Technology

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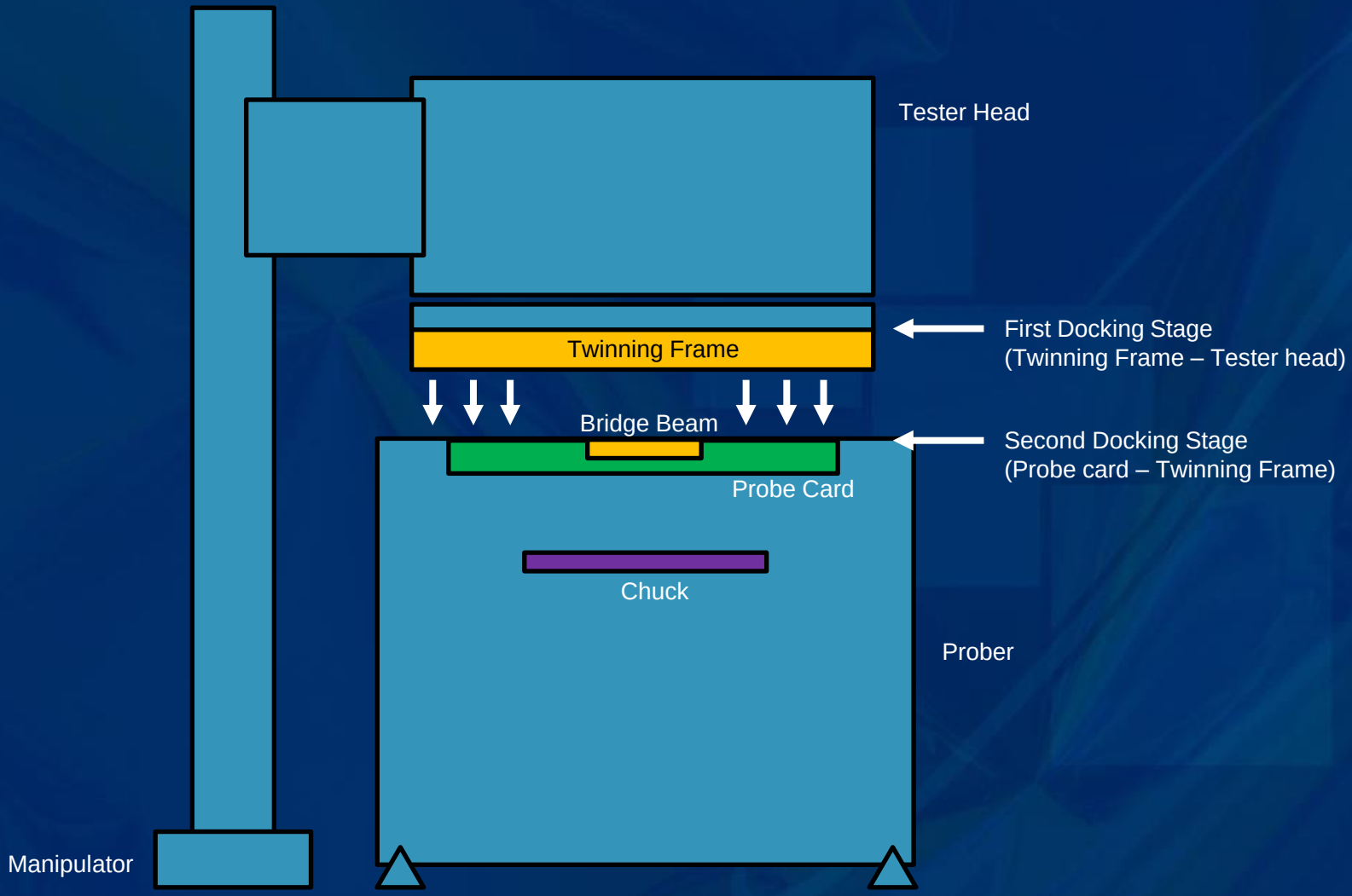
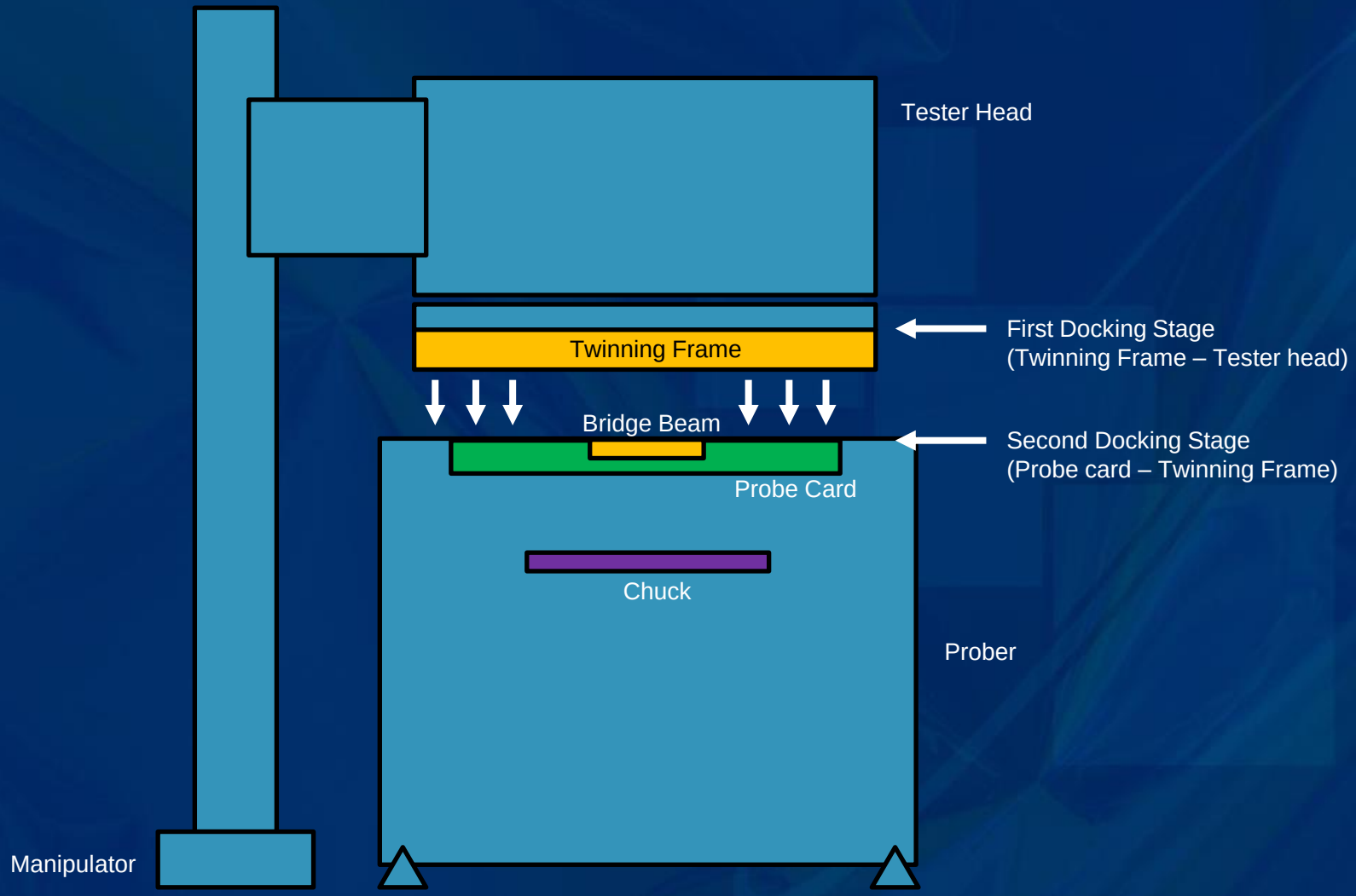
Probe Card Technology

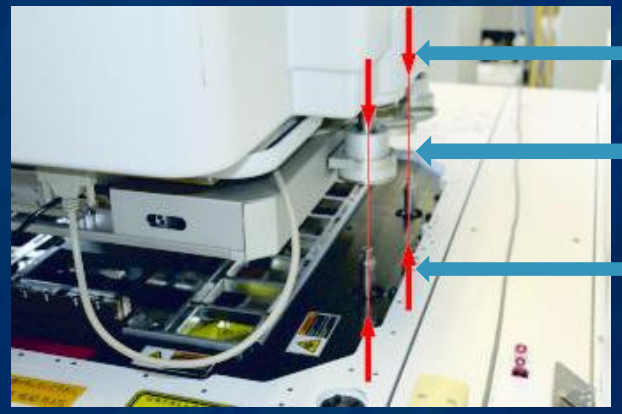
- Light / weak probe marks on RF pins
- Probe mark uniformity issue
- IR drop induced failures
- Low yield after “x” touchdown

KGD Wafer Sort Setup - Twinning Frame



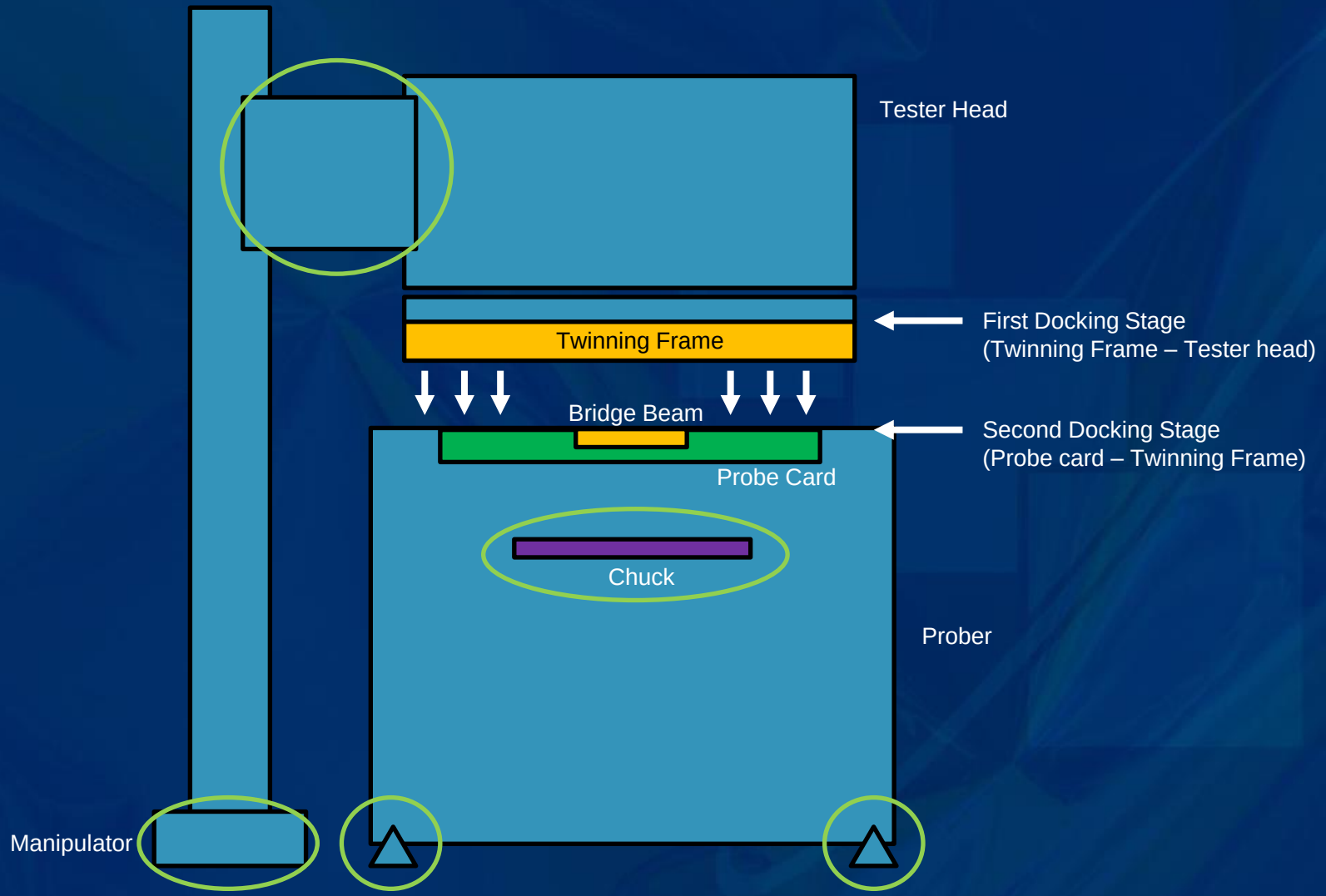
KGD Wafer Sort Setup - Twinning Frame

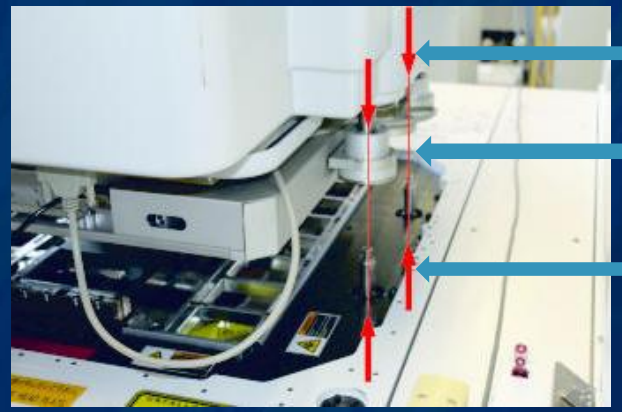




Source: Advantest

KGD Wafer Sort Setup - Twinning Frame





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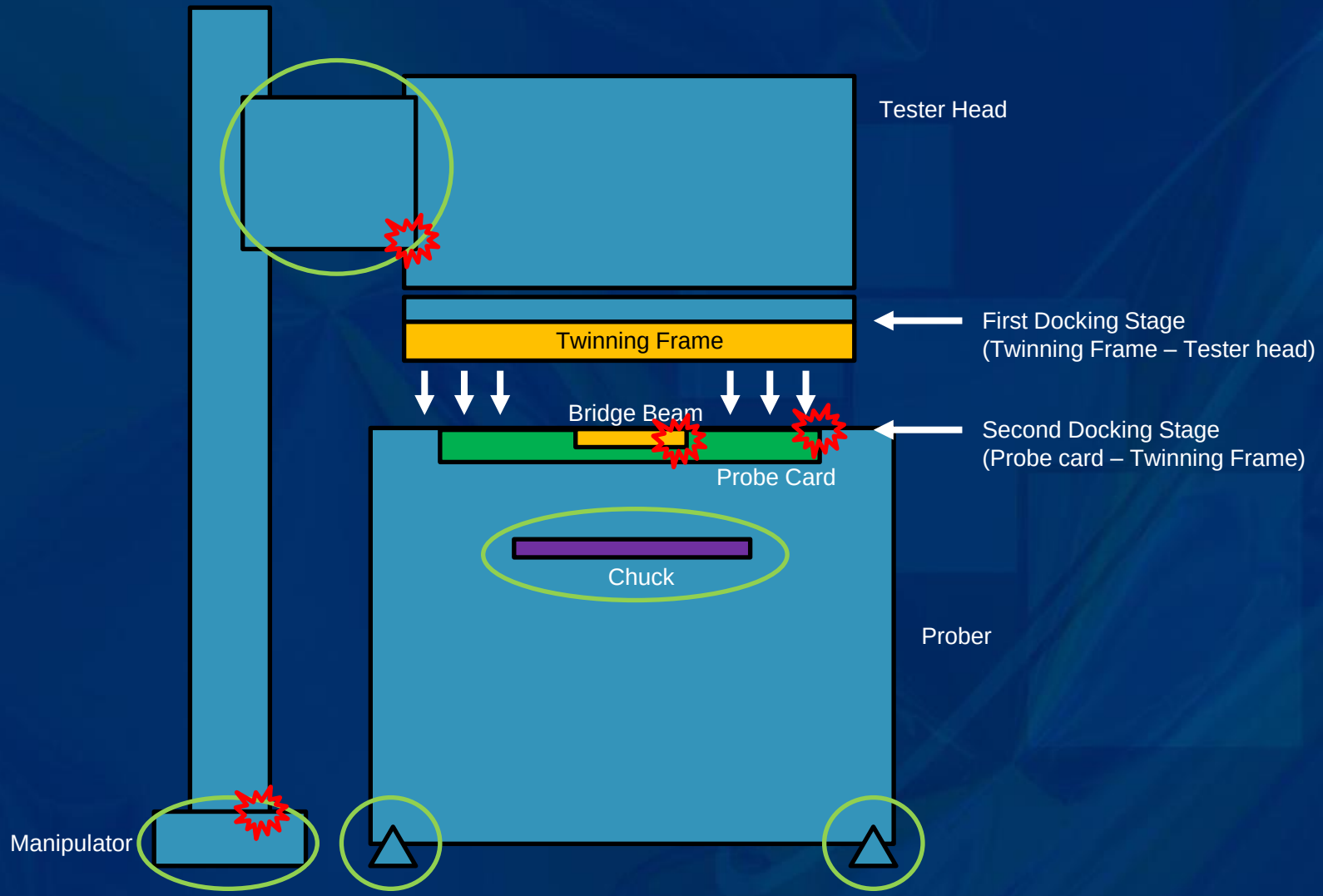
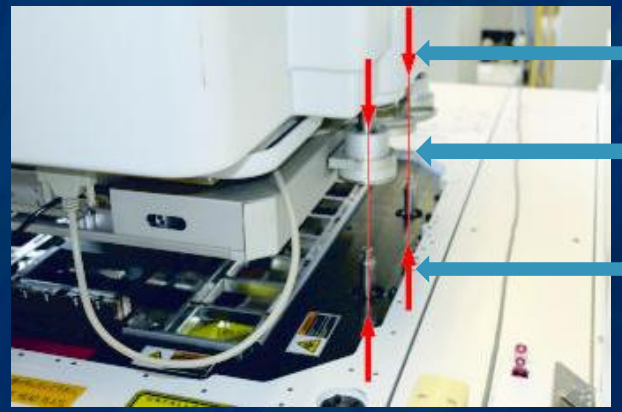
KGD Wafer Sort Setup - Twinning Frame





Source: Advantest

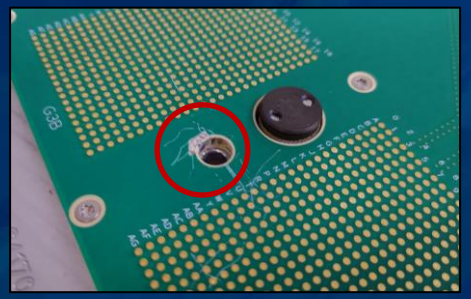
Setup Planarization Issue – Example of Failure

Poor Planarity After Docking

Hardware Damages:

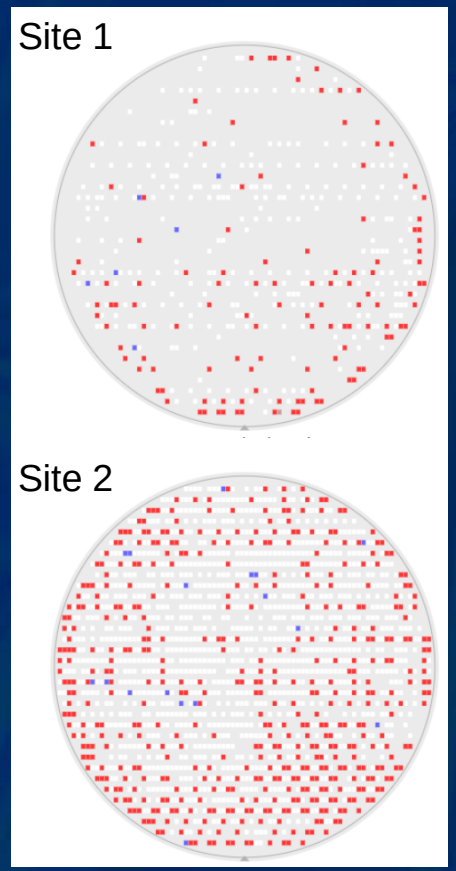
Probe Card Stuck

Damaged SMPM Connectors



Damaged Probe Card

Low Yield & High Site-to Site Variation



Setup Planarization Issue Overview

Before Docking

- Prober / Chuck Planarization
- Tester Head Leveling
- Tester Manipulator Adjustment

Setup Planarization Issue Overview

Before Docking

Prober / Chuck Planarization

Tester Head Leveling

Tester Manipulator Adjustment

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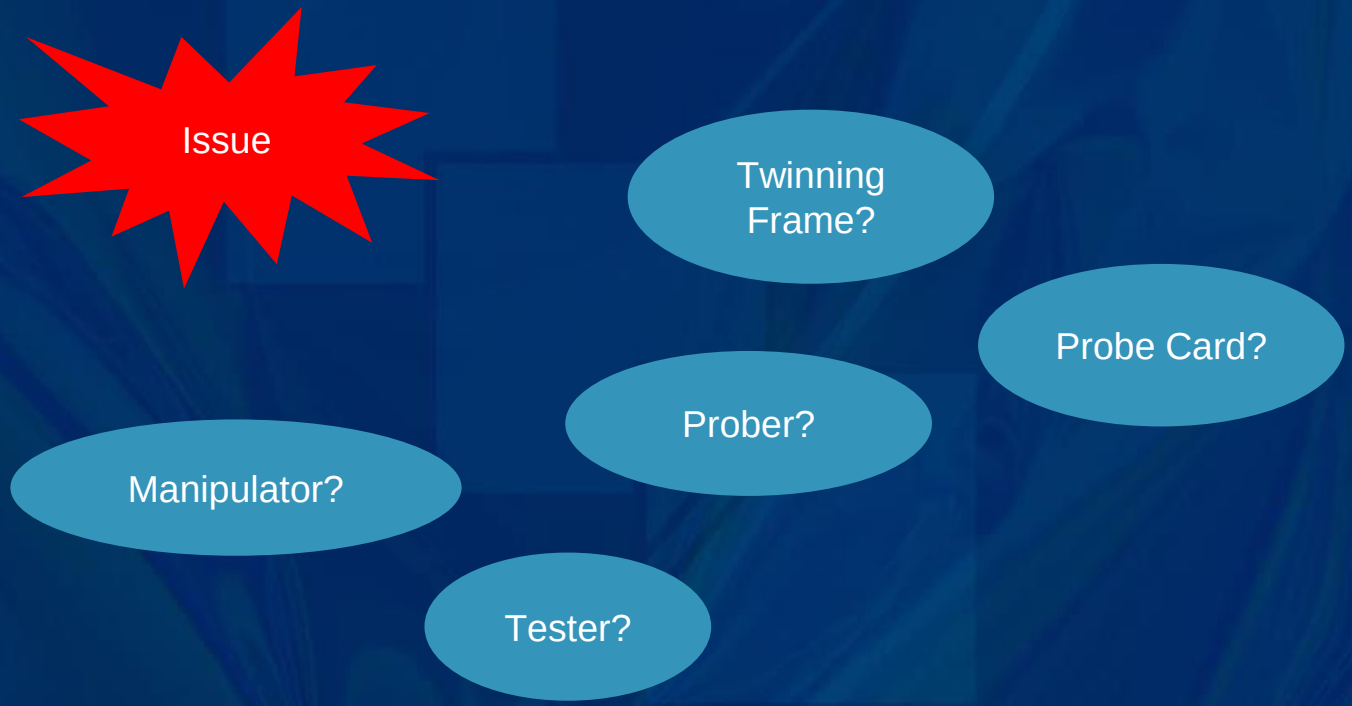

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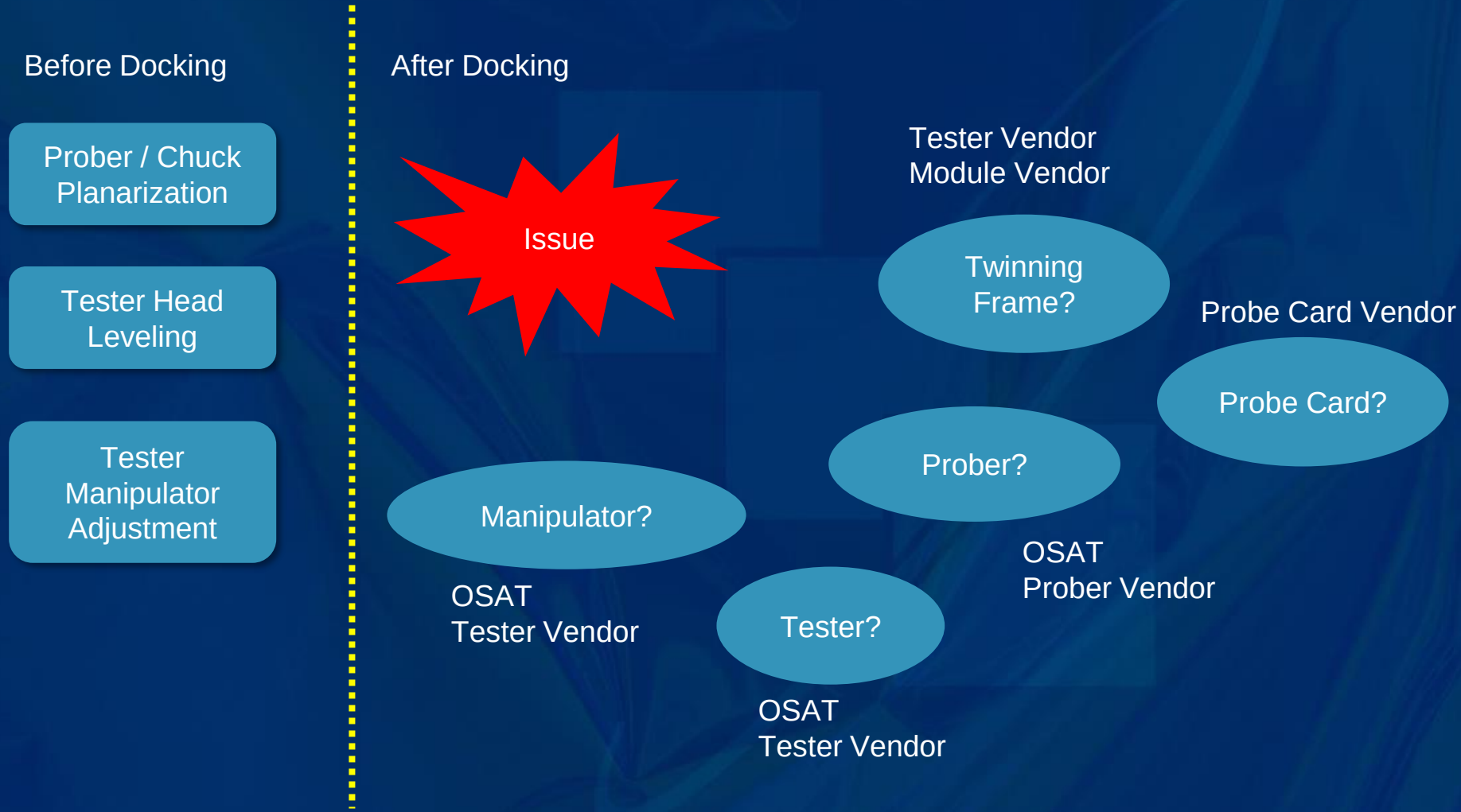

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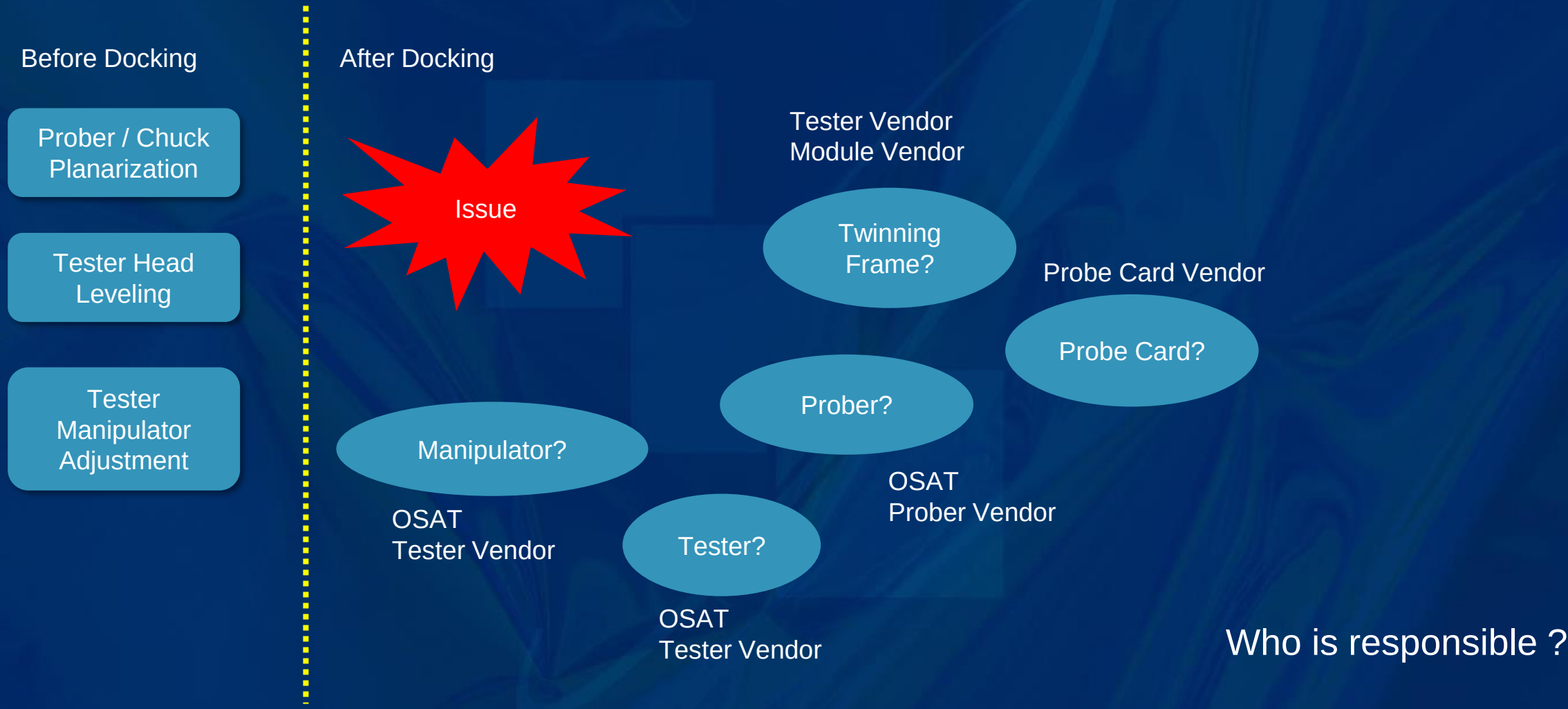

Who is responsible ?

Setup Planarization Issue Resolution

Before Docking

- Prober Planarization
- Tester Head Leveling
- Tester Manipulator Adjustment

Setup Planarization Issue Resolution

Before Docking

- Prober Planarization
- Tester Head Leveling
- Tester Manipulator Adjustment
- Unlock Tester Head
- Guide Pins Height Standardization

Setup Planarization Issue Resolution

Before Docking

Prober Planarization

Tester Head Leveling

Tester Manipulator Adjustment

Unlock Tester Head

Guide Pins Height Standardization

After Docking

Setup Planarization Issue Resolution

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After Docking

- VPG
- Probe Card loading SOP

Setup Planarization Issue Resolution

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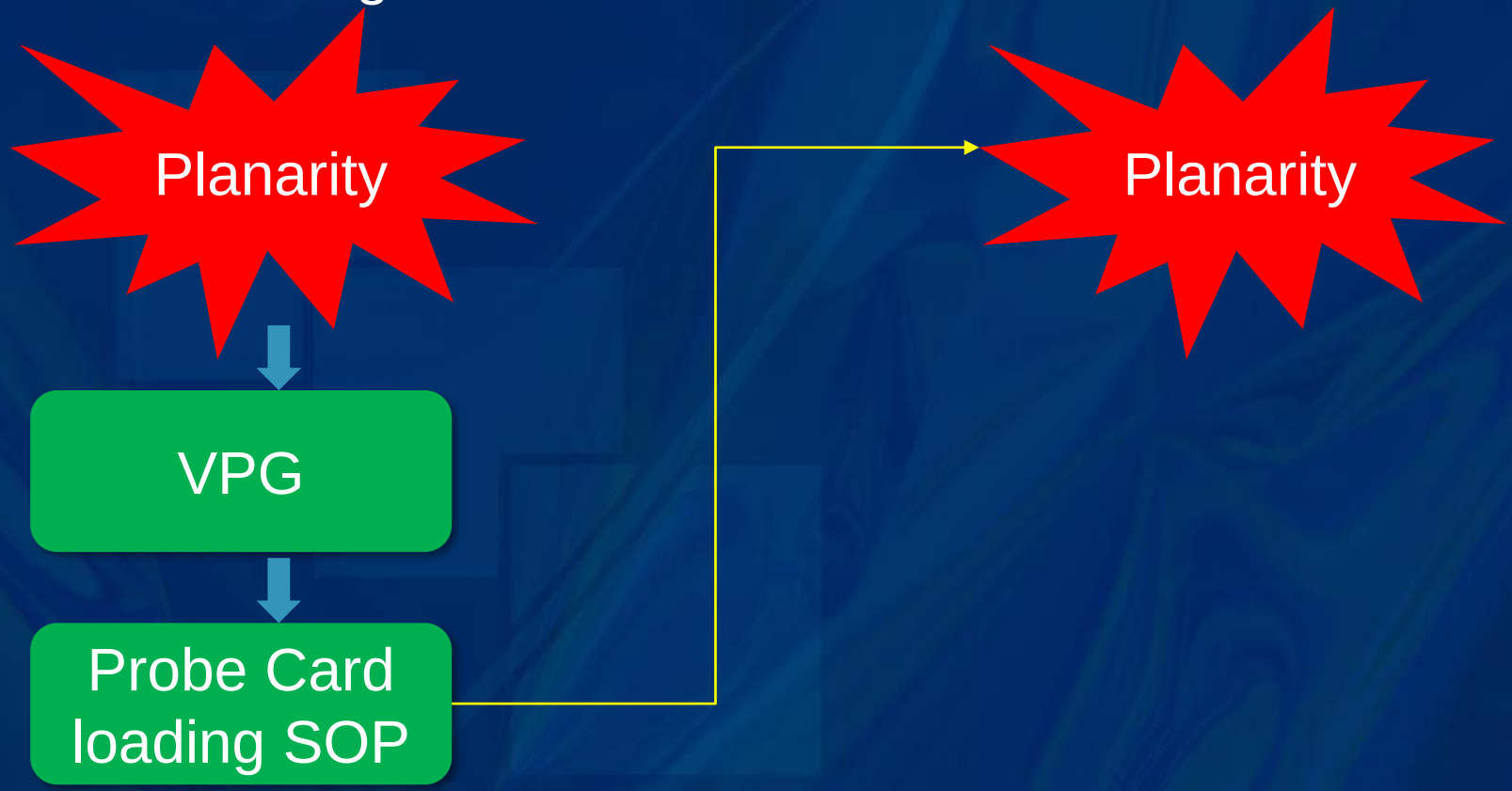
After Docking



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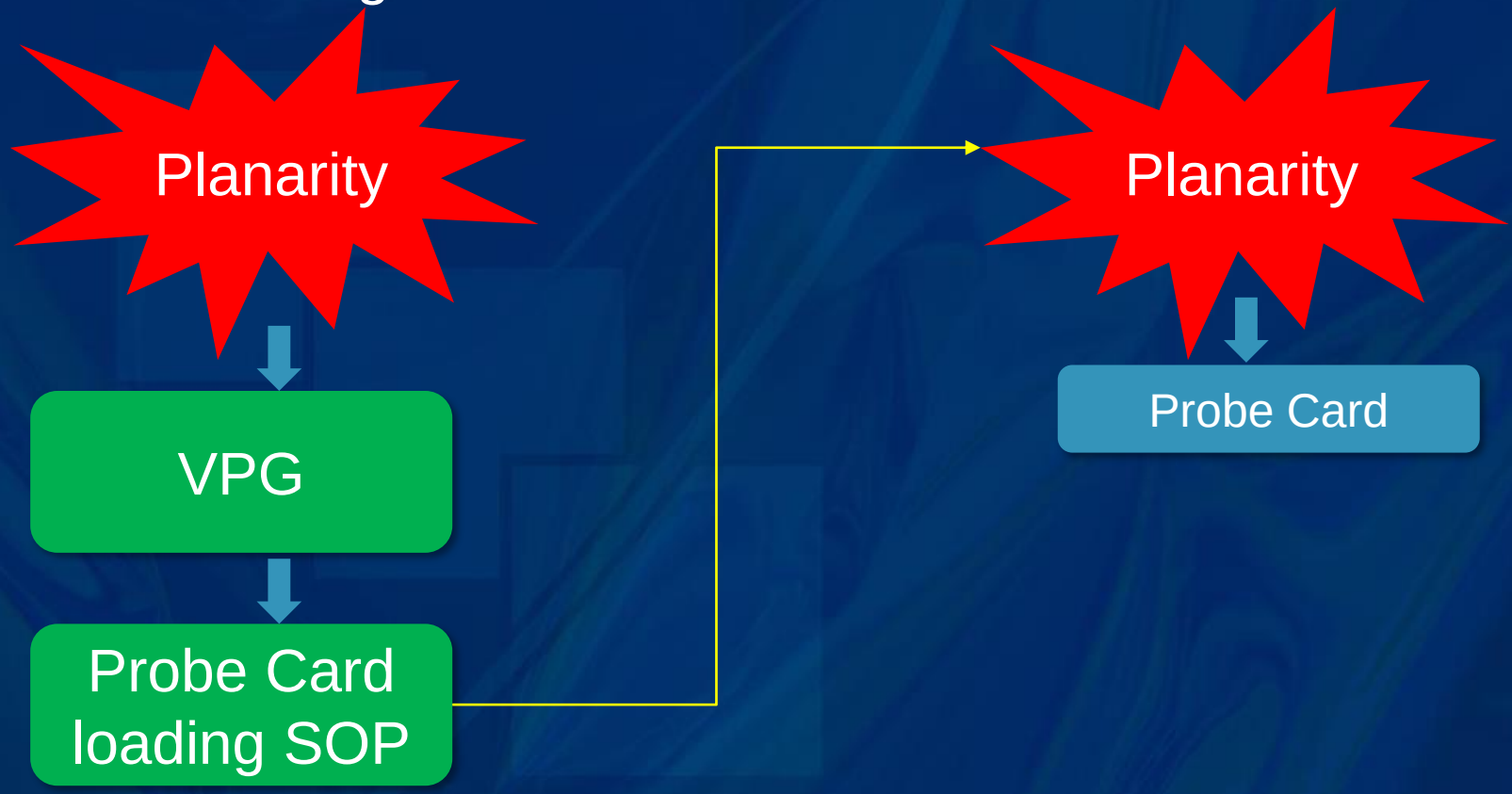

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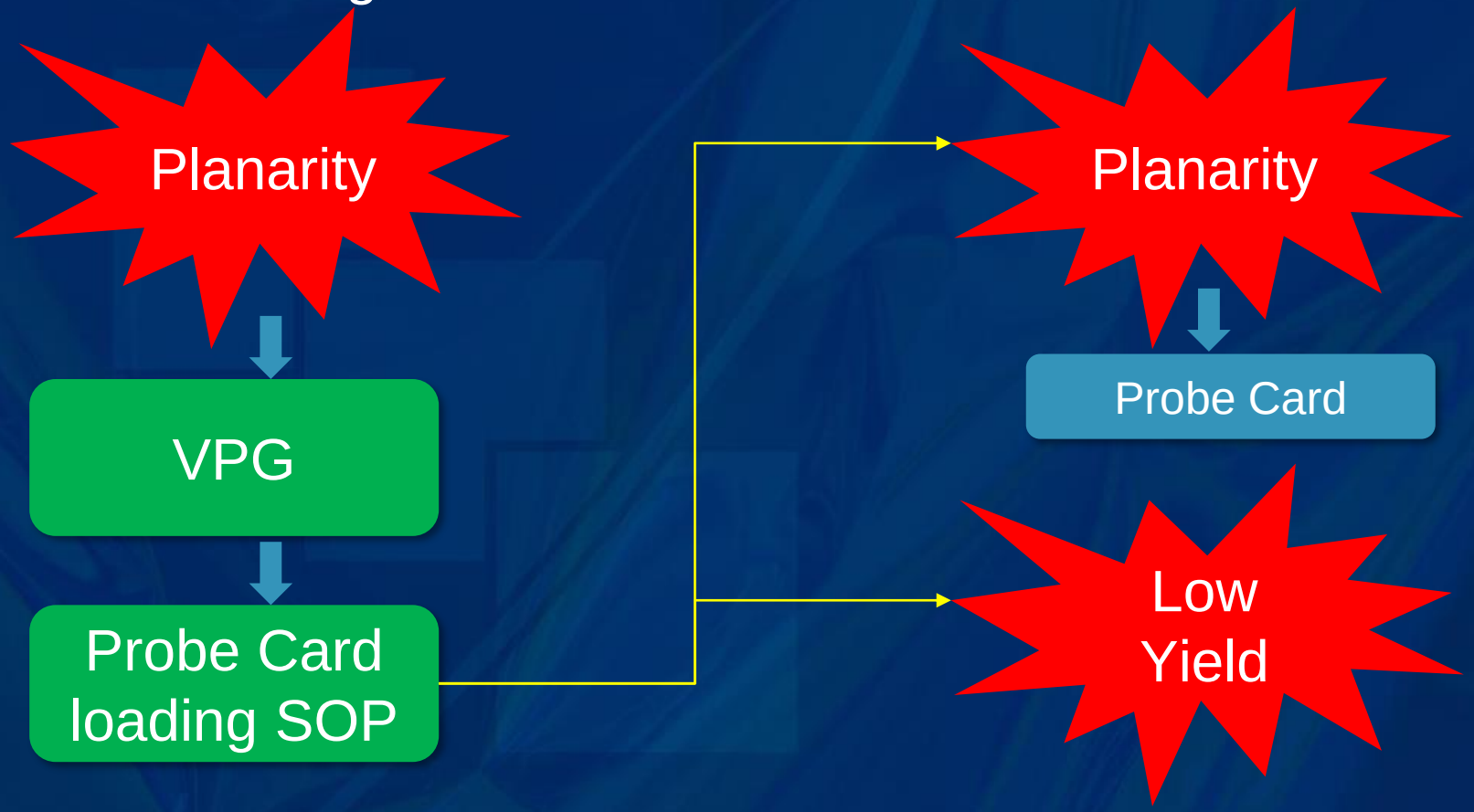

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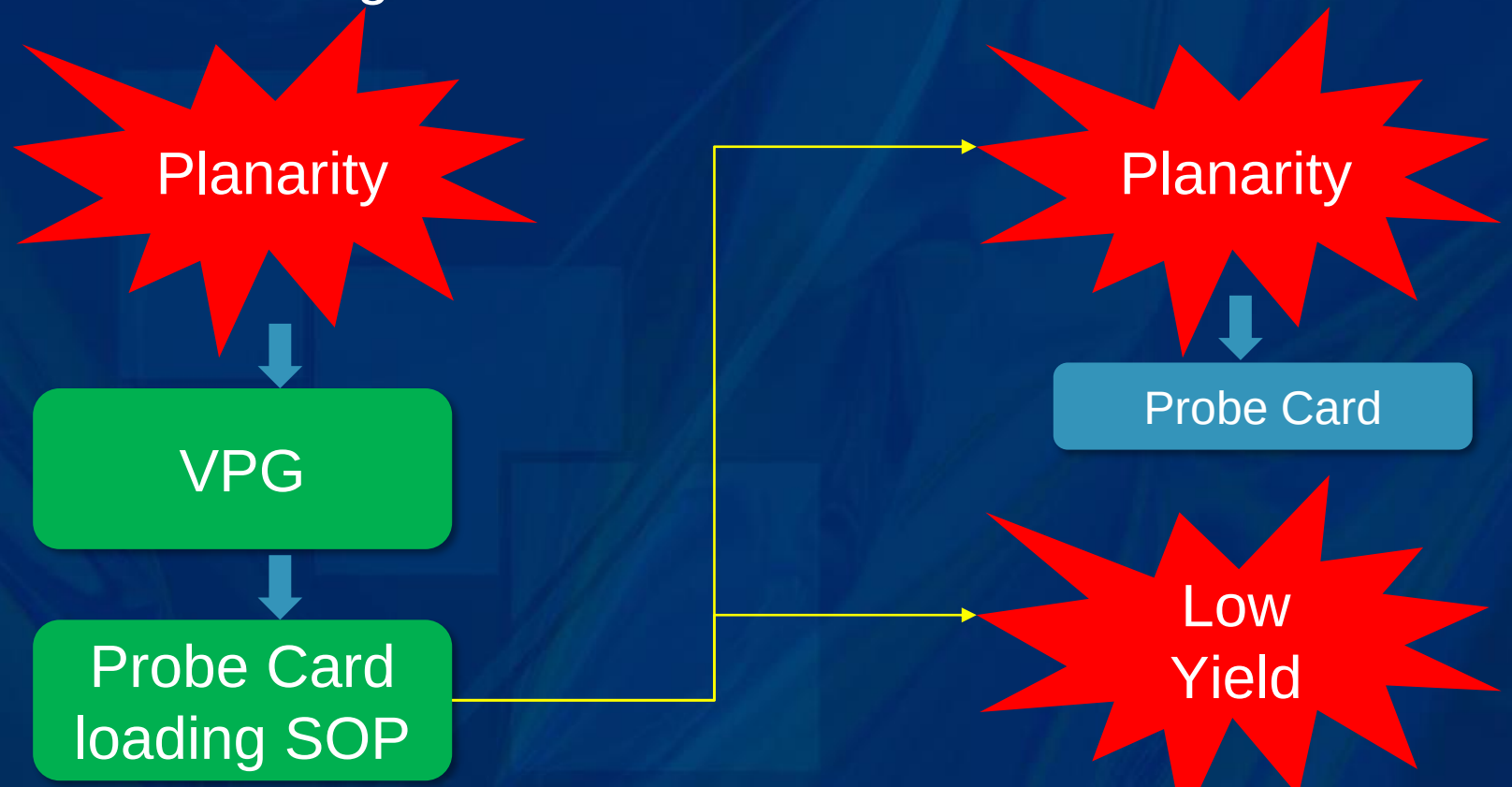

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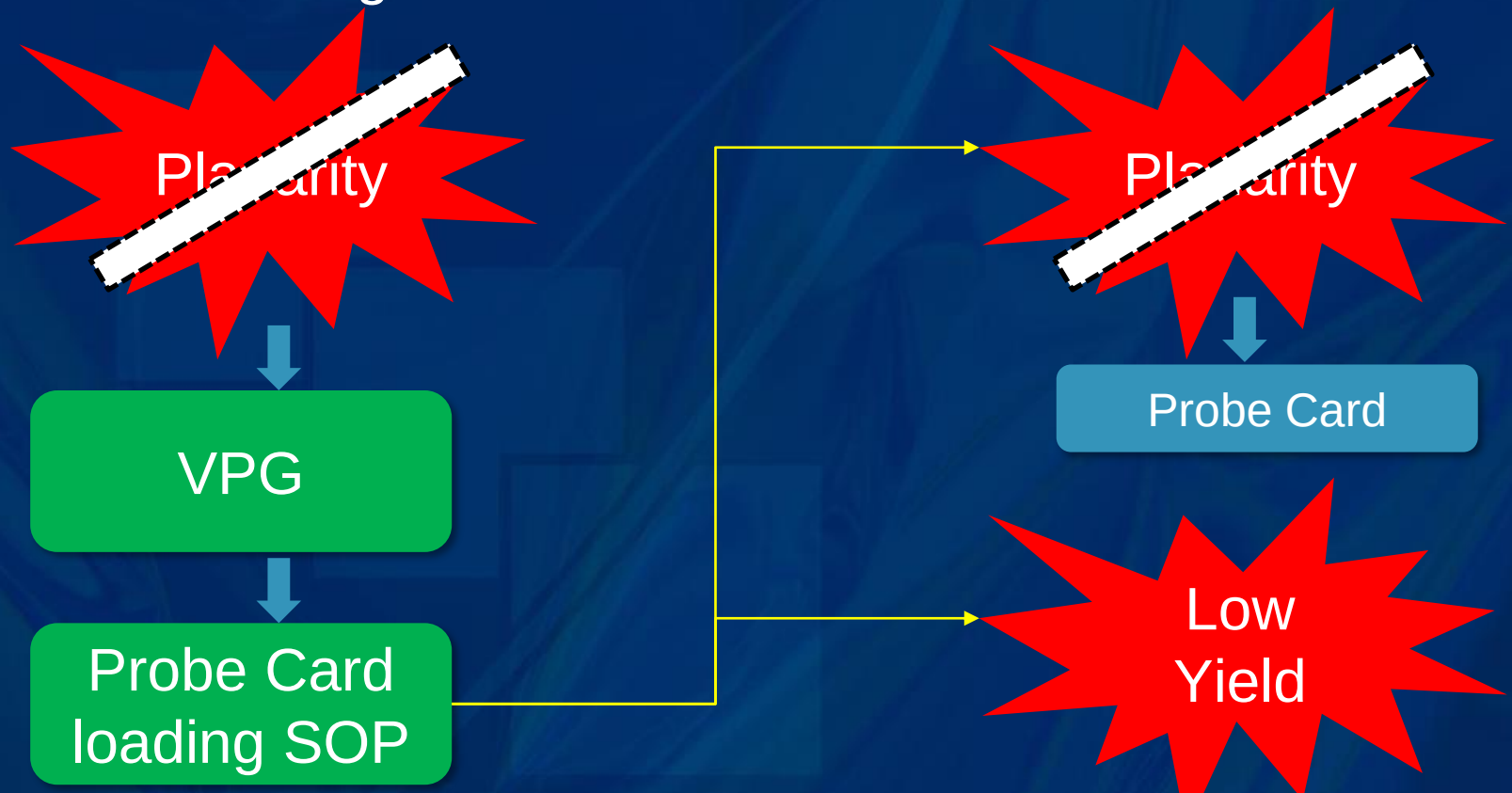
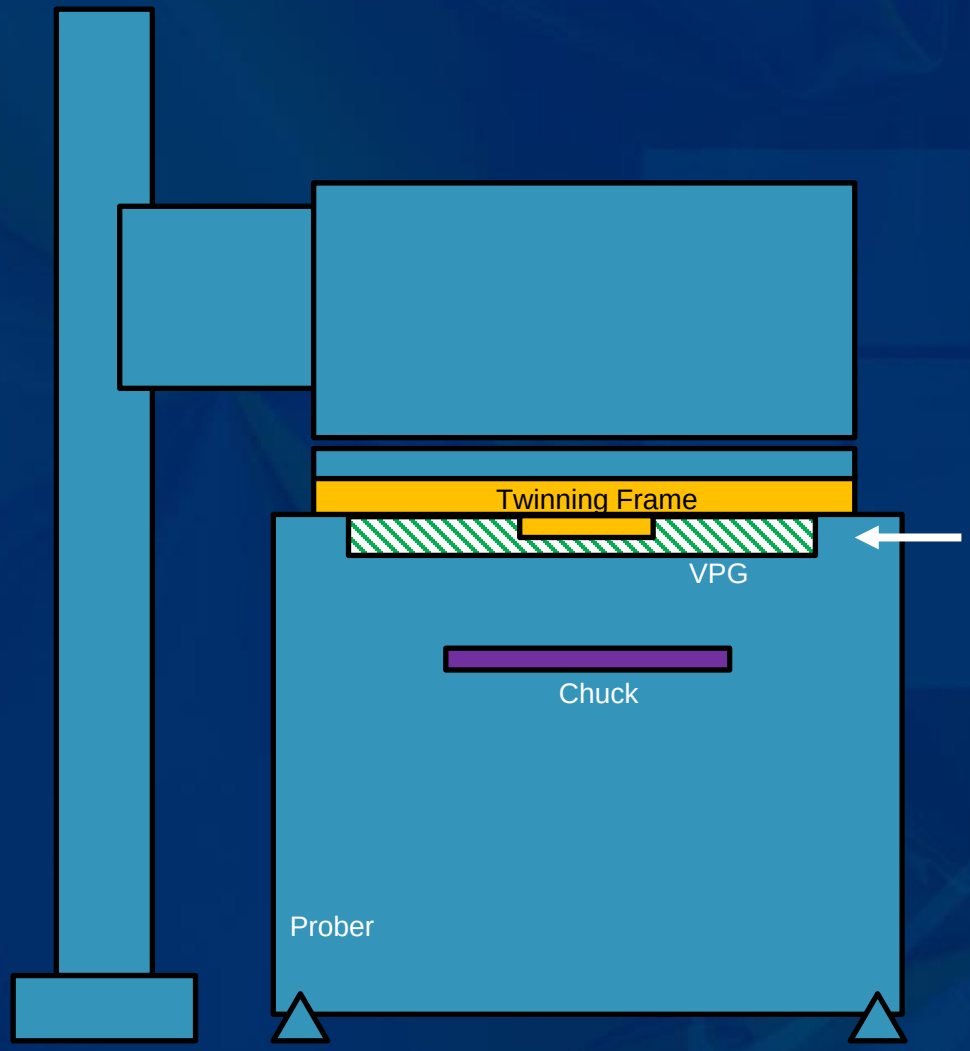


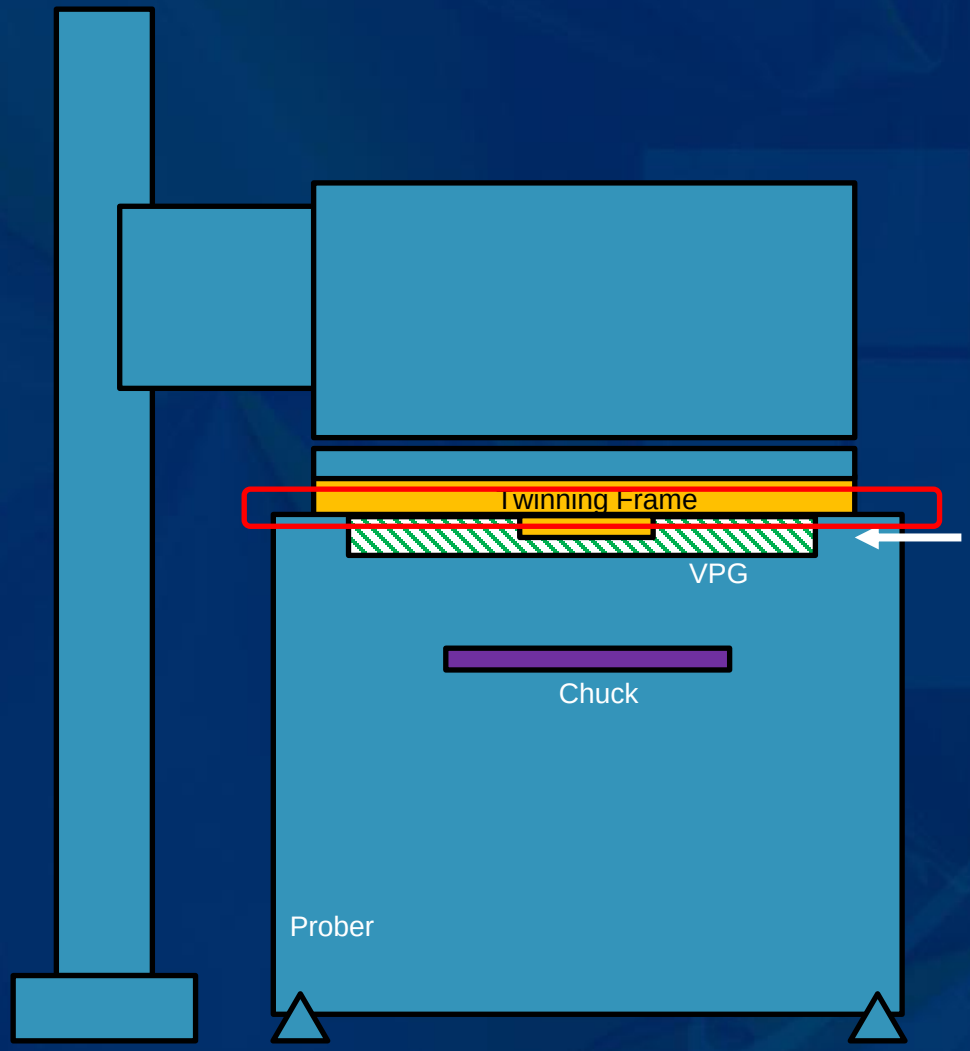
VPG – Verigy Planarization Gauge



- Very effective for prober without auto leveling feature
- Allows minor adjustment to be done on tester head rest planarity
- Reflects the actual planarity on a fully docked system

- Designed and calibrated by Advantest
- Adjustment was done based on 5 calibrated points on VPG unit to meet the expected planarity

VPG – Verigy Planarization Gauge



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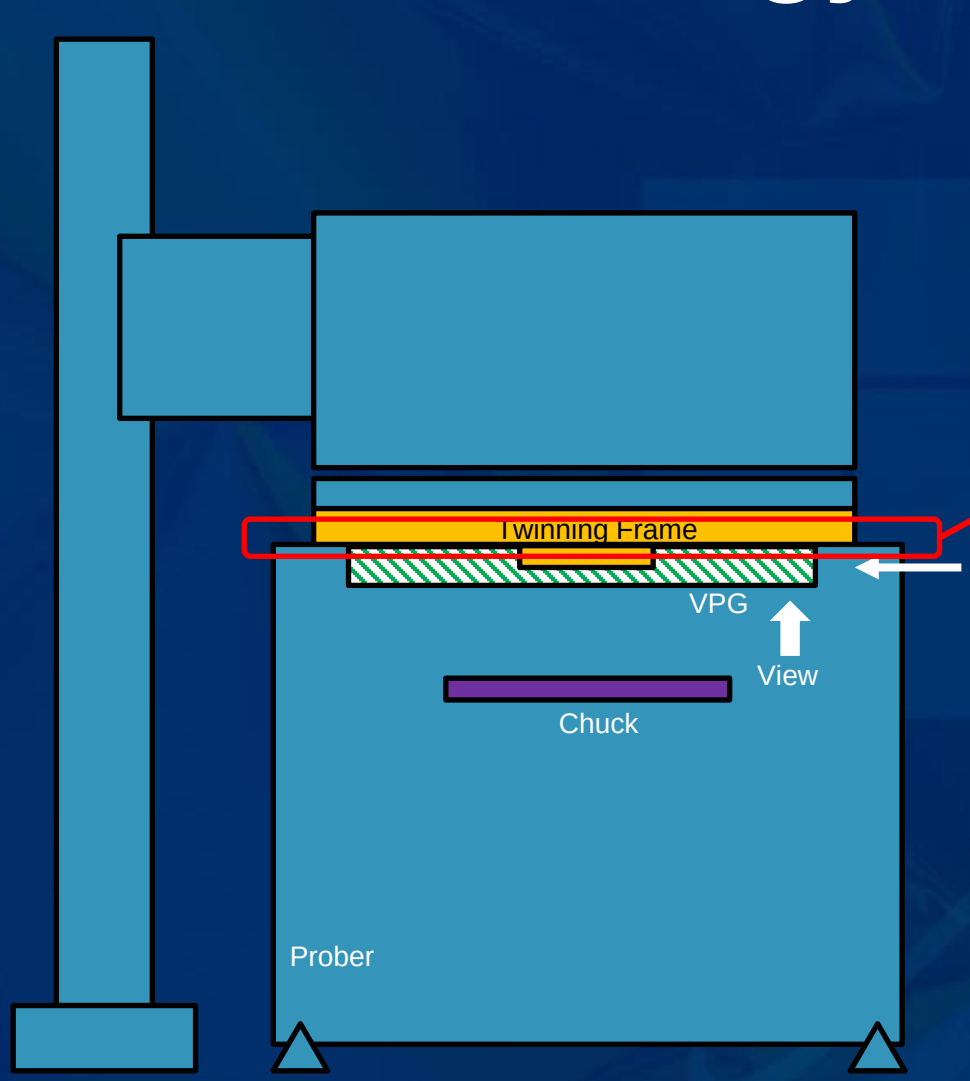

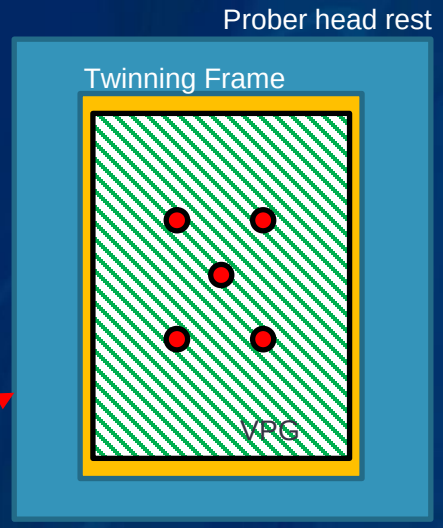

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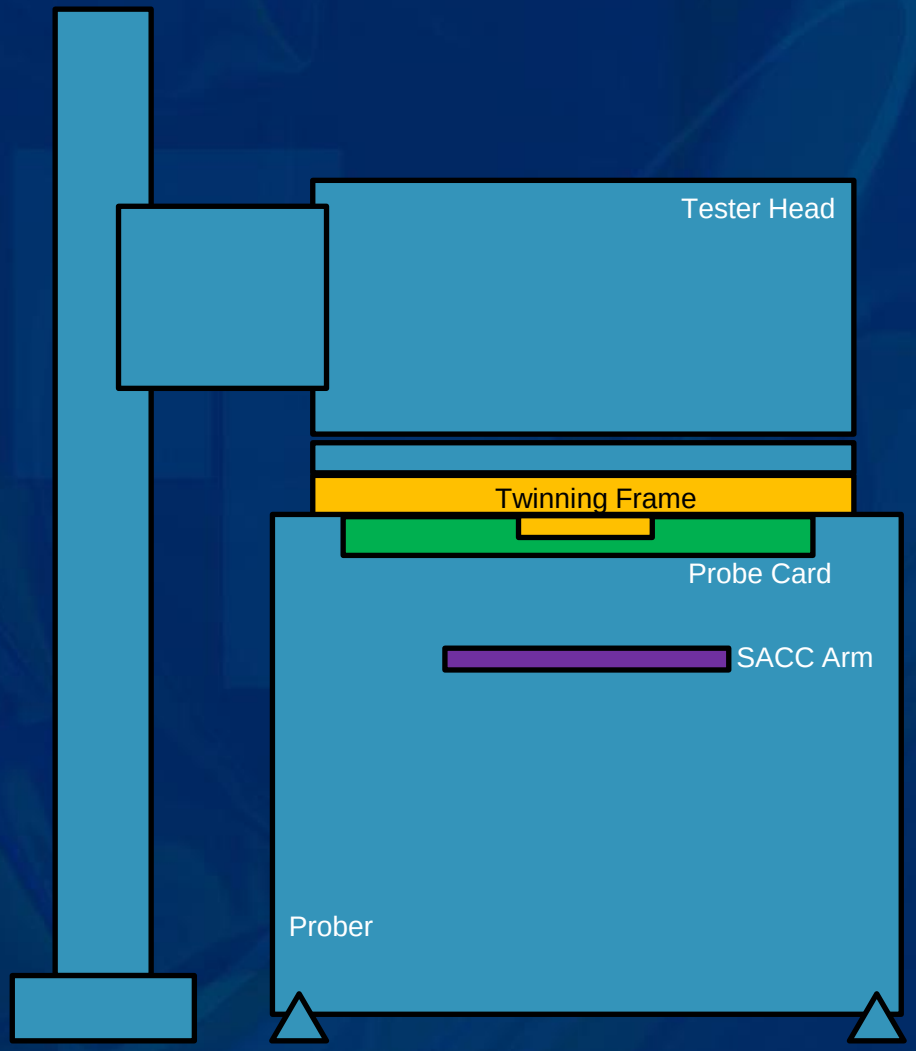
KGD System Setup and Probe Card Loading SOP



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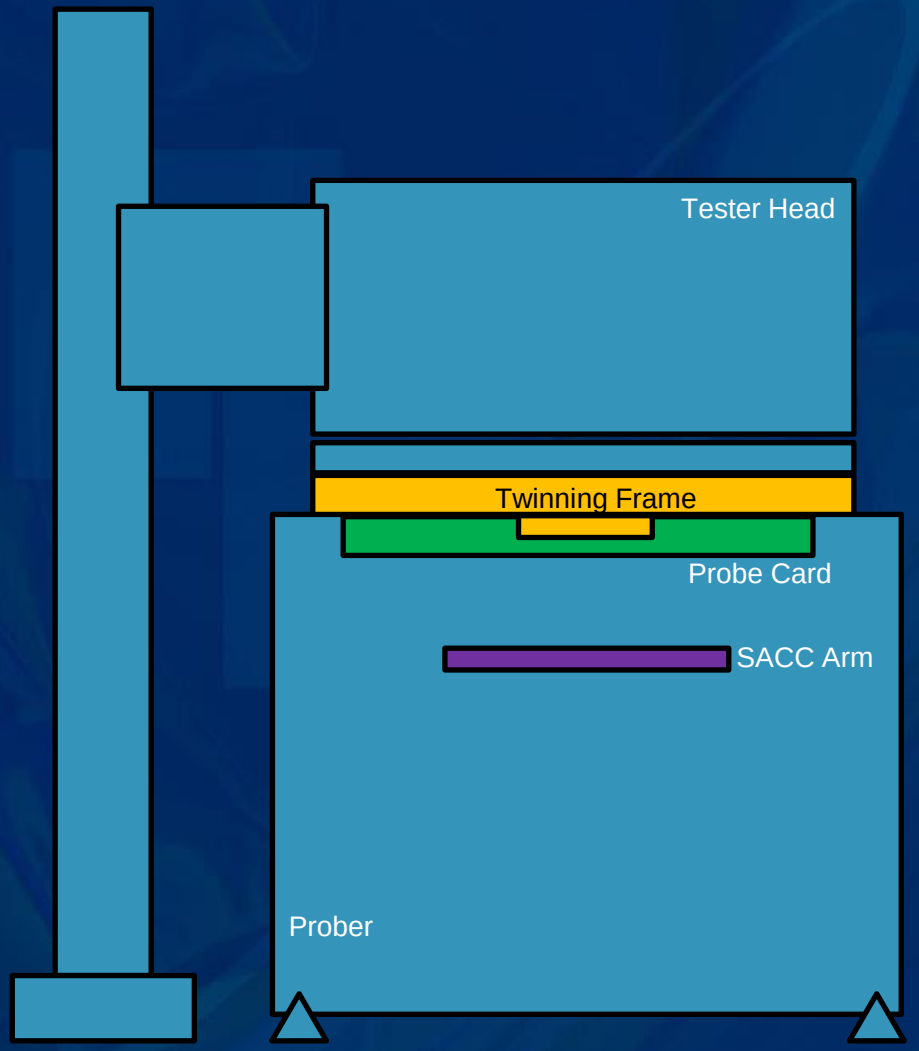

- Multiple external forces / vectors are acting to the probe card during docking process
- These vectors came from various component ie. Tester head, prober , twinning frame, bridge beam, and probe cards

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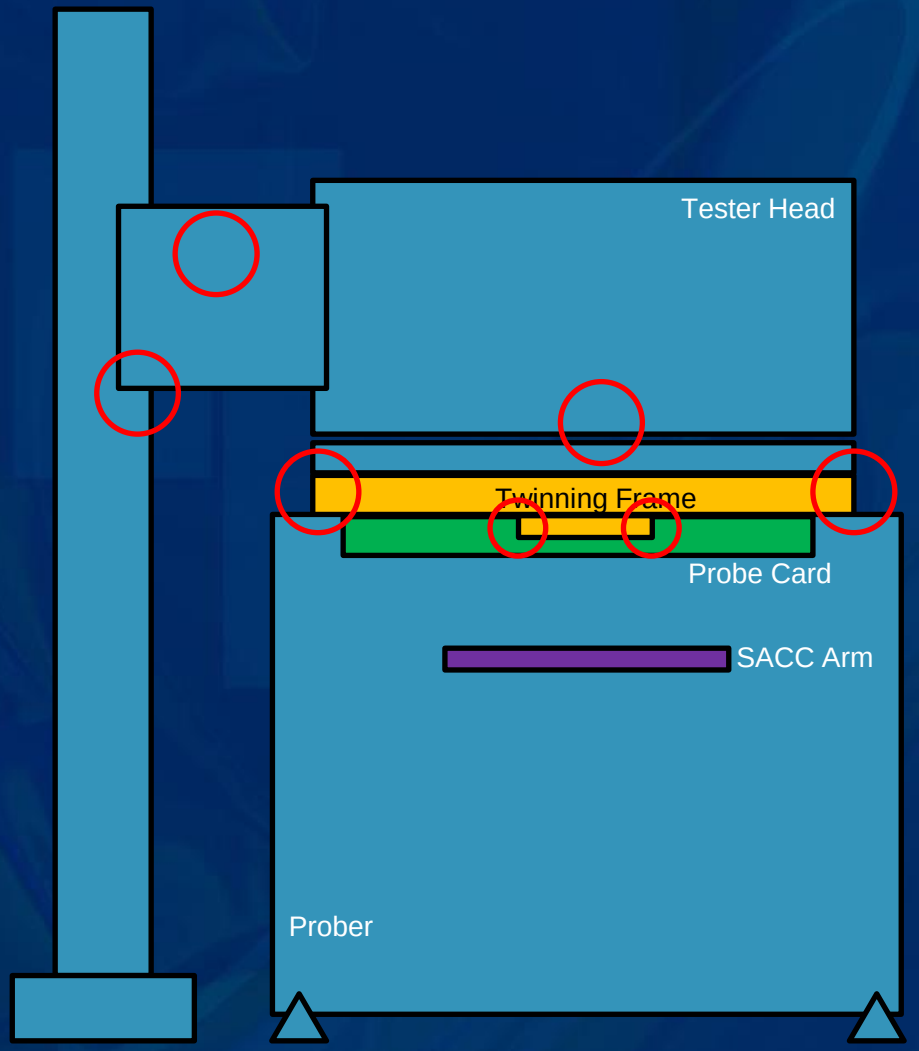

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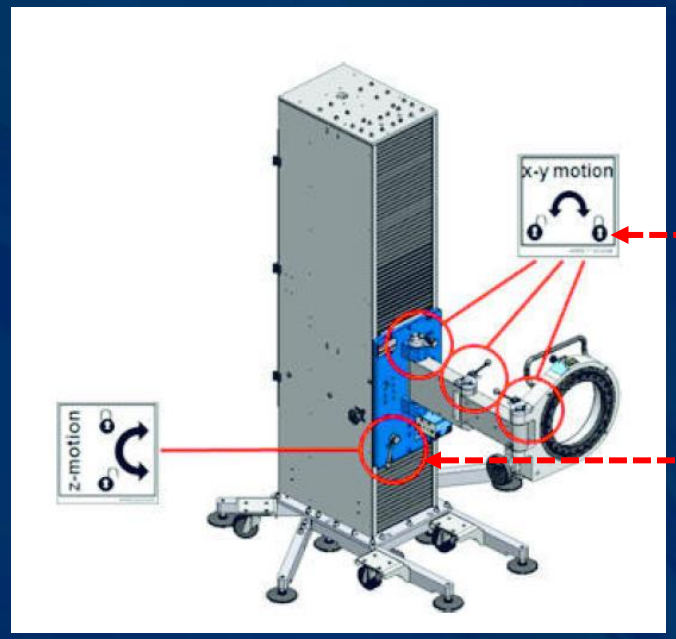

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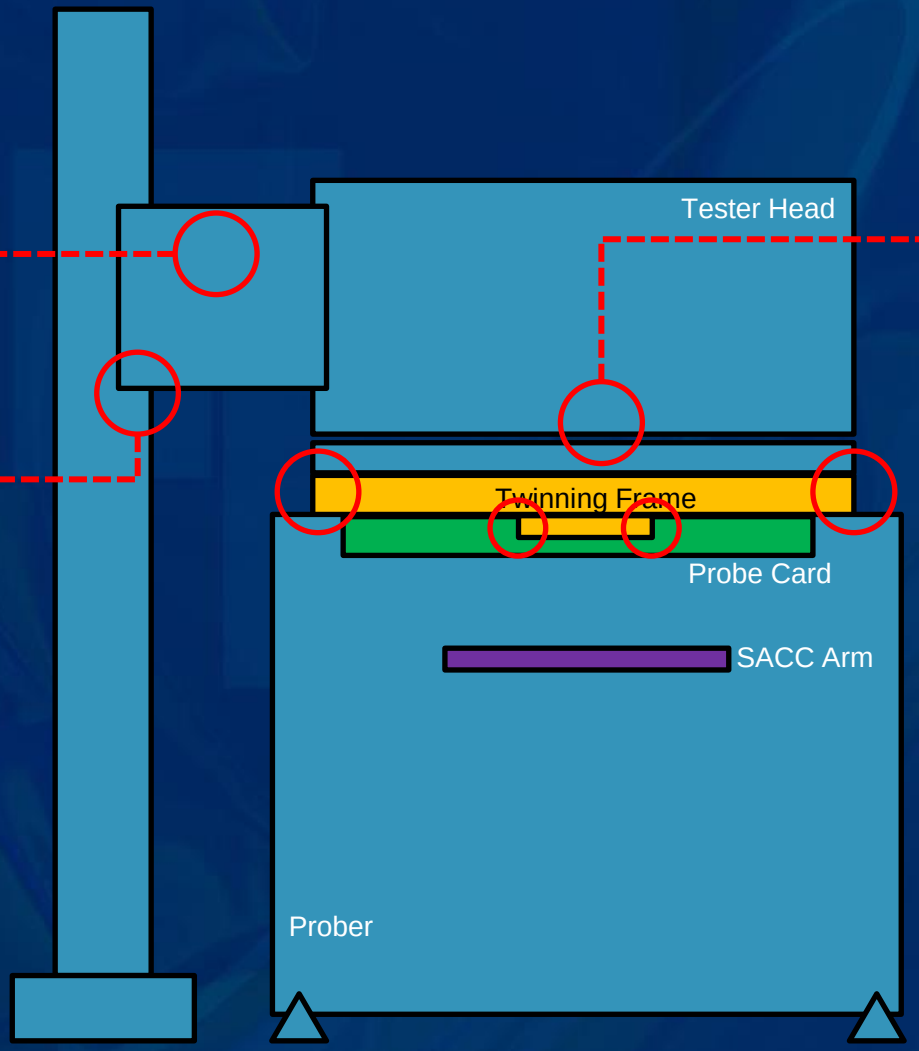

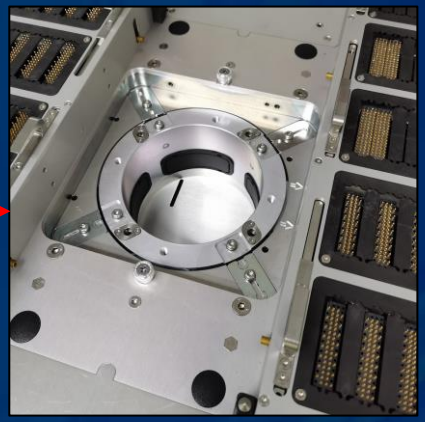

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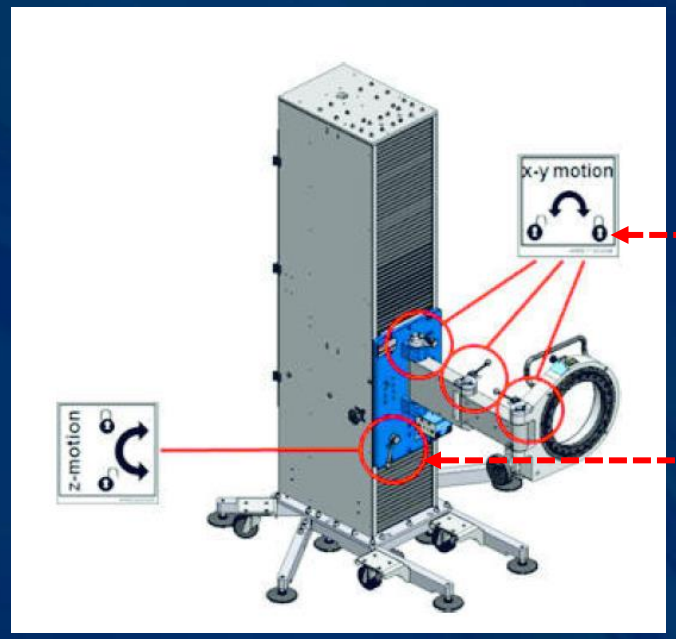

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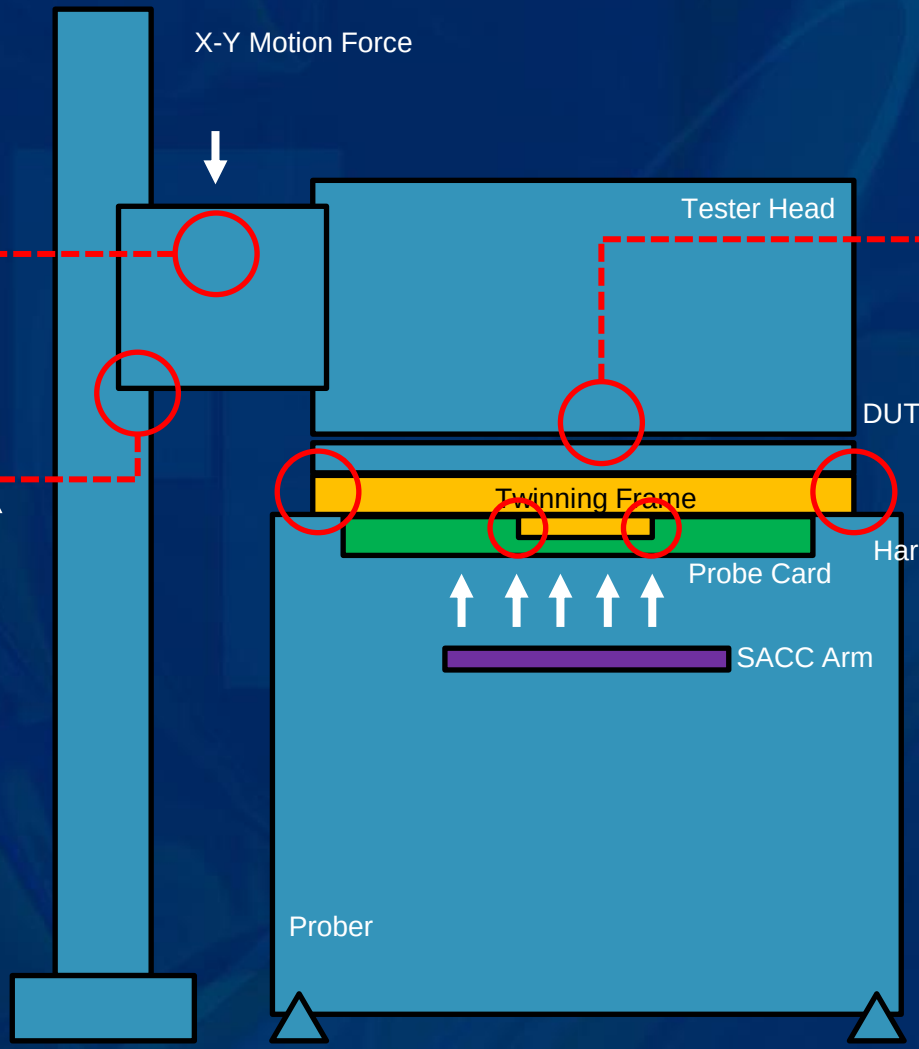

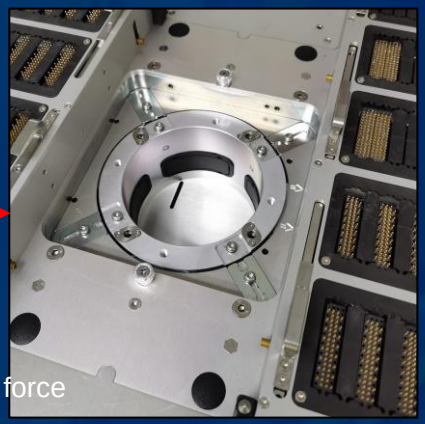

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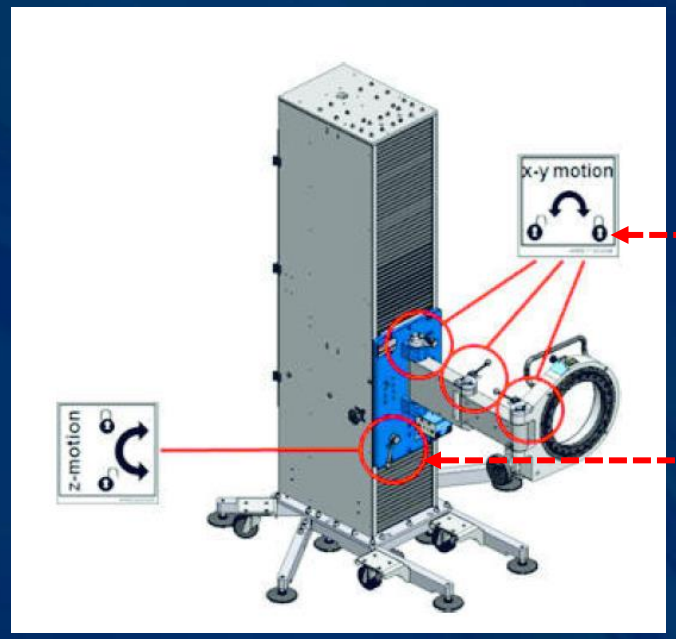

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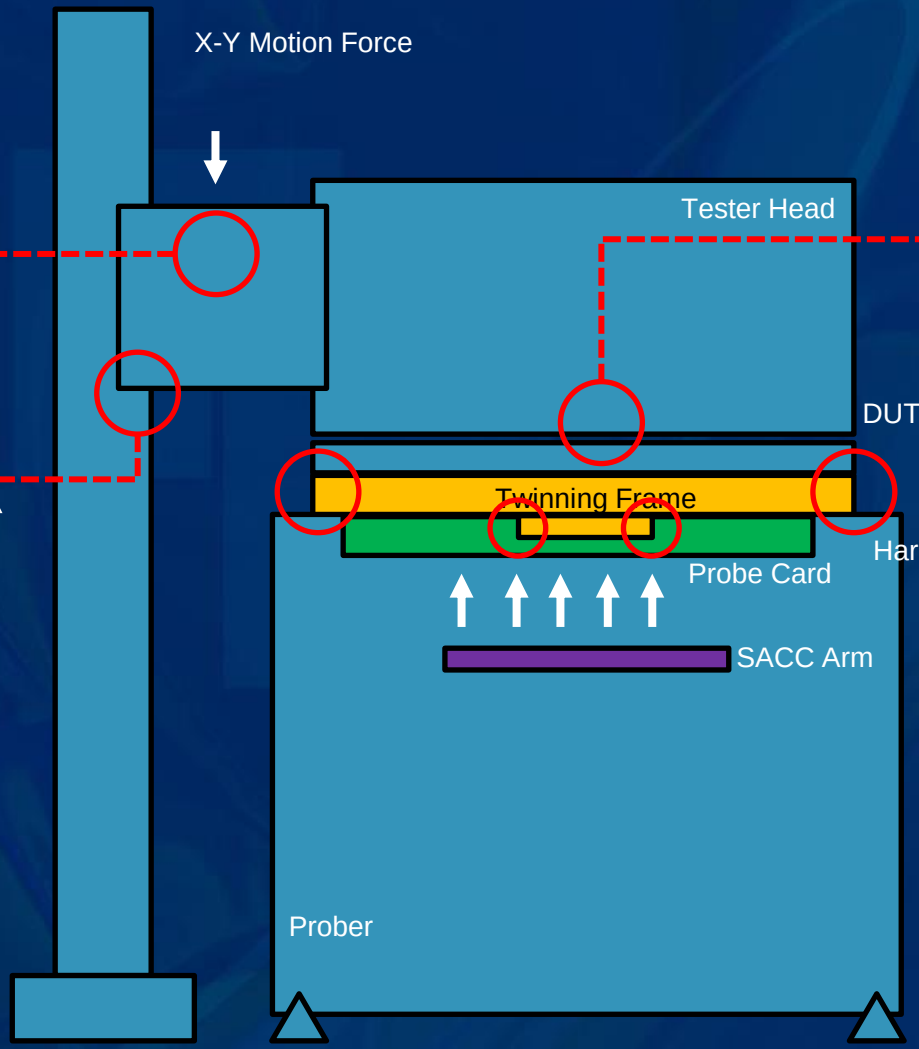

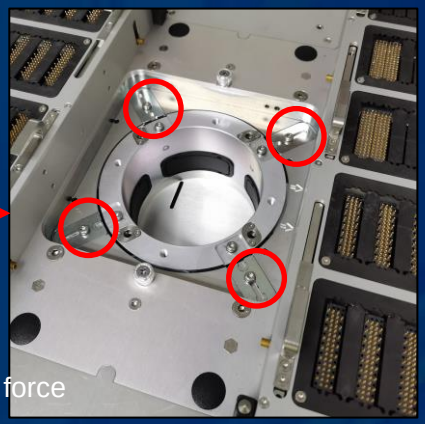

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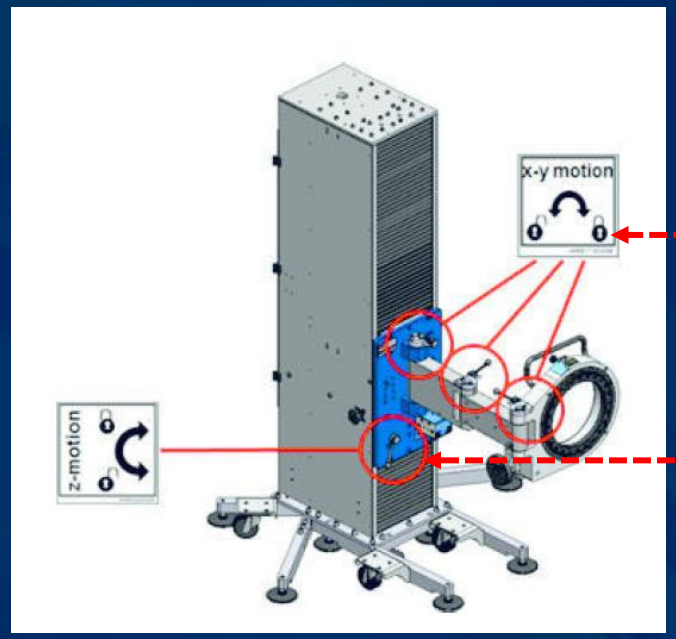

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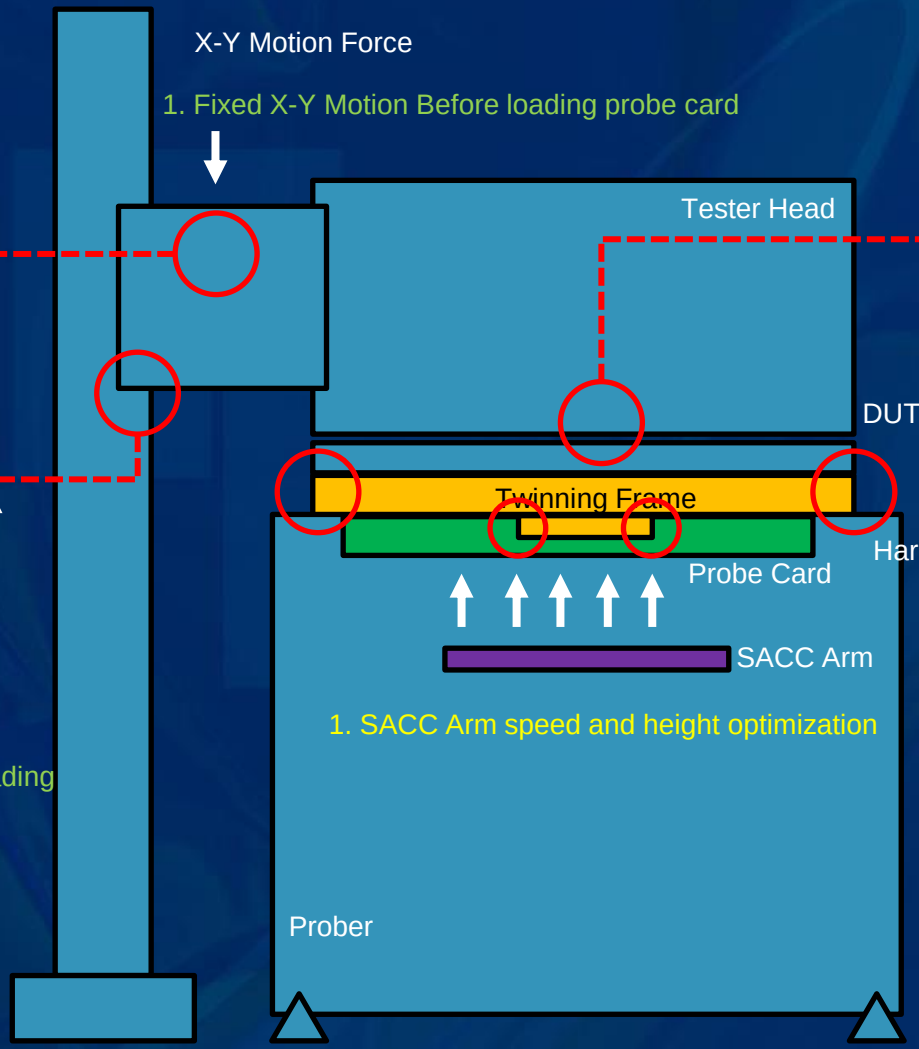

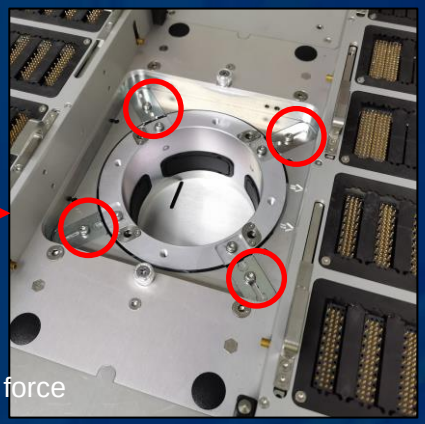

2. Release tester head – allowing better tolerance to external forces

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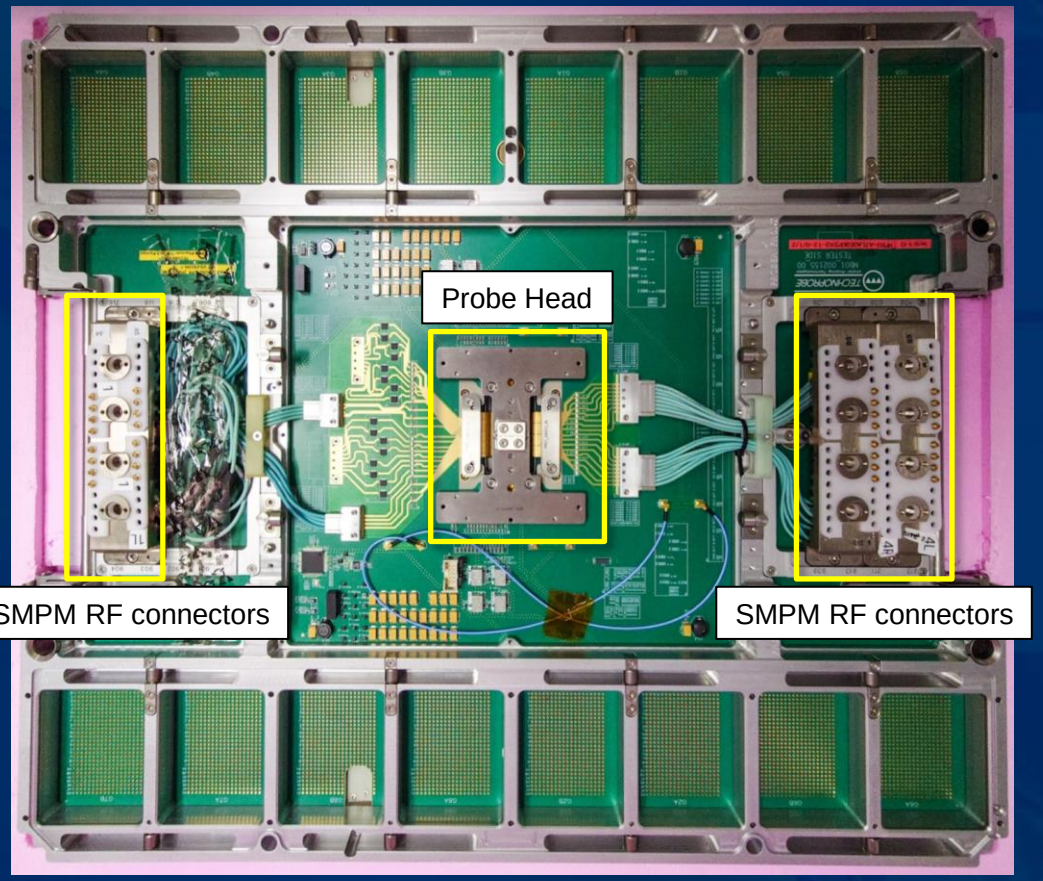
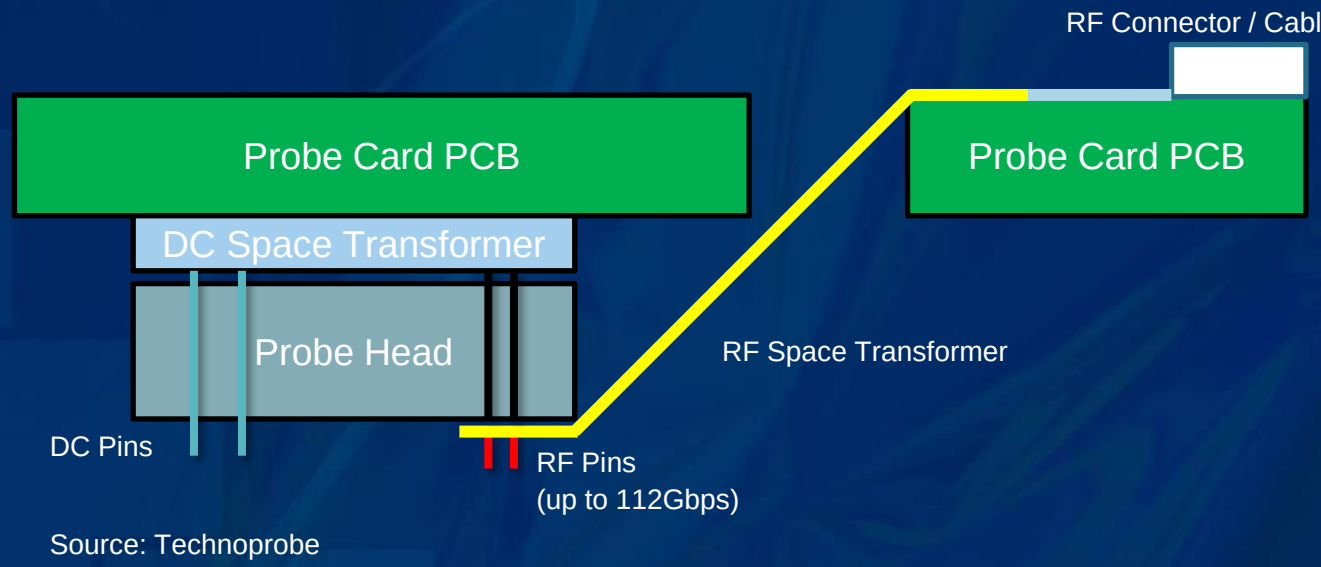
Probe Card Overview





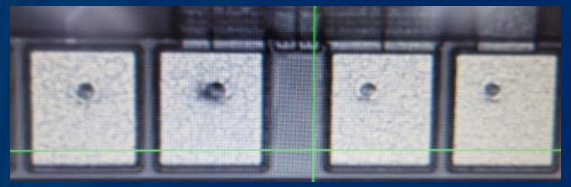
Source: Technoprobe

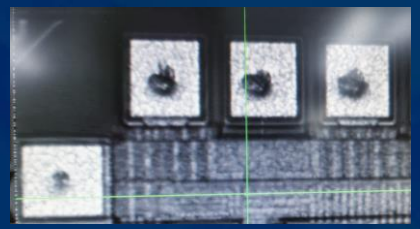
Probe Card Issue and Challenges

- Probe Needle Planarity
- Contact Issue
- Handling / Sustaining
- Long setup time
- Needle's IR drop
- Cleaning Activation Routine
- Irregular Probe marks
- Performance degradation over time
- High Working OD

Probe Needles' Planarity

- Unoptimized alignment
- Risk of probing at edges of pad





- Uniformity issue
- Poor contact
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- Inconsistent overtravel across probe cards
- Risk of damaging circuit under pad

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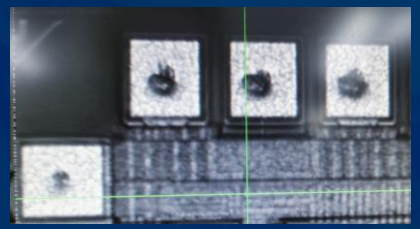

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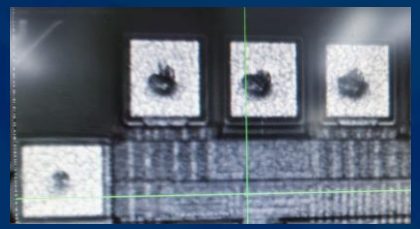

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- Next generation of guide plate was introduced to strengthen probing
- Less aggressive WOD
- Inconsistent WOD across different probe cards

Probe Needles' Planarity

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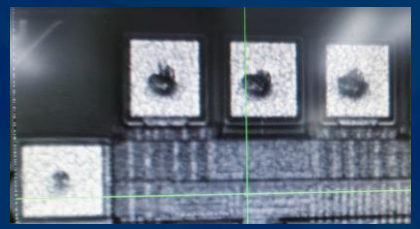

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Gen 3
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- Consistent WOD recipe can be applied
- Higher pin resistivity causing IR drop on power pins (40% higher)

Probe Needles' Planarity

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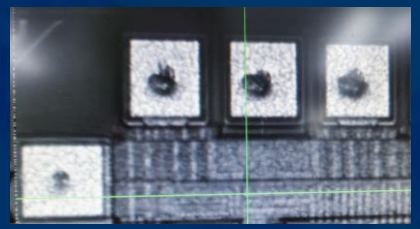

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Gen 4
- Higher gram force
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- Lower pin resistivity

Probe Needles' Planarity

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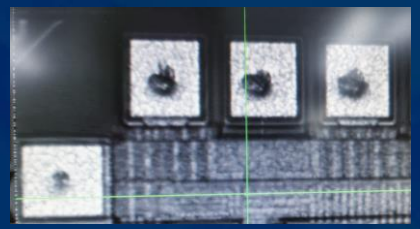

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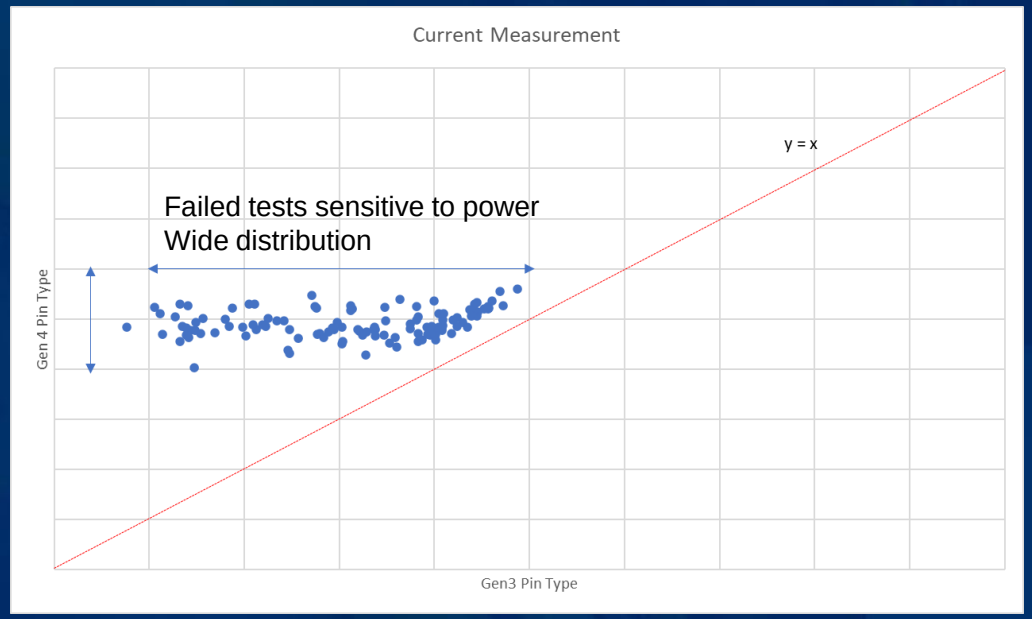
- Lower pin resistivity

Gen 5
- Thicker gold plating being introduced to further reduce overall resistivity on DC power pins

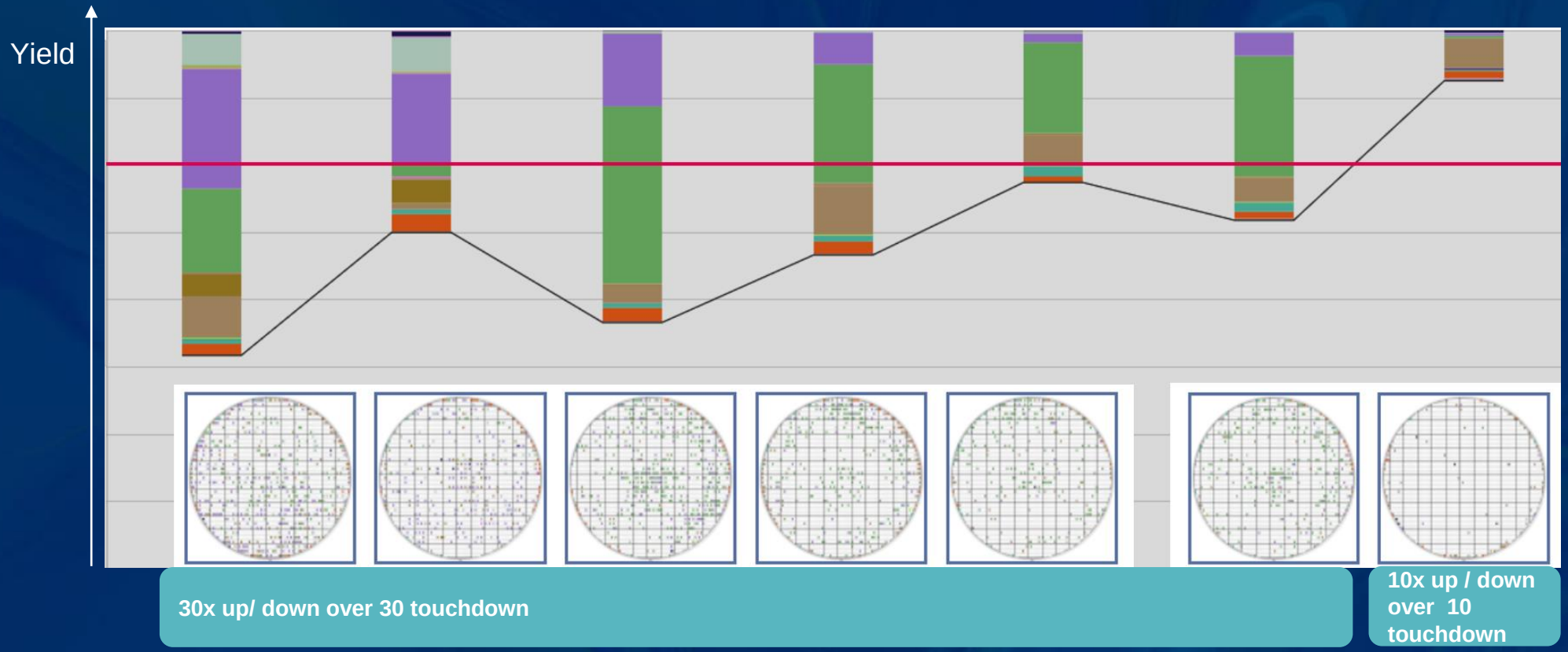
IR Drop Issue



- **Current measurement of Gen3 (x-axis) vs Gen4 (y-axis) pin type on same samples**

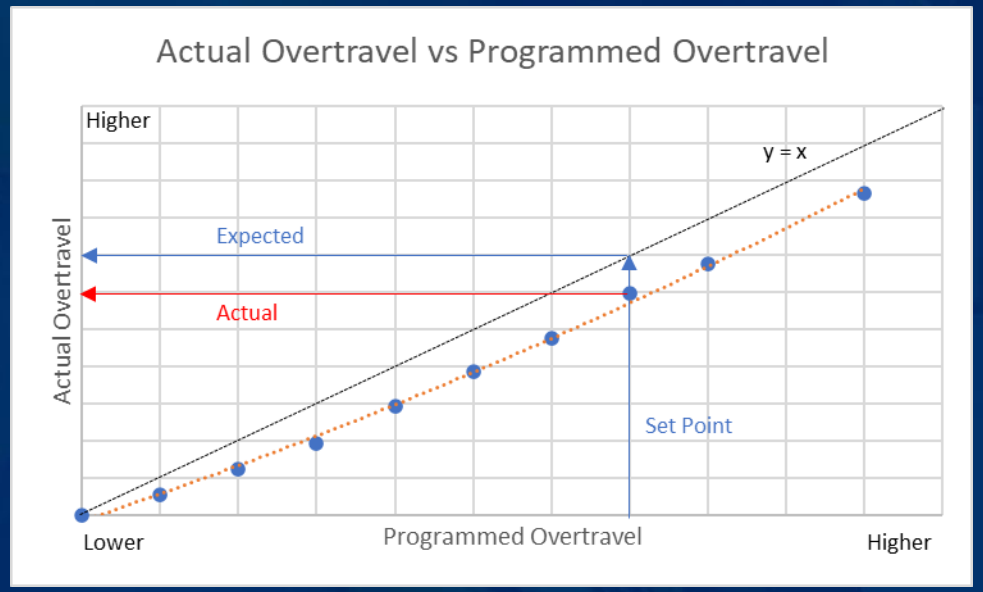
- **IR Drop is contributed by**
  - Probe needles' characteristic (Resistivity) – addressed with lower resistivity needle type
    - Historical data revealed yield loss on voltage sensitive tests reduced from > 40% to <5%
  - Poor Contact – requires optimized cleaning recipe
    - Cumulated particles over time
    - Oxidation

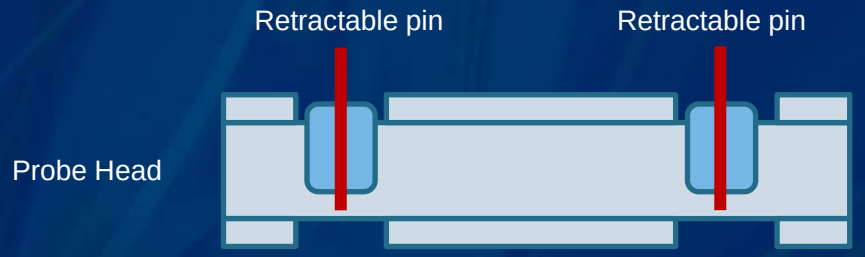
Probe Card - Sustaining and Handling



- **Aggressive cleaning resulted in better yield with the trade off over the needles' life span**

Contact Issue – Actual Overtravel vs Programmed Overtravel





Configuration for AOT vs POT characterization

Source: Technoprobe

- **Programmed Overtravel: setting on prober UI**
- **Actual Overtravel: Resultant overtravel considering the deflection of the system (Prober, Bridge Beam, Probe Card Load)**
- **The study provides additional margin in POT, helps in achieving better contact, lower contact resistance. Improving yield on contact sensitive tests.**

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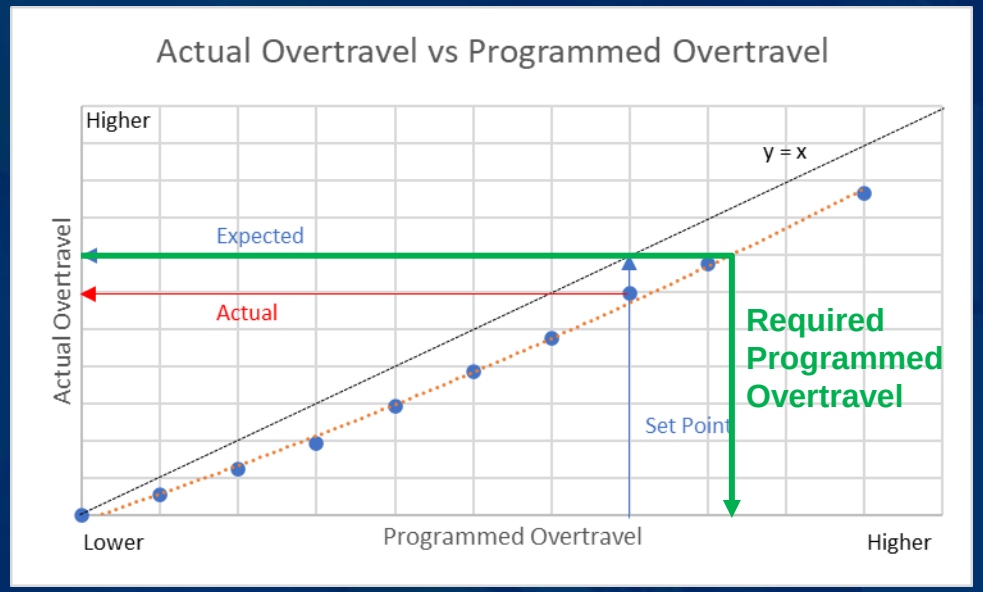

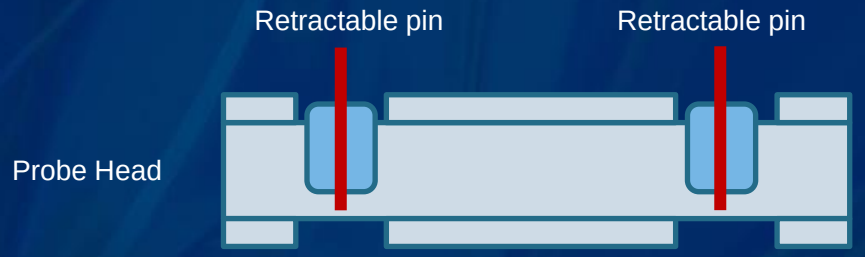

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Conclusions

- **Wafer sort setup with twinning options is a solution to high-speed testing for KGD products with limited loopback capability**
- **Stable high-volume manufacturing setups are achievable via:**
  - Studying the root cause and narrowing down the components leading to setup planarity issue
  - Establishing new S.O.P governing the initial setup and regular production routine
  - Continue collaboration with vendors in exploring existing and new technology to optimize product yield

High Speed Probe Card Architecture for High End Devices

Alice Ghidoni Technoprobe Italy
Alberto Berizzi Technoprobe Italy

4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

Overview

- **Introduction:** Data Intensive Market and Challenges
- **High End Probe Card Requirements**
- **Probe Head Design Optimization**
- **Merlion Probe Head:** Main Features
- **Characterization Data:** Test Fixture

Data Intensive Markets

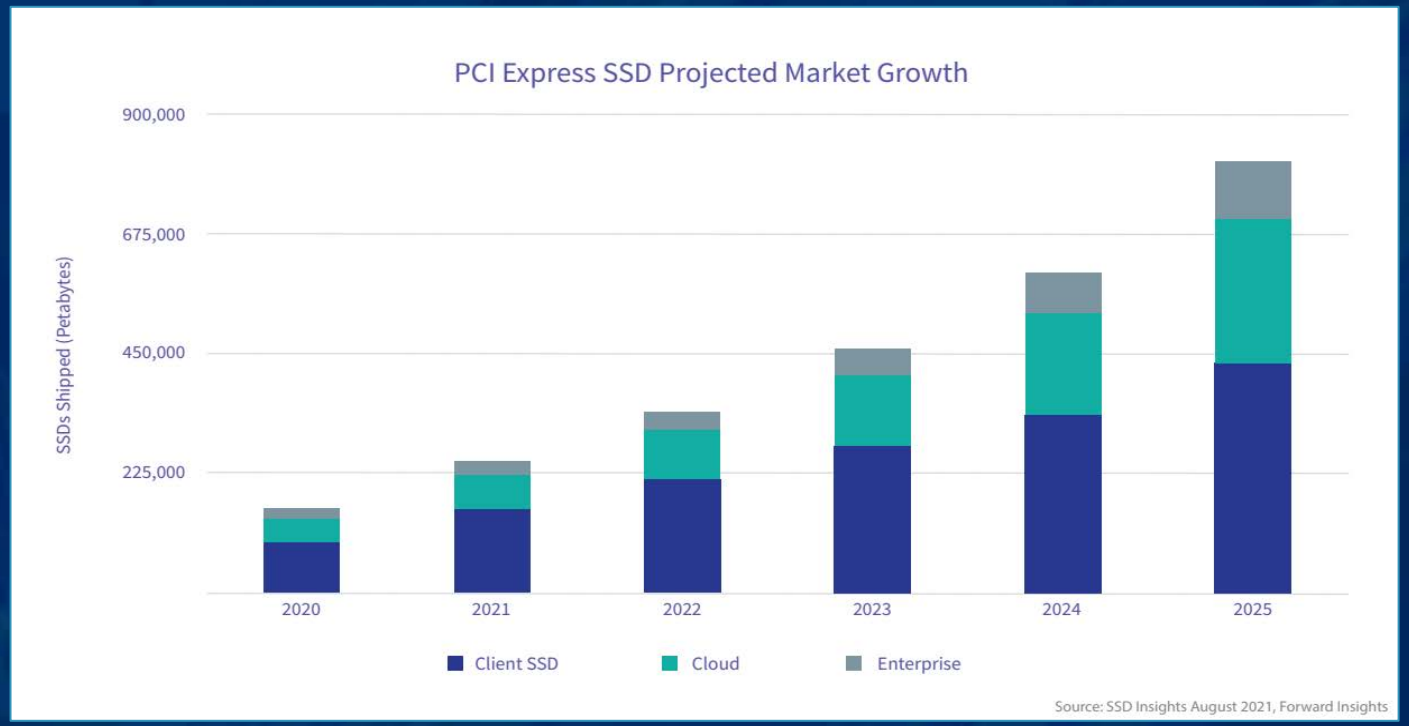
High Performance Computing (HPC)

Automotive

Military and Aerospace

Artificial Intelligence (AI) and Machine Learning (ML)

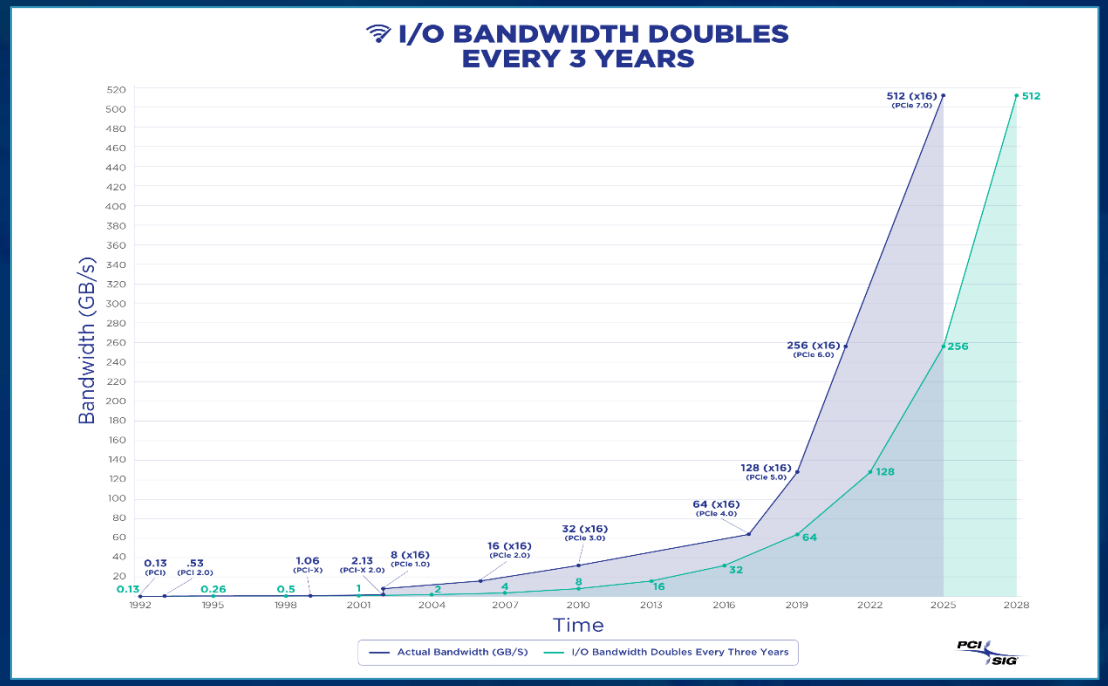
Data Centre



Alice Ghidoni
Alberto Berizzi

Data Rate Explosion

- **PCIe specification doubles the I/O bandwidth every three years and continues to meet industry demand**



Specifications	Lanes				
	x1	x2	x4	x8	x16
2.5 GT/s (PCIe 1.x +)	500 MB/S	1 GB/S	2 GB/S	4 GB/S	8 GB/S
5.0 GT/s (PCIe 2.x +)	1 GB/S	2 GB/S	4 GB/S	8 GB/S	16 GB/S
8.0 GT/s (PCIe 3.x +)	2 GB/S	4 GB/S	8 GB/S	16 GB/S	32 GB/S
16.0 GT/s (PCIe 4.x +)	4 GB/S	8 GB/S	16 GB/S	32 GB/S	64 GB/S
32.0 GT/s (PCIe 5.x +)	8 GB/S	16 GB/S	32 GB/S	64 GB/S	128 GB/S
64.0 GT/s (PCIe 6.x +)	16 GB/S	32 GB/S	64 GB/S	128 GB/S	256 GB/S
128.0 GT/s (PCIe 7.x +)	32 GB/S	64 GB/S	128 GB/S	256 GB/S	512 GB/S

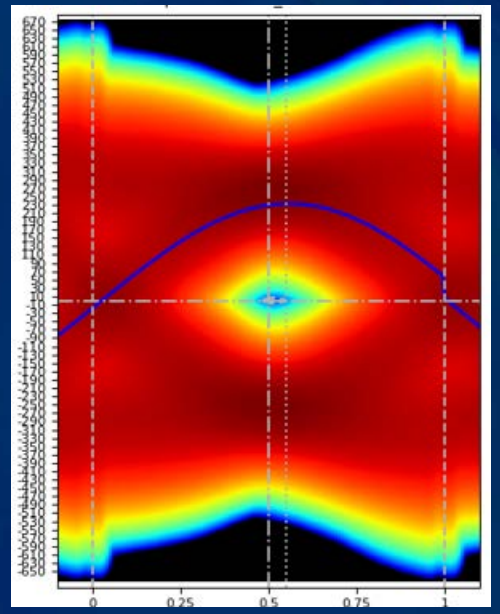
- **Demand for a reliable, high-speed, low latency I/O interconnect for data-intensive applications and markets, (Artificial Intelligence and Machine Learning (AI/ML), High Performance Computing (HPC), Quantum Computing, Hyperscale Data Centers and Cloud).**

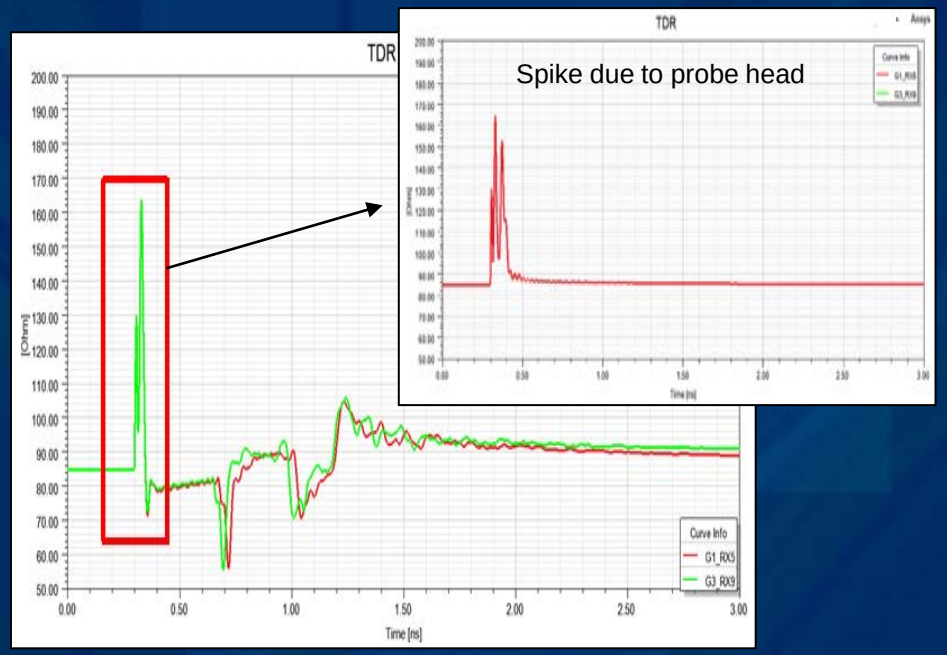
Challenges

- **Bump pattern is not optimized for EWS probe solution from Signal Integrity point of view.**
- **Probe impedance and Crosstalk are strongly dependent on bump pattern and power and ground position compared to high-speed signals bump.**

- **Existing probe solution is a closed eye at NRZ 25GT/s.**

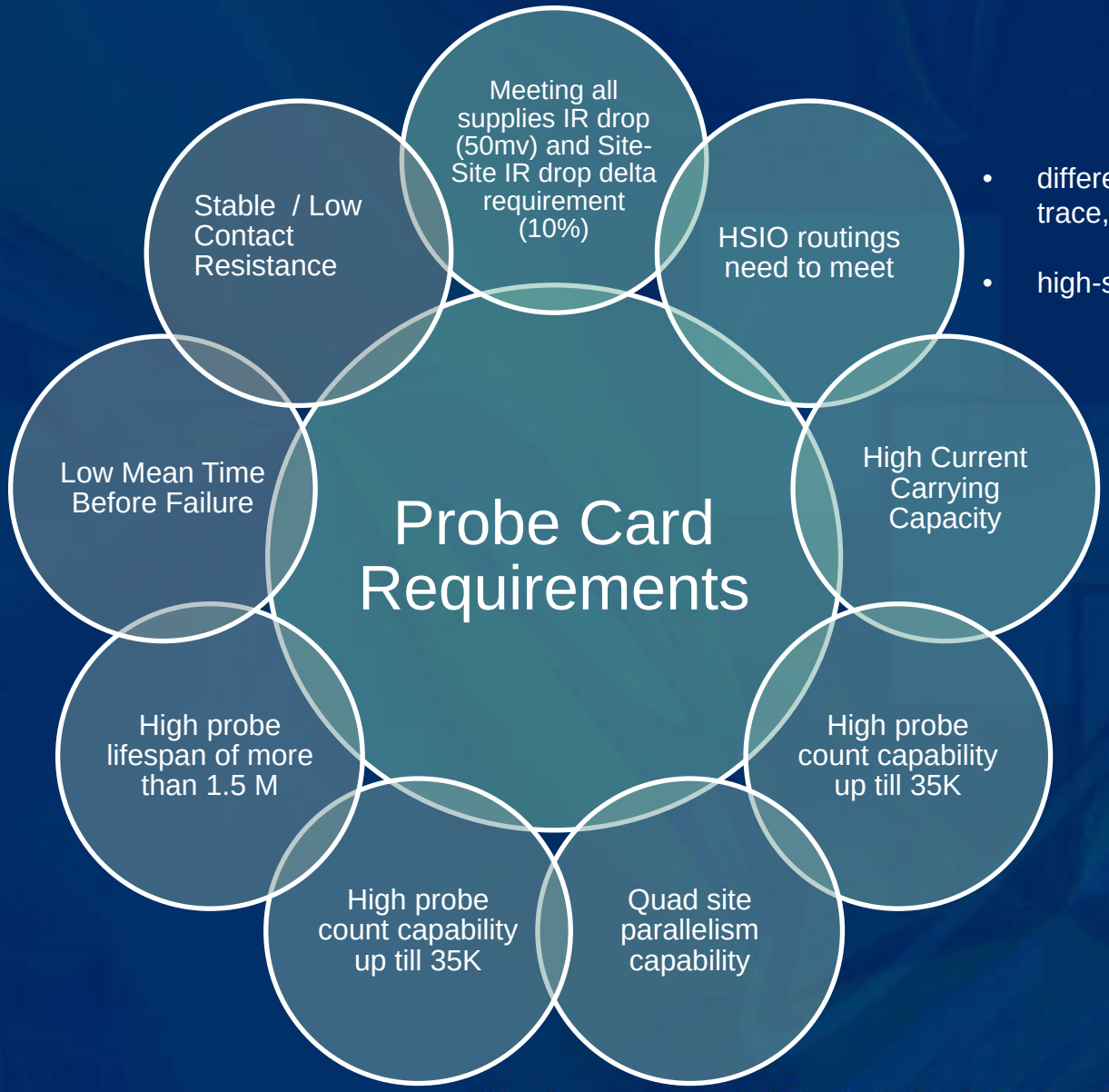
  → Impedance mismatches at probe head to probe card.





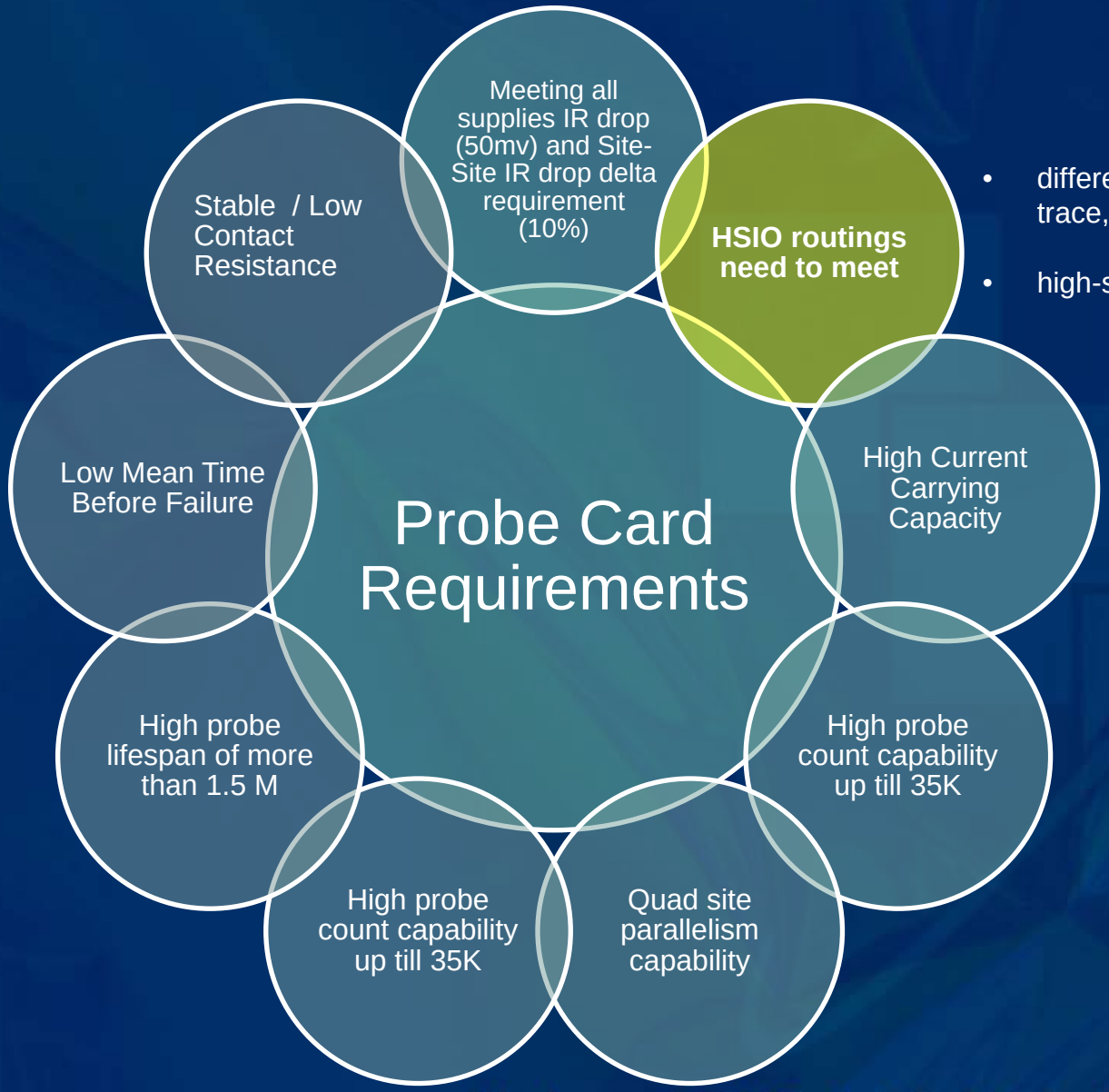
Standard probe card solution in the market does not offer **HIGH SPEED** , **HIGH CURRENT CARRYING CAPACITY** and **HIGH LIFETIME** at the same time.

High End Probe Card Requirements



- differential / single ended impedance target for overall path (includes loopback through direct trace, relays, bias-T, and high-speed routes to ATE tester)
- high-speed end-to-end requirement for HSIO loopback path (up to 32GT/s NRZ)

High End Probe Card Requirements



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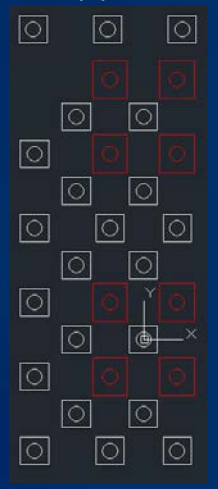
Probe Head Design SI Optimization: Optimization Strategy

- **Target: High-speed signals performance:**
  - Reference Impedance match
  - Crosstalk
- **Challenge:** high speed interface bump isn't optimized for EWS test
- **Solution:**
  - Coaxial cable concept
  - Faraday's cage concept
  - Short needles

Bump position

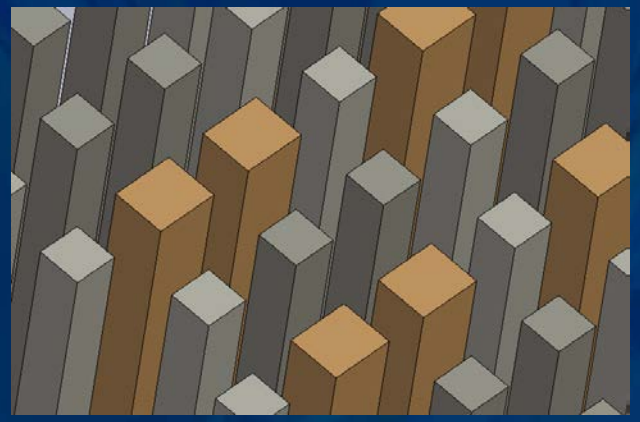


Chess configuration
min 130um pitch

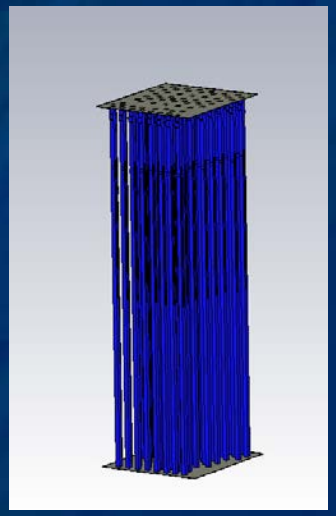
Signal bumps in red

Power and Ground
Bumps in white

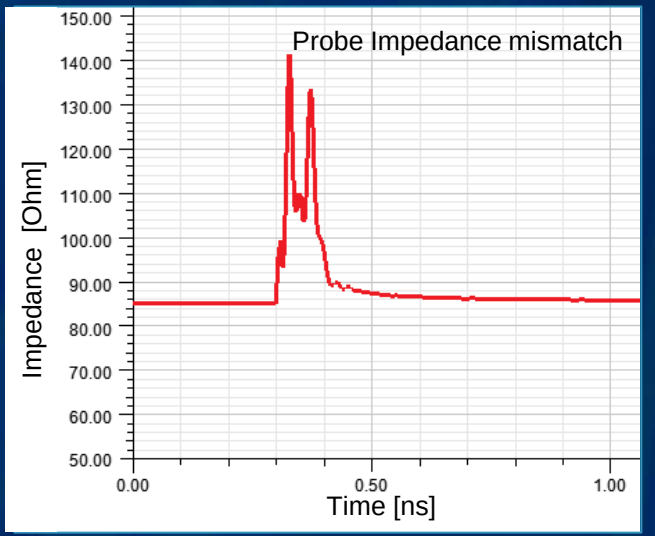
Probe position



Probe FEM model

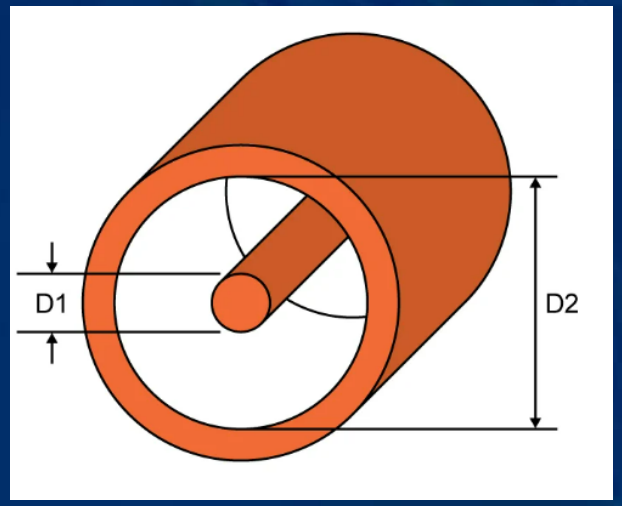


Probe impedance Simulation



Probe Head Design SI Optimization: Coaxial cable concept

- **Probe Head impedance is depending on**
  - High speed interface bump array
  - Needle technology
  - Gap between high-speed signals and reference power and ground probes
- **Idea: coaxial cable concept**



Can be optimized using Hybrid technology

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} ln \frac{D1}{D2}$$

Probe Head Design SI Optimization: Coaxial cable concept

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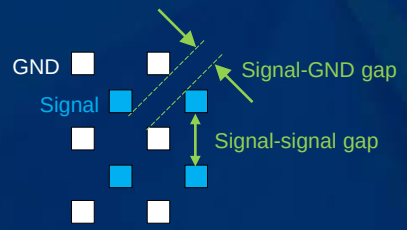
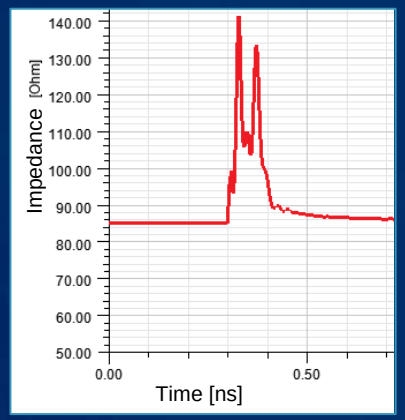
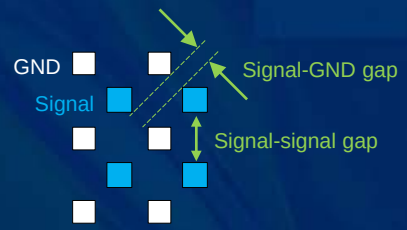
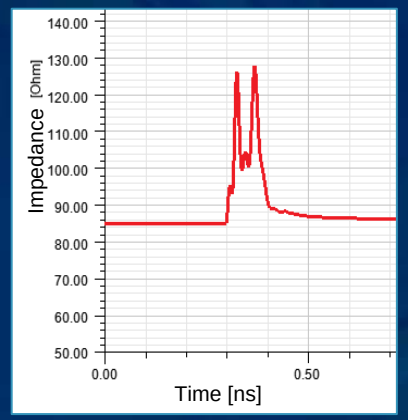
Standard cross section





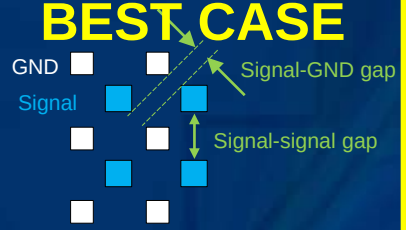
+20% cross section

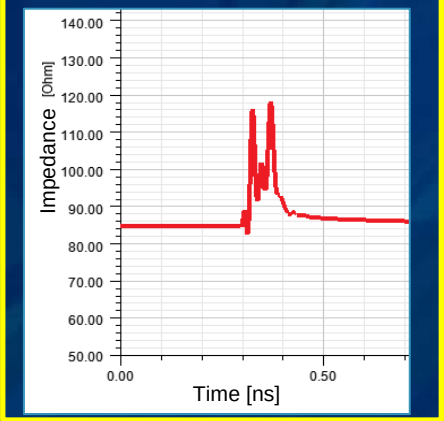




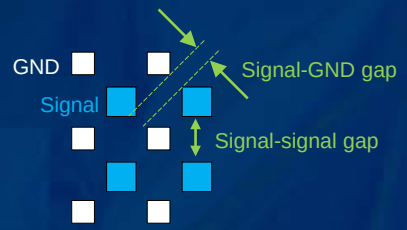
+40% cross section

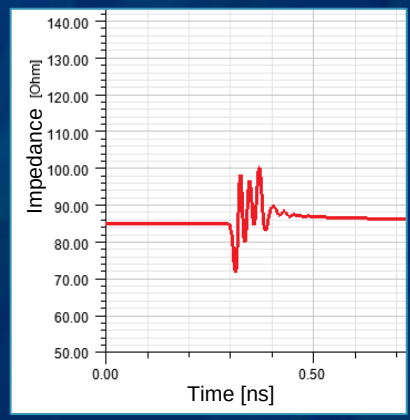
BEST CASE



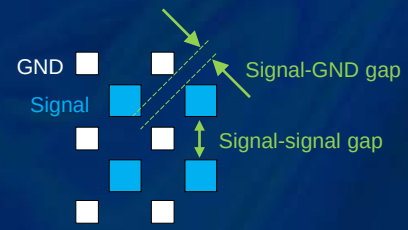


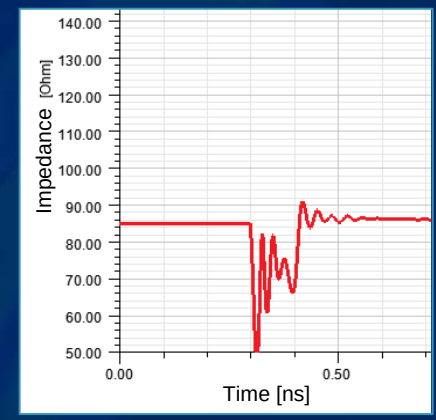
+70% cross section





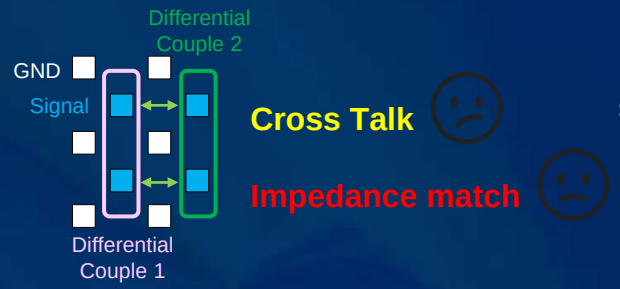
+100% cross section





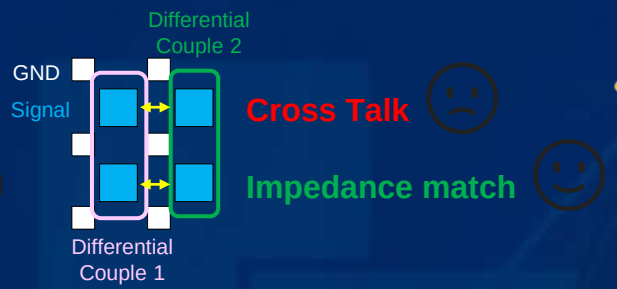
Probe Head Design SI Optimization: Faraday's cage concept

- **Signal probe cross section optimization cause Cross Talk performance downgrade**



Cross Talk

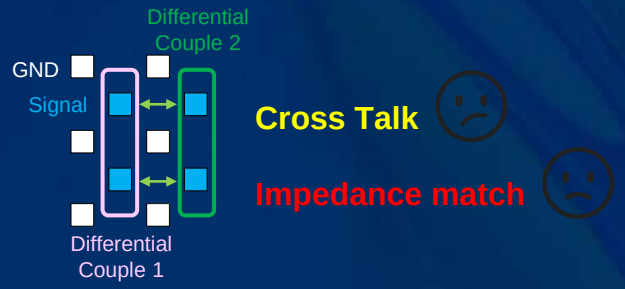
Impedance match



Cross Talk

Impedance match

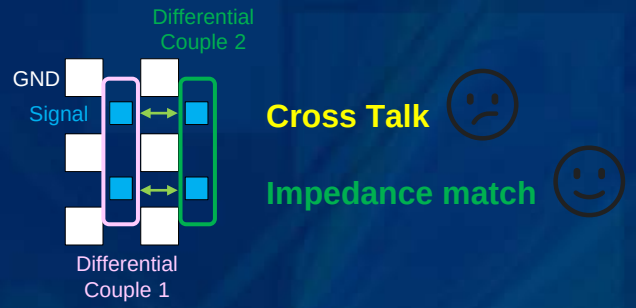
- **Idea: Faraday cage concept**



Cross Talk

Impedance match

POR

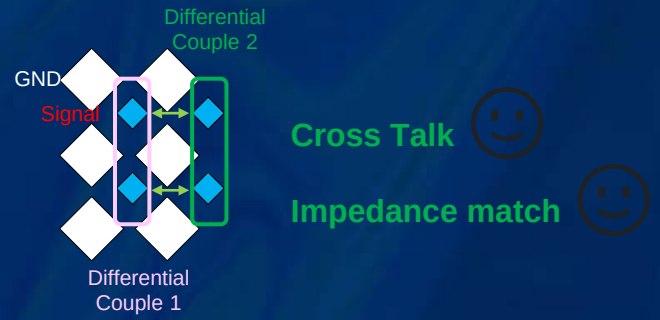


Cross Talk

Impedance match

Step1

Swap probes cross section between signals, power and ground



Cross Talk

Impedance match

Step2

Change probes rotation

Probe Head Design SI Optimization: Short needles

- **Probe Head discontinuity is probe length dependent**
- **Idea: decreasing probe length, probe head bandwidth increase**

Short probe

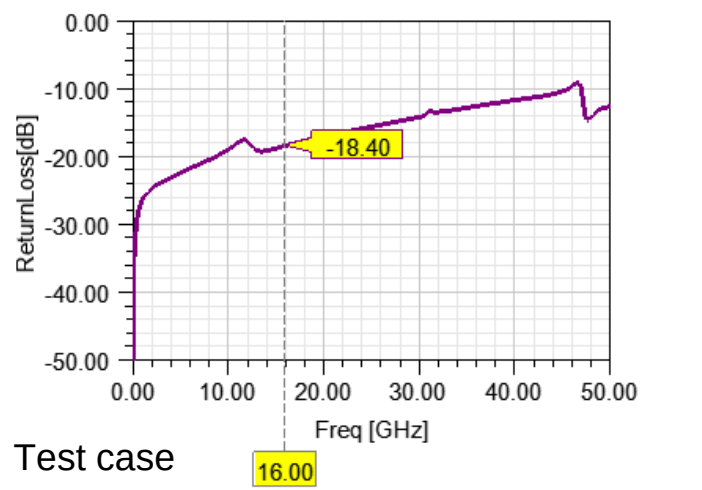
Length: reference
Intrinsic resonance: 25GHz

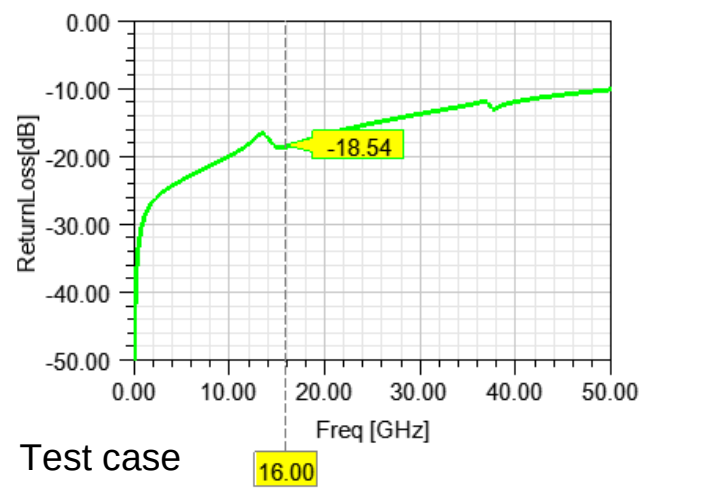
Extra-Short probe

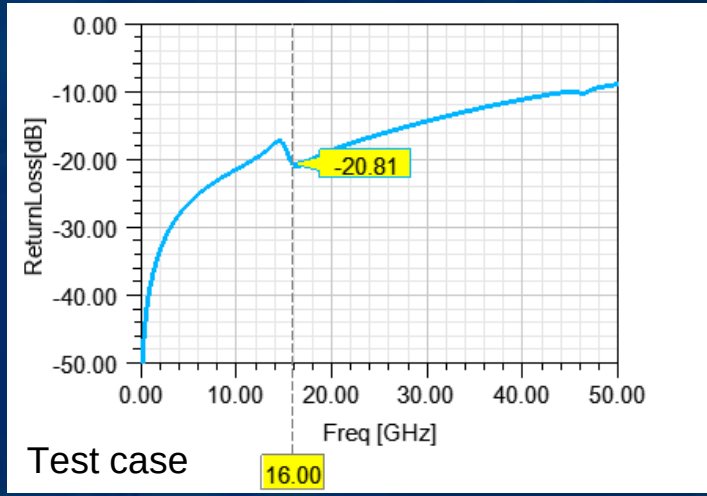
Length: reference - 25%
Intrinsic resonance: 30GHz

Ulta-Short probe

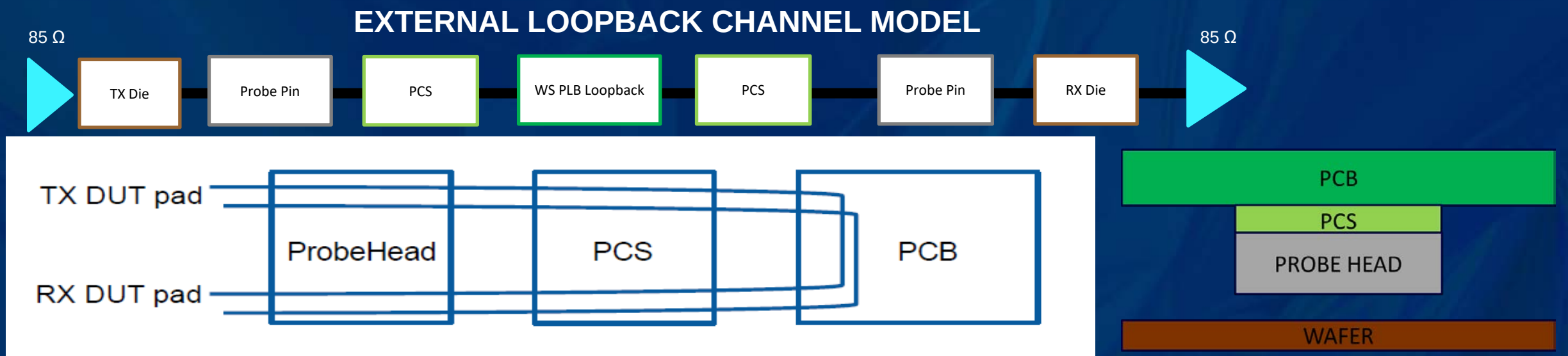
Length: reference – 40%
Intrinsic resonance: 40GHz







Probe Head Design SI Optimization: Simulation



Co-Develop with customer for the next generation *Merlion* Probes series to meet high-end HSIO test requirement

Merlion: Official mascot of Singapore. A mythical creature with the head of a lion and the body of a fish similar to a hybrid probe solution

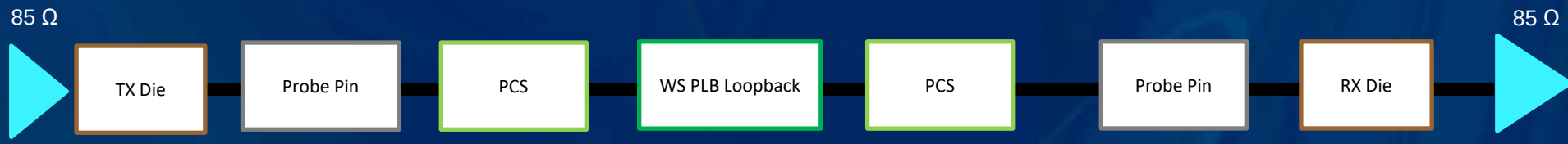
Probe Head Design SI Optimization: Simulation summary

Probe Needle (Hybrid)	Probe Length	Probe Dimension	Rotation	Probe Intrinsic Resonant	Insertion to Crosstalk Ratio (ICR)	Nominal Channel Eye Width and Height
Merlion 1	REF	CS + 40%	0°	25GHz	20dB	120mV , 0.25UI
Merlion 2	REF – 25%	CS + 40%	0°	30GHz	26dB	130mV , 0.28UI
Merlion 3	REF – 40%	CS + 40%	0°	40GHz	26dB	150mV , 0.31UI
Merlion 4	REF	Optimized	45°	27GHz	28dB	169mV , 0.32UI
Merlion 5	REF – 25%	Optimized	45°	34GHz	26dB	184mV,0.36 UI
Merlion 6	REF – 40%	Optimized	45°	40GHz	25dB	184mV,0.36 UI

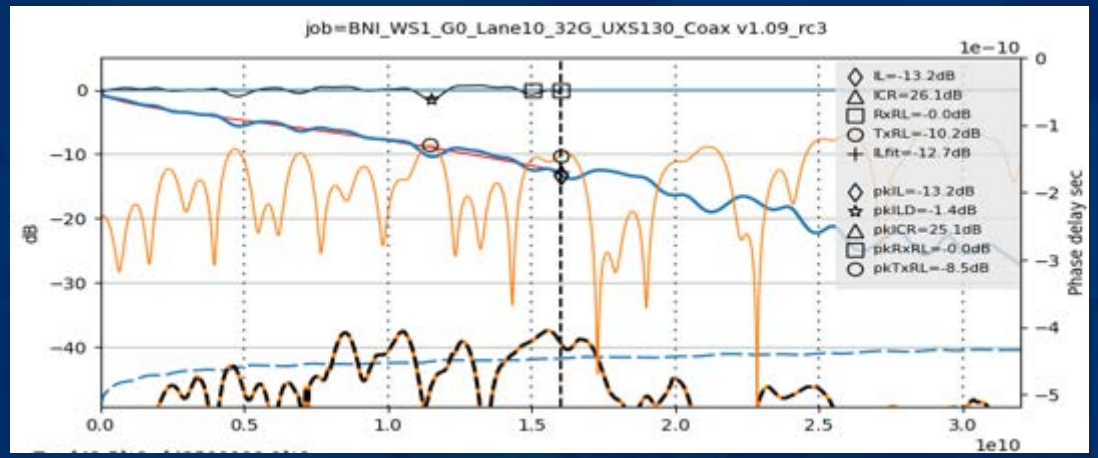
- **Probe impedance is highly influence by the C4 bump S/G pattern. Coaxial cable concept plus Faraday cage concept used in Merlion technology improves the probes SI performance significantly.**
- **Merlion 6 can meets external loopback requirement @ 32GT/s NRZ. It is the best SI performance probing solution and could potentially extend the reach to 64GT/s NRZ.**

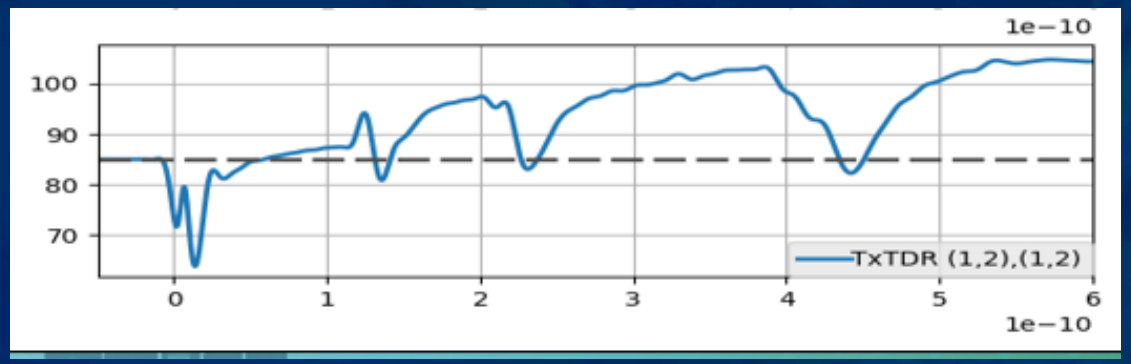
* For more detailed data refer to “High Speed Probe Card Architecture for High End Devices” Xin Reng FOO Chee Hoe LIN (AMD – Singapore) SWTest| June 5-7, 2023

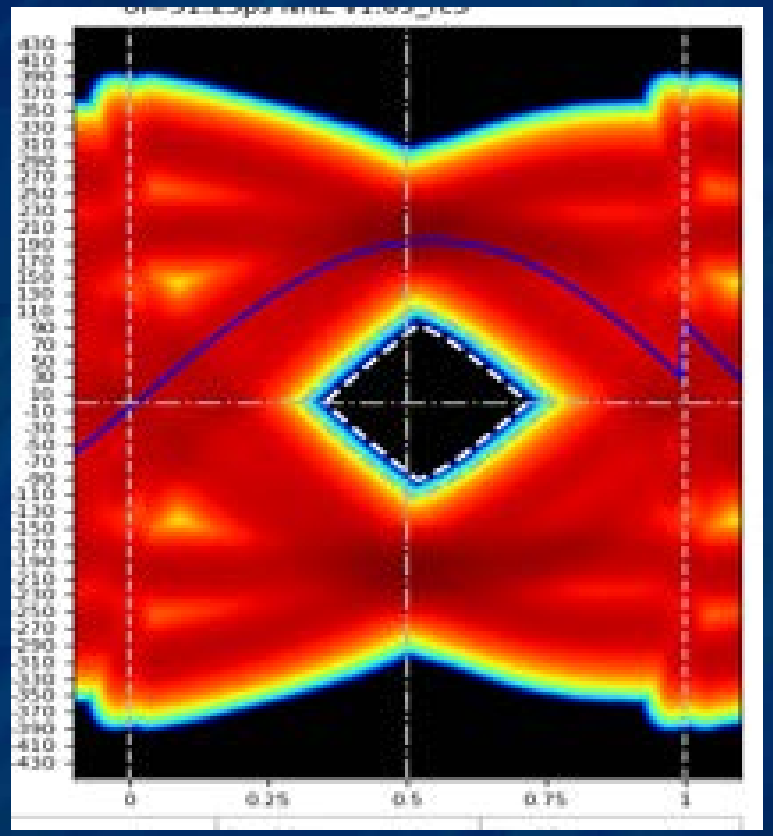
Probe Head Design SI Optimization: Simulation results



- **Merlion 6 channel simulation data , S-parameters, TDR and Crosstalk.**

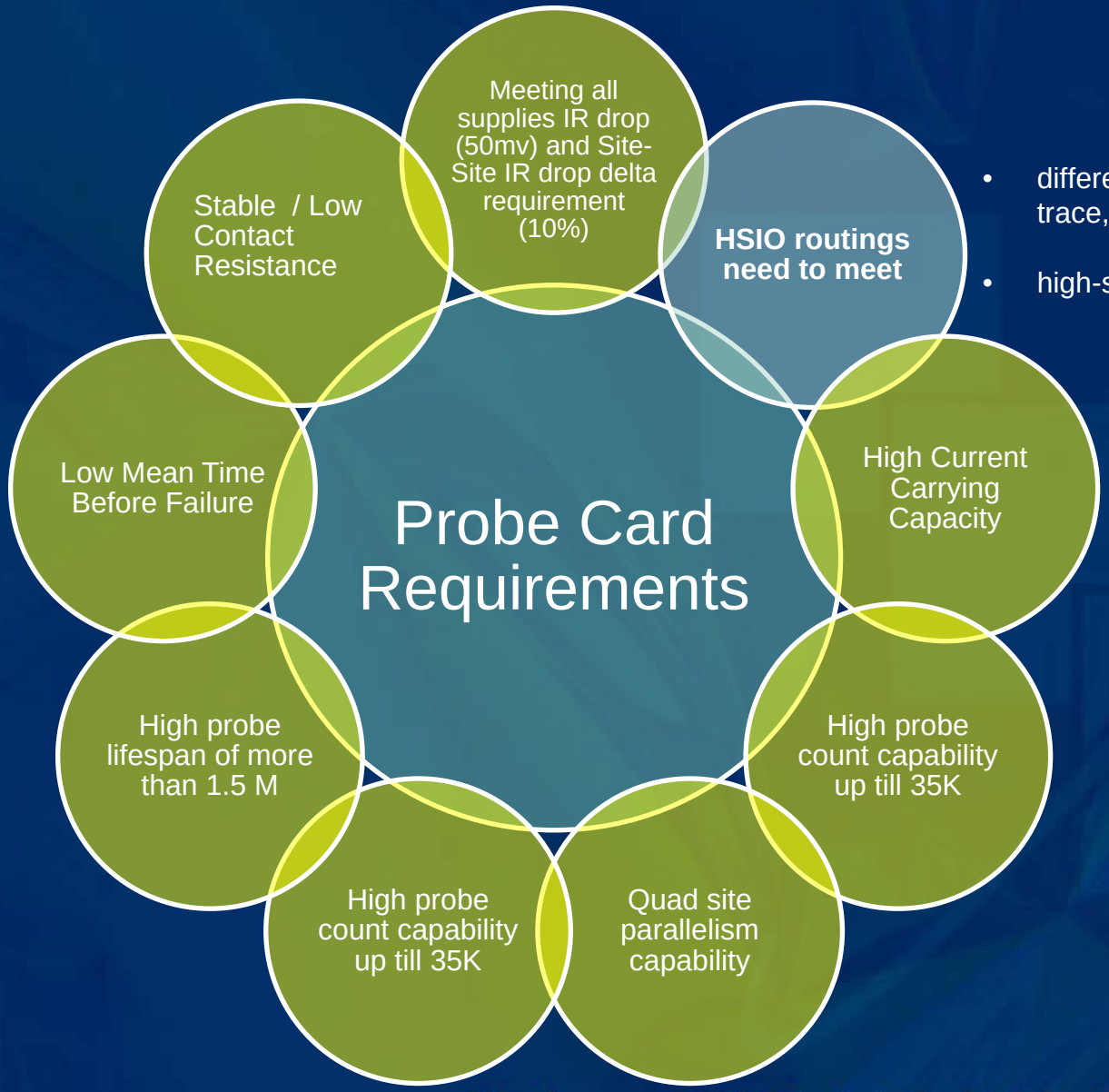






Alice Ghidoni
Alberto Berizzi

High End Probe Card Requirements



- differential / single ended impedance target for overall path (includes loopback through direct trace, relays, bias-T, and high-speed routes to ATE tester)
- high-speed end-to-end requirement for HSIO loopback path (up to 32GT/s NRZ)

Merlion 6 Probe Head

Key Features

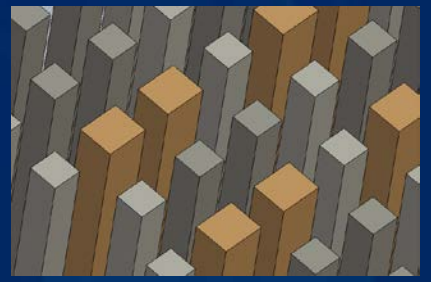
HYBRID PROBES CONCEPT

3 Different probe designs to optimize CCC/MAC and High-Speed performances

HIP (High Power PH) ARCHITECTURE

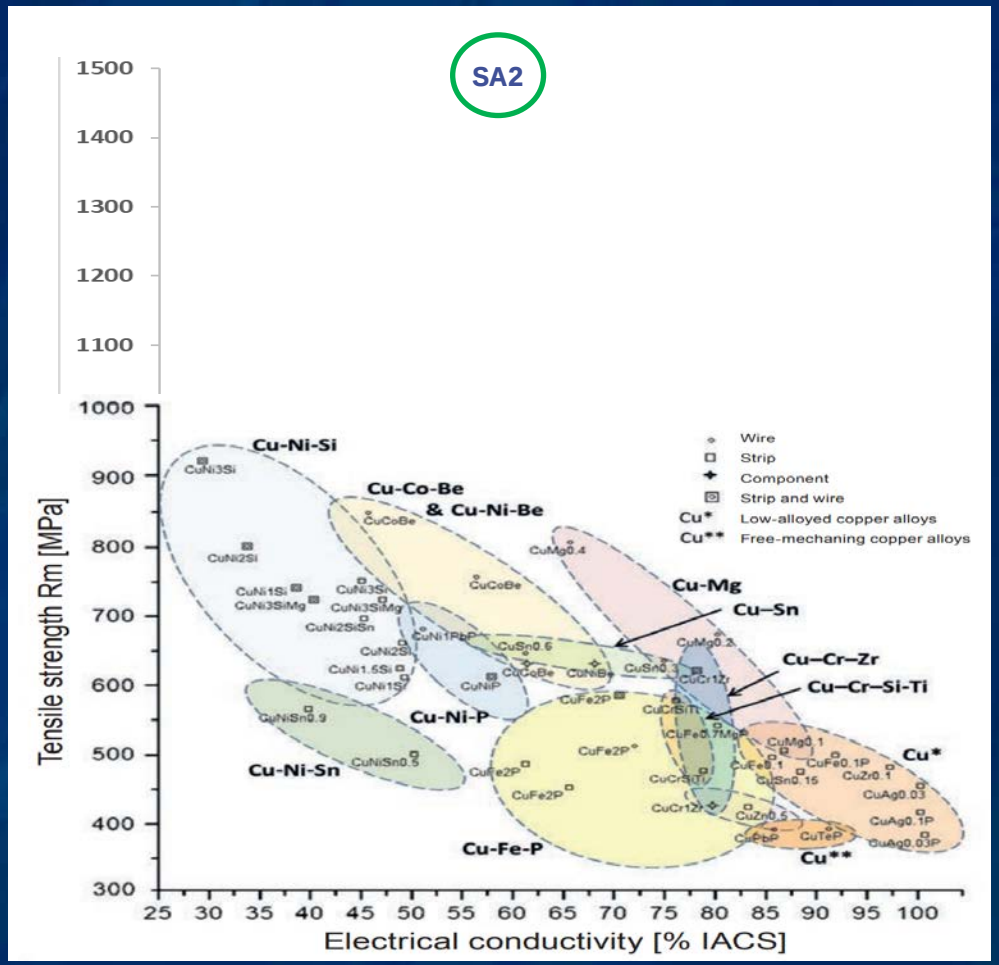
Minimize probe burnt and maximize MTBF

Hybrid Probes Solution



Technology name	Merlion 6a	Merlion 6b	Merlion 6c
Tip	Flat	Flat	Flat
XLT	YES	YES	YES
Radial alignment [µm]	8	8	8
Z planarity [µm]	Δ = 20	Δ = 20	Δ = 20
Min pitch: Linear	90 µm	100 µm	120 µm
Min pitch: Full array regular	90 µm	115 µm	150 µm
Min pitch: Full array any angle	110 µm	135 µm	170 µm
CCC/MAC [mA]	1450/1300	1500/1400	1900/1700
Force (at 75 um OT)	1.8 g	2.3 g	3.2 g
Temperature range	-45 to +175 °C	-45 to +175 °C	-45 to +175 °C
Probe alloy	SA2	SA2	SA2
Max working OD	100 µm	100 µm	100 µm

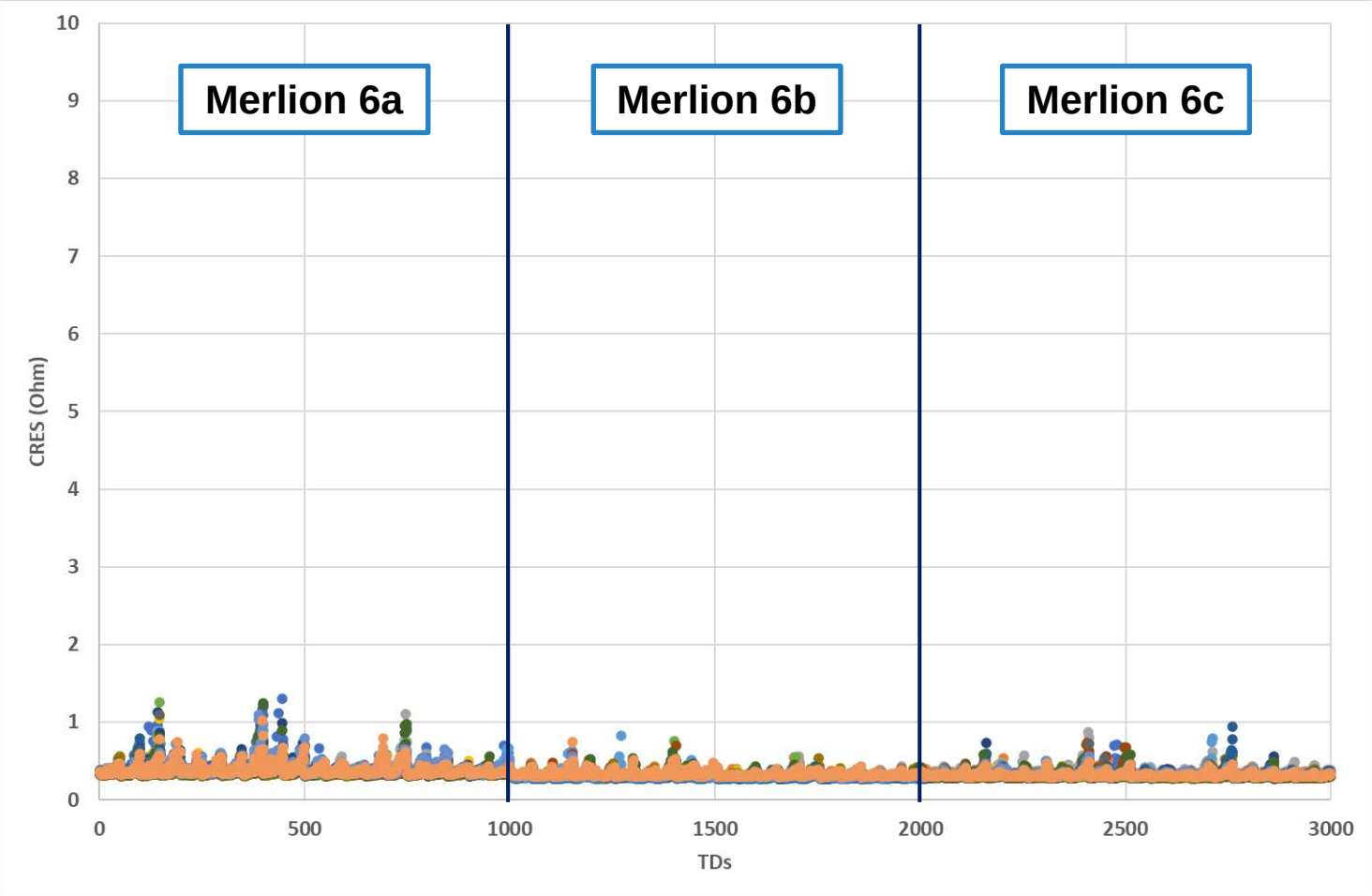
SA2 Probe Alloy



Merlion 6 – CRES Characterization

CRES tests on bumped wafer at RT

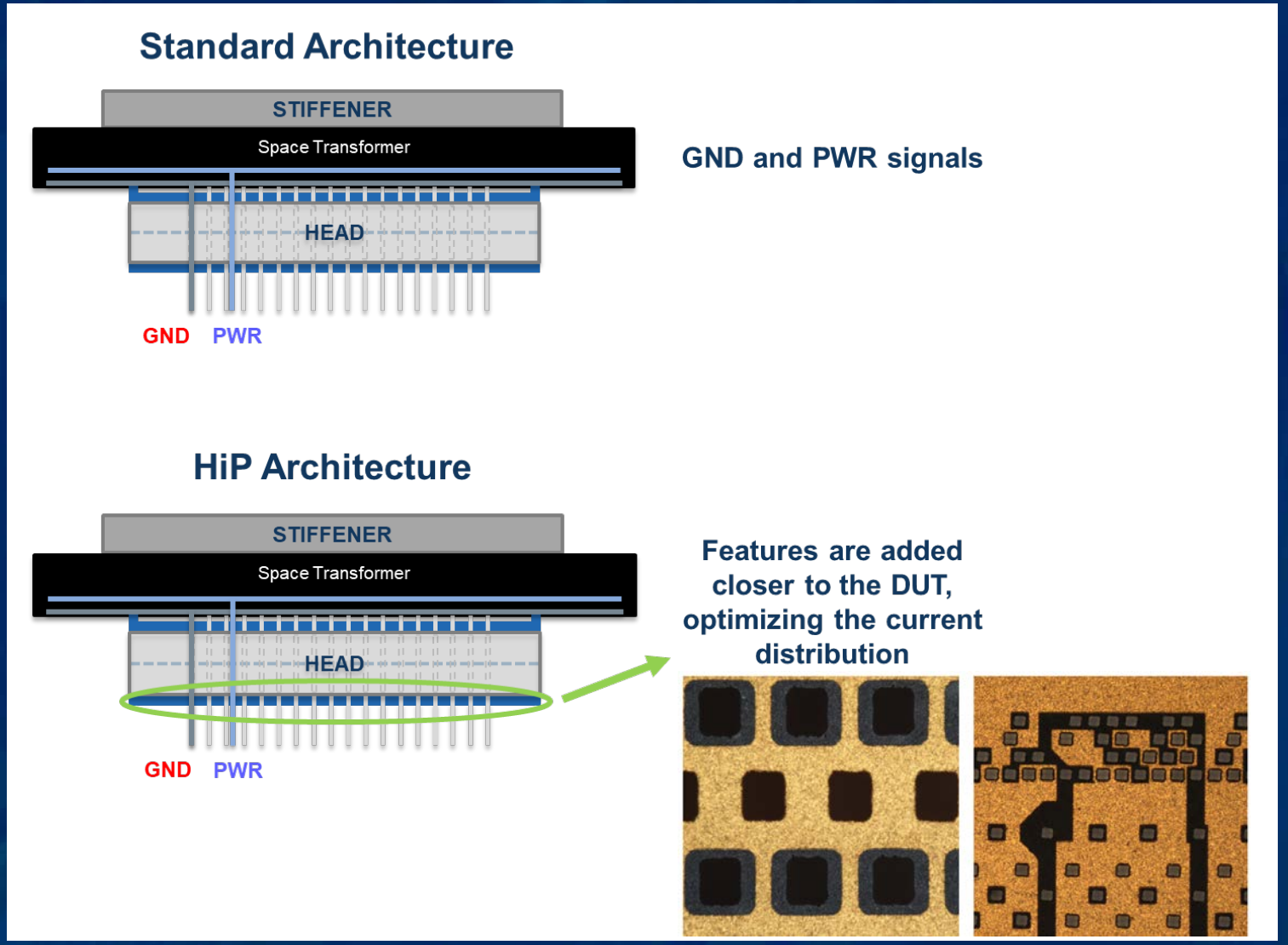
Cleaning (XY=60): 5TDs @50OT on 3M-3µm pink every 50TDs on wafer



Subtech	CRES avg [Ohm]	CRES st.dev [Ohm]
Merlion 6a	0.31	0.09
Merlion 6b	0.32	0.07
Merlion 6c	0.38	0.08

HiP PH architecture

- **TP Patented solution**
- **HiP (High Power) Probe Head:**
  - Additional features are inserted in the PH with the aim of distributing the current more evenly at PWR and GND level
  - Lithographic process (semicon-like)
  - High layout complexity: High holes of several power planes can be routed in same layers or multiple layers
  - Minimize probe burnt and maximize MTBF



HiP PH architecture

- **HiP (High Power) Probe Head:**

This results in an **increased CCC of probes**, when those are combined with HiP architecture

Technology name	Merlion 6a	Merlion 6b	Merlion 6c
Tip	Flat	Flat	Flat
XLT	YES	YES	YES
Radial alignment [µm]	8	8	8
Z planarity [µm]	Δ = 20	Δ = 20	Δ = 20
Min pitch: Linear	90 µm	100 µm	120 µm
Min pitch: Full array regular	90 µm	115 µm	150 µm
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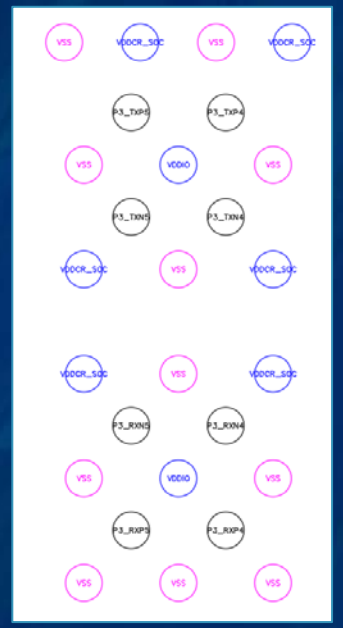
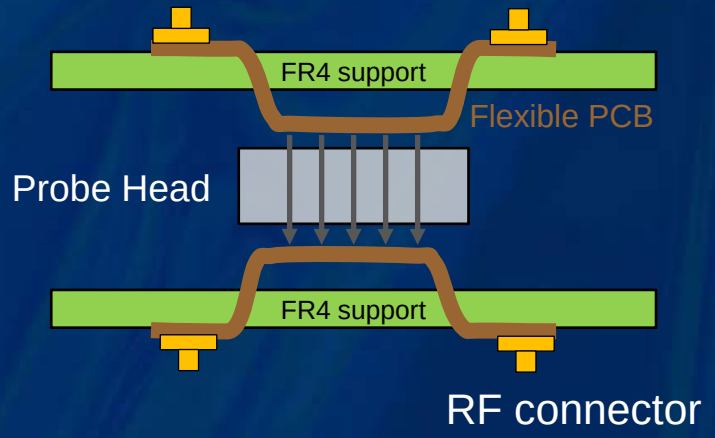
CCC/MAC [mA]	1450/1300 **HiP: 2700/2400**	1500/1400 **HiP: 2800/2500**	1900/1700 **HiP: 3000/2700**
Force (at 75 um OT)	1.8 g	2.3 g	3.2 g
Temperature range	-45 to +175 °C	-45 to +175 °C	-45 to +175 °C
Probe alloy	SA2	SA2	SA2
Max working OD	100 µm	100 µm	100 µm

Characterization Data (Test Fixture)

- Validate the frequency performances in terms of S parameter and impedance matching of the Merlion 6 Probe Heads with simulations
- Customized test fixture designed to “sandwich” the Probe Head between 50-ohm impedance-controlled traces at each end to allow VNA interface.
- Test PH with 27 Needles (8 RF Loopback and 19 GND Needles);
- Total of 16 2.92mm Connectors (8 Head side + 8 Tip side), to allow a 4 simultaneous ports measurement.





Test PH with 27 Needles (8 RF Loopback and 19 GND Needles);
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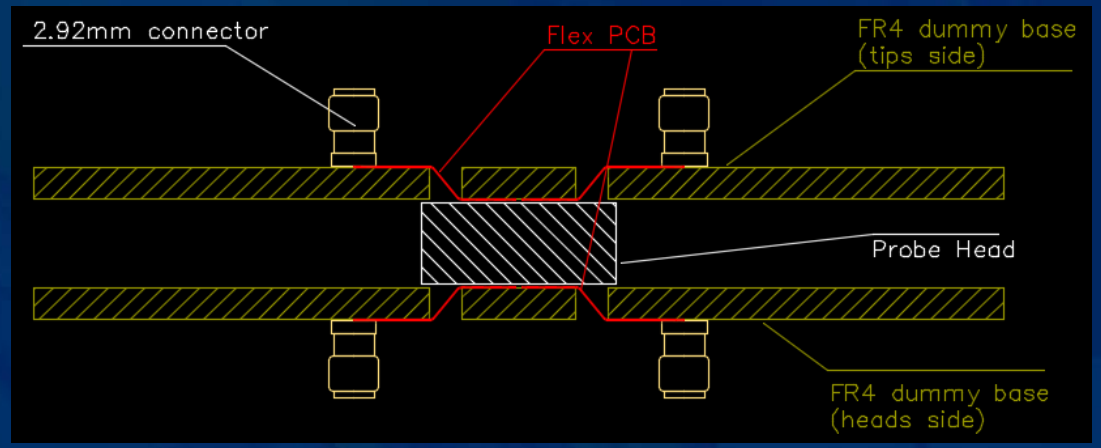
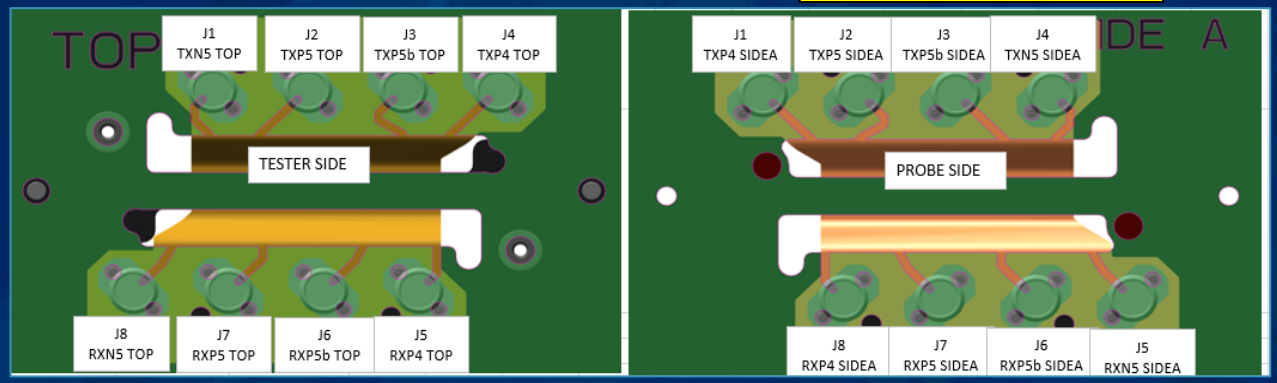
Characterization Data (Test Fixture)

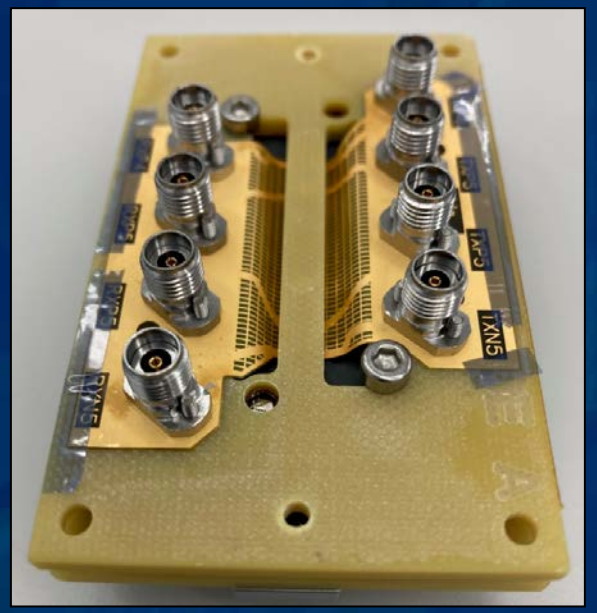


Needle Head Side

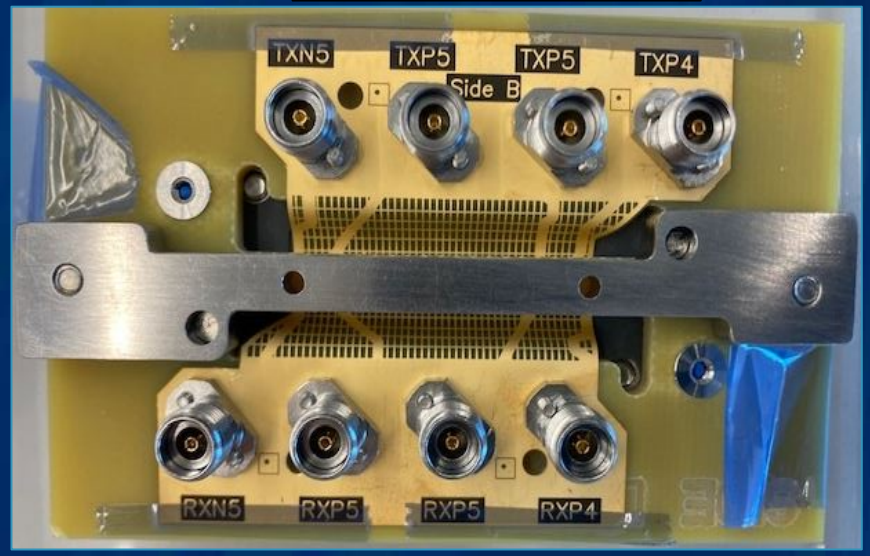
Needle Tip Side



Needle Tip Side

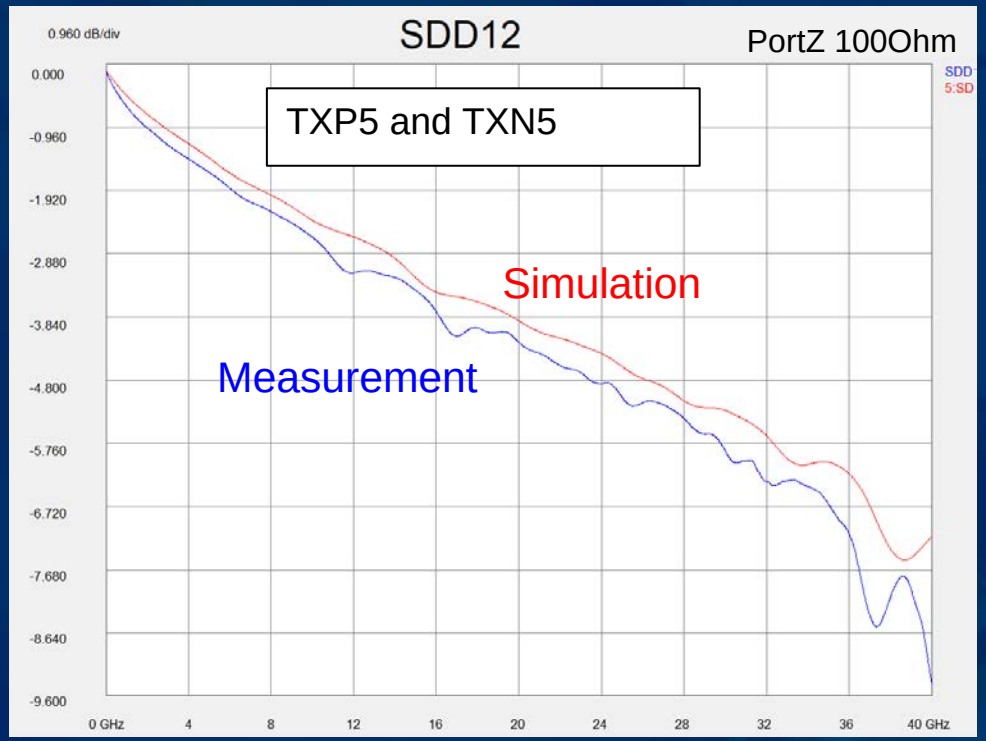


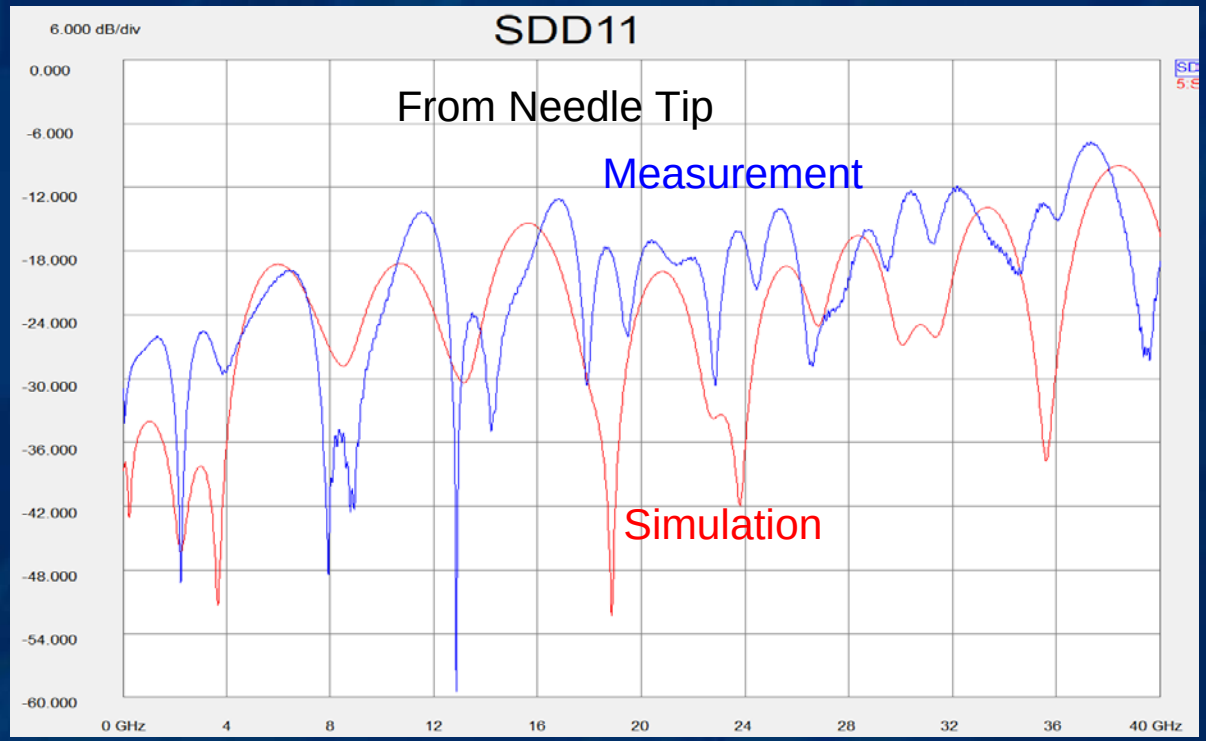
Needle Head Side



Characterization Data (Test Fixture): measures

- Insertion loss and return loss shows high degree of variability due to RF Space Transformer microstrip manufacturing tolerance, impedance mismatches between SMA connector to trace and mechanical assembly.
- Single ended crosstalk simulation of probe needle matches the measurement.

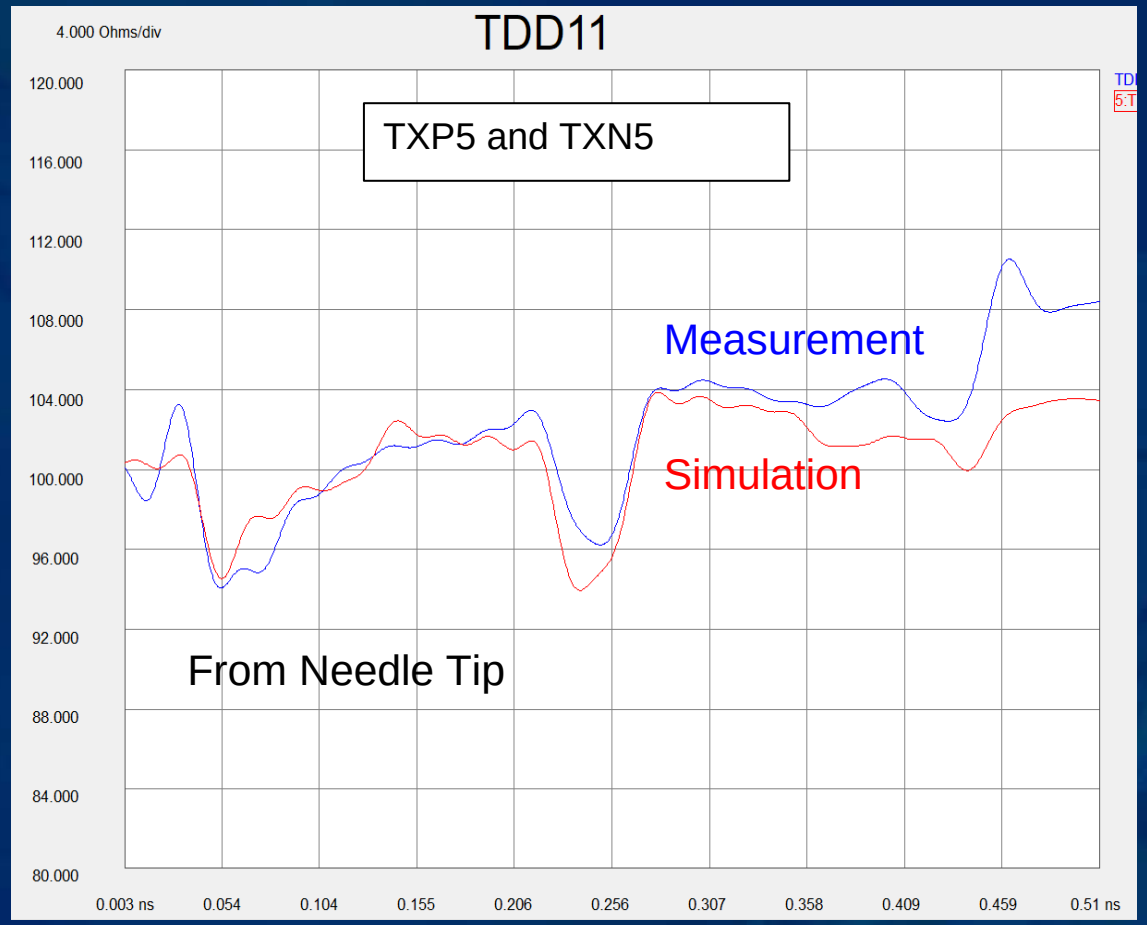


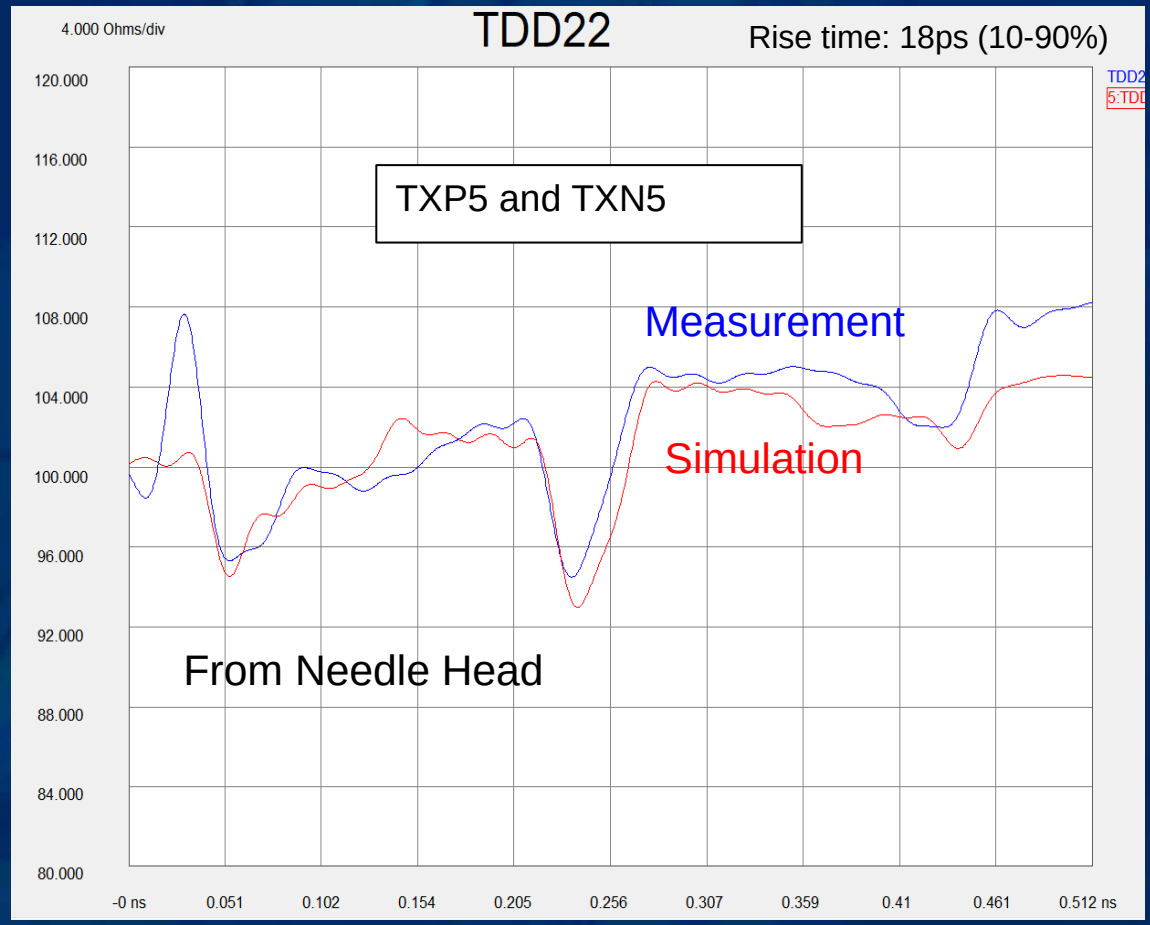


* For more detailed data refer to “High Speed Probe Card Architecture for High End Devices” Xin Reng FOO Chee Hoe LIN (AMD – Singapore) SWTest| June 5-7, 2023

Characterization Data (Test Fixture): measures

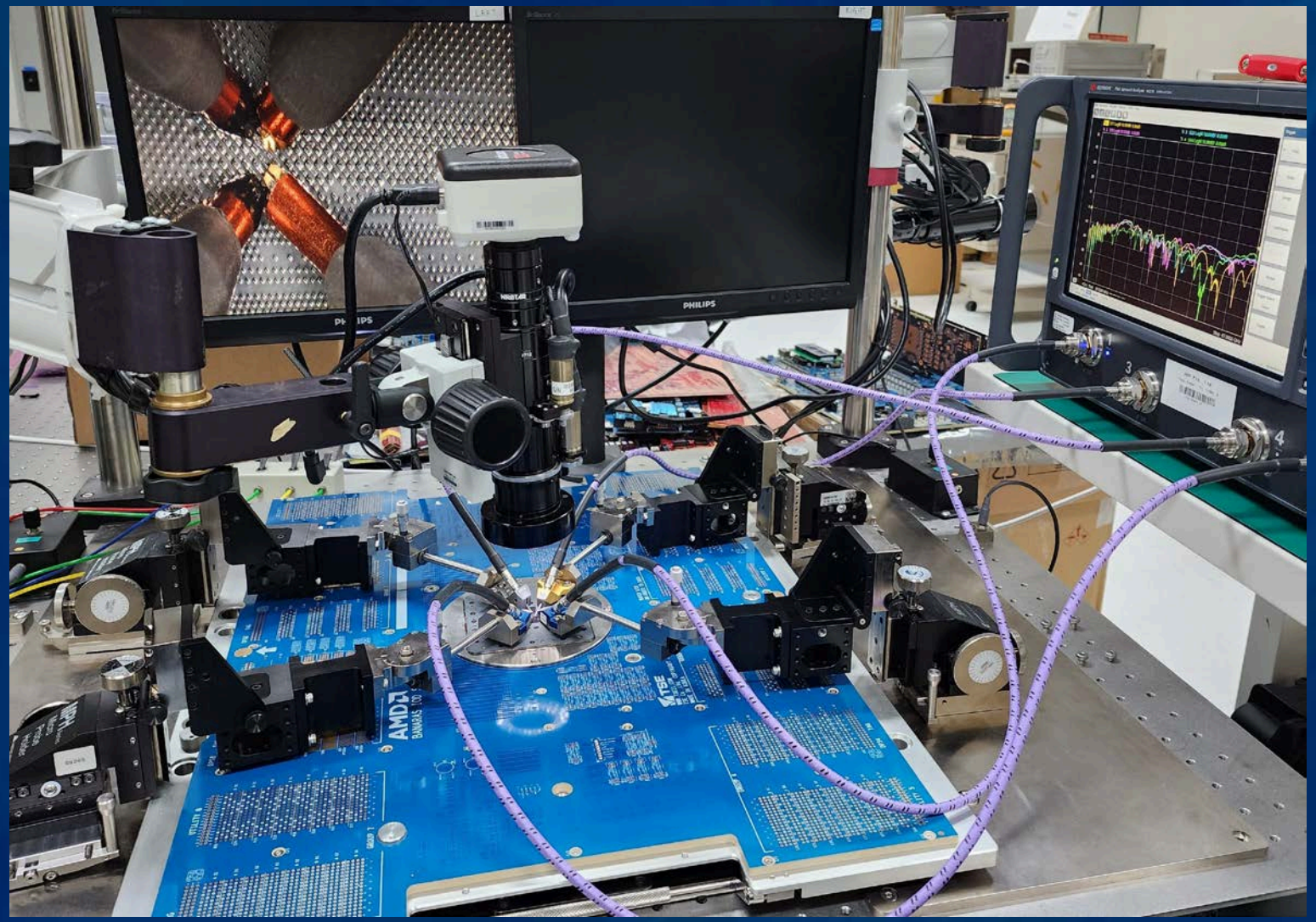
- TDR measurement shows good agreement in predicting probe head impedance profile.

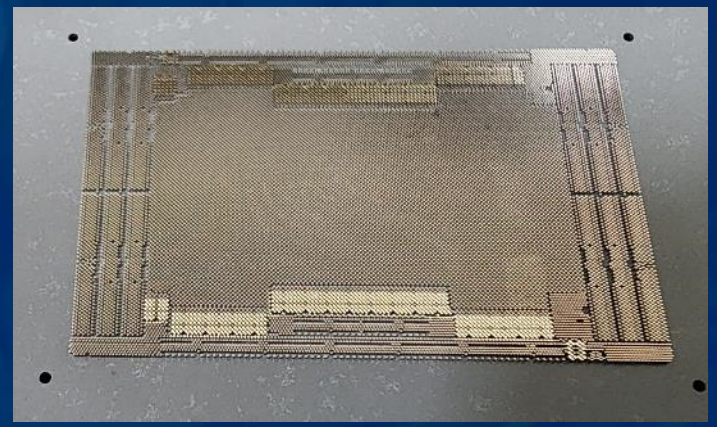




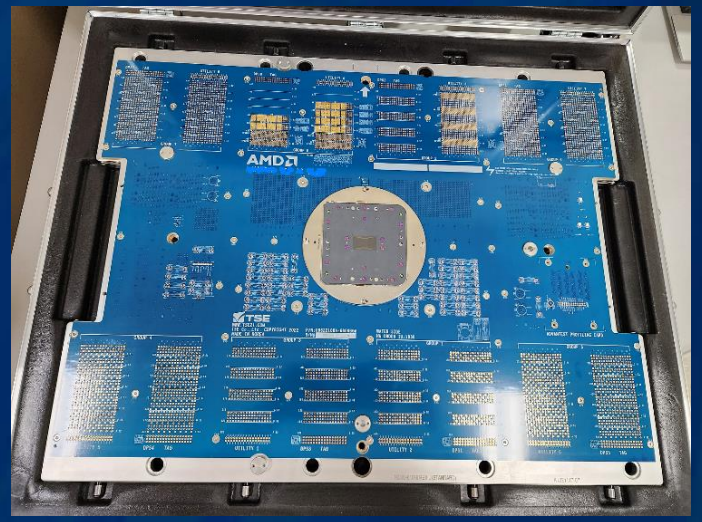
* For more detailed data refer to “High Speed Probe Card Architecture for High End Devices” Xin Reng FOO Chee Hoe LIN (AMD – Singapore) SWTest| June 5-7, 2023

Probe card External Loopback End to End measurement

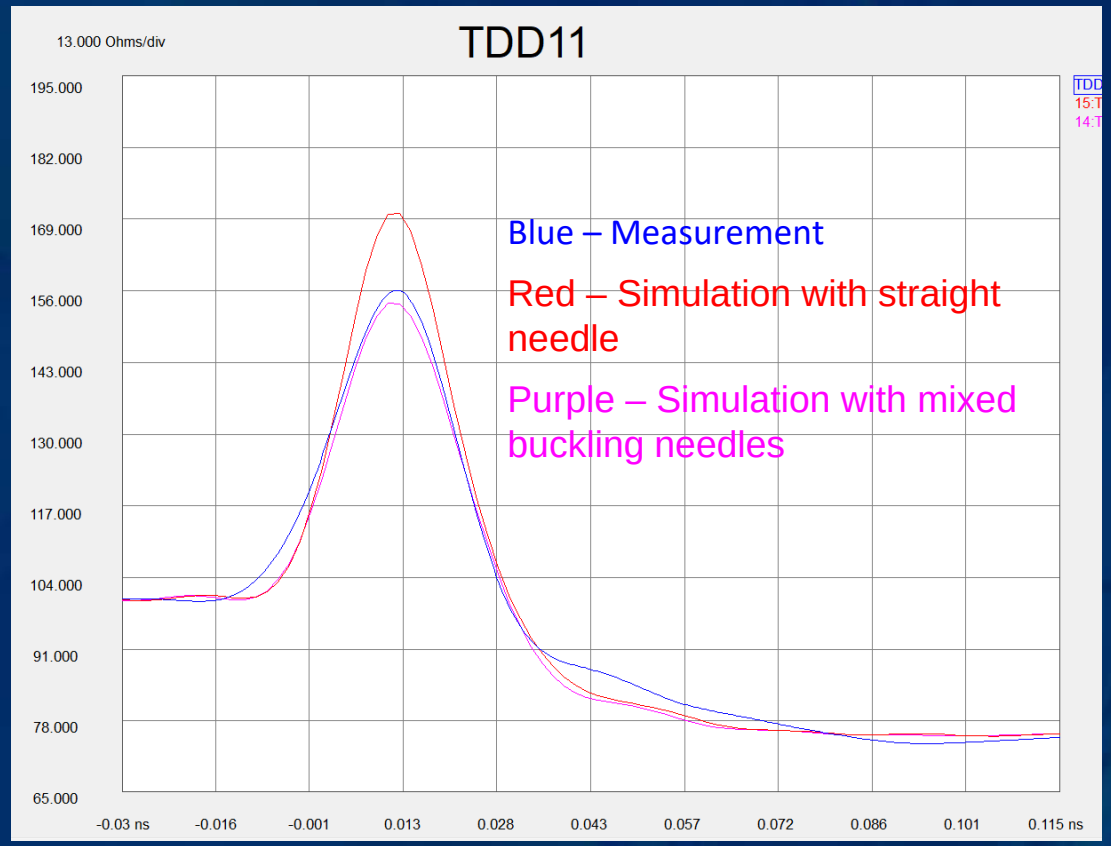




PCB + PCS+PH



End to End - DIFF TDR Simulation vs Measurement

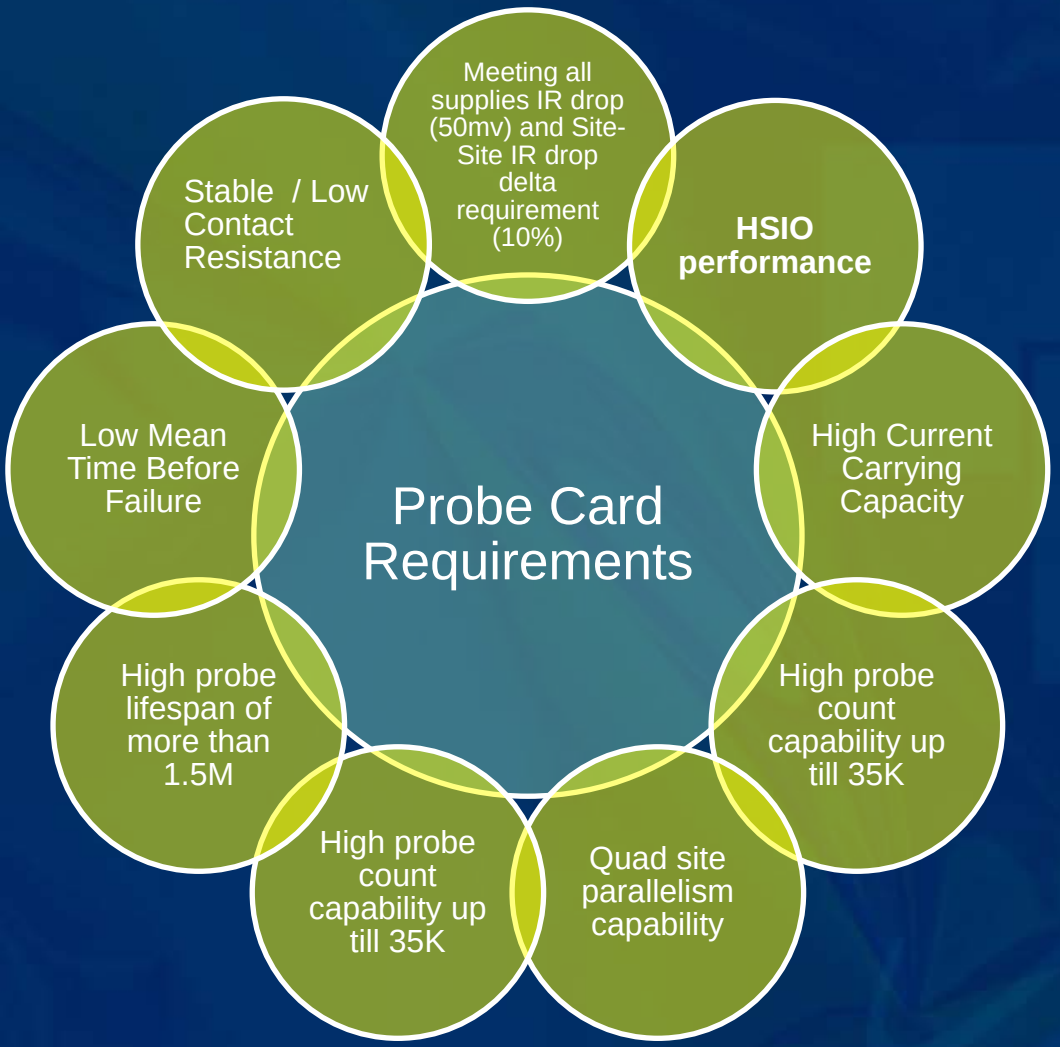


RF Ground-Signal probe

Only 1single ground probes has been considered inside measure

- Micro probing VNA measurement directly on probe needle tip is not recommended.
- Without proper connection on all probe GND on the tip side, the return current is forced through only the microprobe GND pin thus causing higher loop inductance and hence higher measured impedance.

Conclusions



MERLION 6 Hybrid Probe Head Solution can meet:

- Customer High-Speed test requirement and provide high current carrying capacity for test
- Low and stable CRES with high strength & conductivity
- High current carrying capacity for test
- Minimize probe burnt and maximize MTBF in production, thanks to HiP (High Power PH) architecture
- Simulation (TDR measurement) shows good agreement in predicting probe head impedance profile.
- De-embedded S-parameters measurement shows good IL and RL correlation with simulation.

Thanks for your Support !

Acknowledgement

The authors express their gratitude to **Xin Reng Foo** and **Chee Hoe Lin** from AMD as well as **Ivan Giudiceandrea** and **Raffaele Vallauri** from Technoprobe for their valuable contribution to this paper.

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- **Contact the SWTest Asia Team with any questions**

Complex Impedance Matching Structures for Advanced On–Wafer AiP Testing

Pratik Ghate, Ph.D.
FormFactor, Inc.

4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

Overview

- Market Drivers
- What is Antenna in Package (AiP)?
- Impedance Matching
- Challenges with Complex Impedance Matching
- Probehead Design
- Test Setup and Measurement Results
- Conclusion

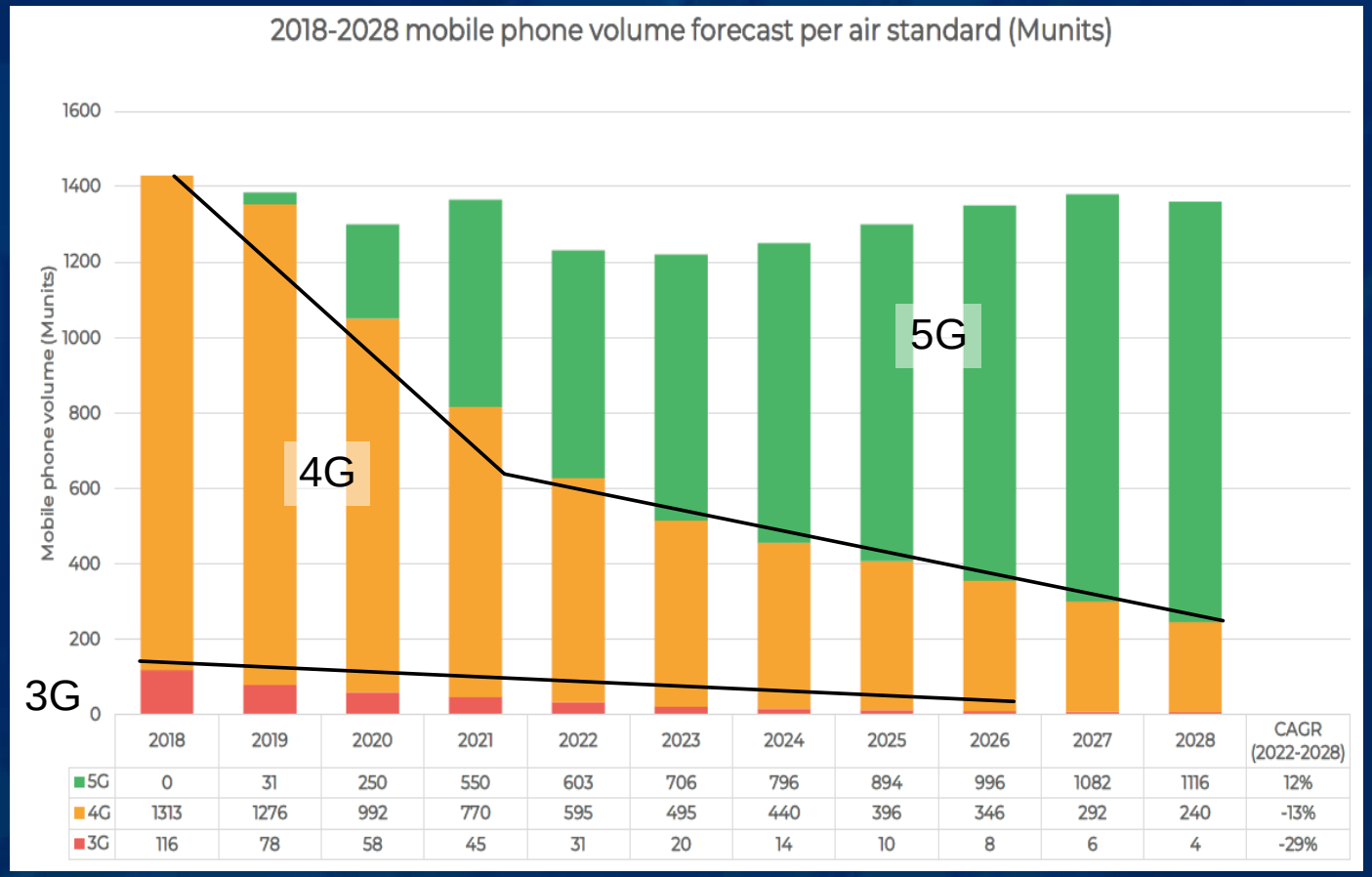
Market Drivers

5G: Smaller Better Faster

- The world's leading economies are actively deploying 5G coverage
- Demand ramp is soaring and will continue

Advantages of 5G

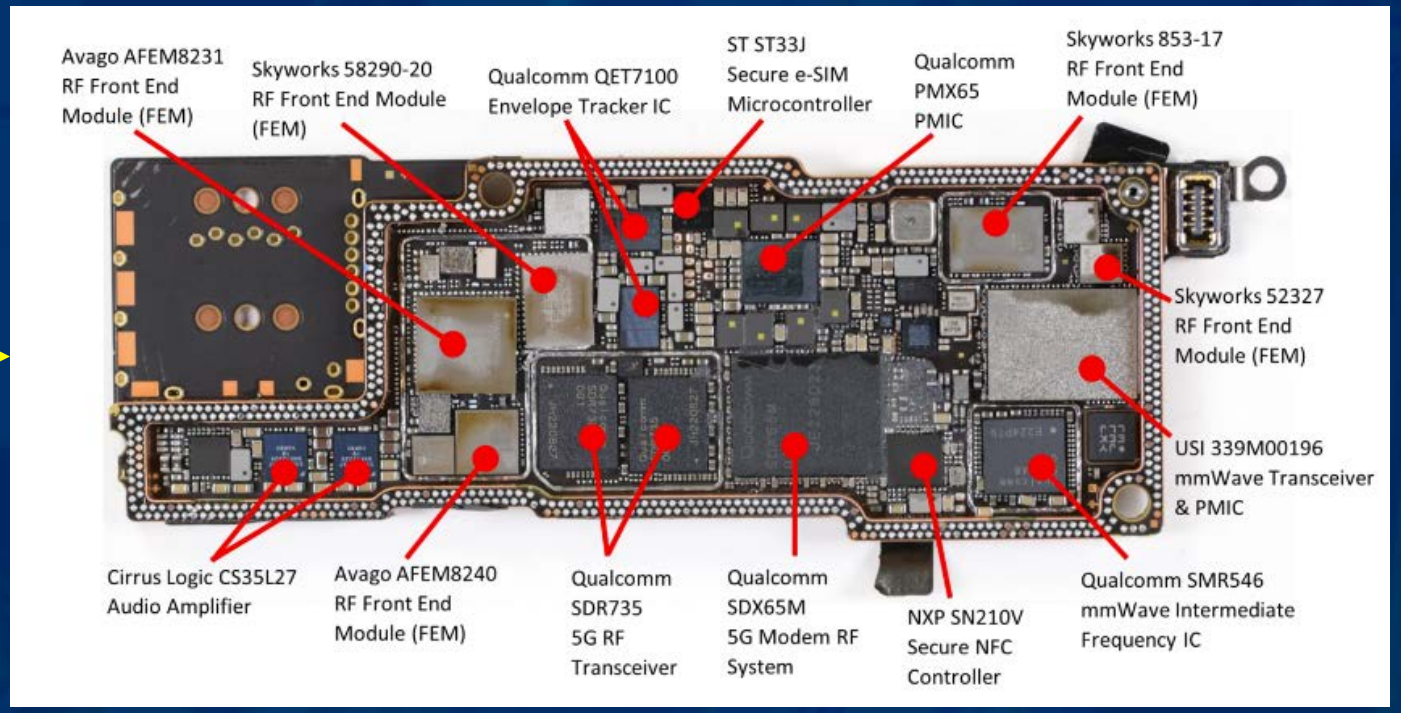
- High Speed
- Large Capacity
- Wide Spectrum
- Low Latency
- More Security



	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	CAGR (2022-2028)
5G	0	31	250	550	603	706	796	894	996	1082	1116	12%
4G	1313	1276	992	770	595	495	440	396	346	292	240	-13%
3G	116	78	58	45	31	20	14	10	8	6	4	-29%

RF Front-End for Mobile 2023 | Report | www.yolegroup.com

5G mmWave in the Handset



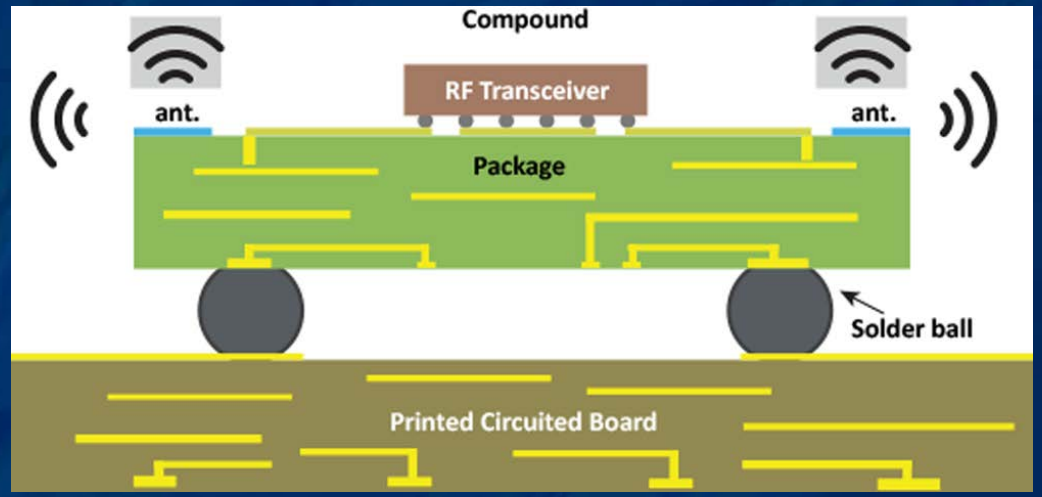
https://unitedlex.com/insights/apple-iphone-14-pro-teardown-report/

What is AiP?

- AiP (Antenna in Package) is an antenna packaging approach that implements an antenna or antennas in an IC-like package that also houses the bare RF chip transceiver.
- The AiP combination can be further integrated with front-end components such as power amplifiers (PA) or low-noise amplifiers (LNA), switches, etc.

Advantages of AiP

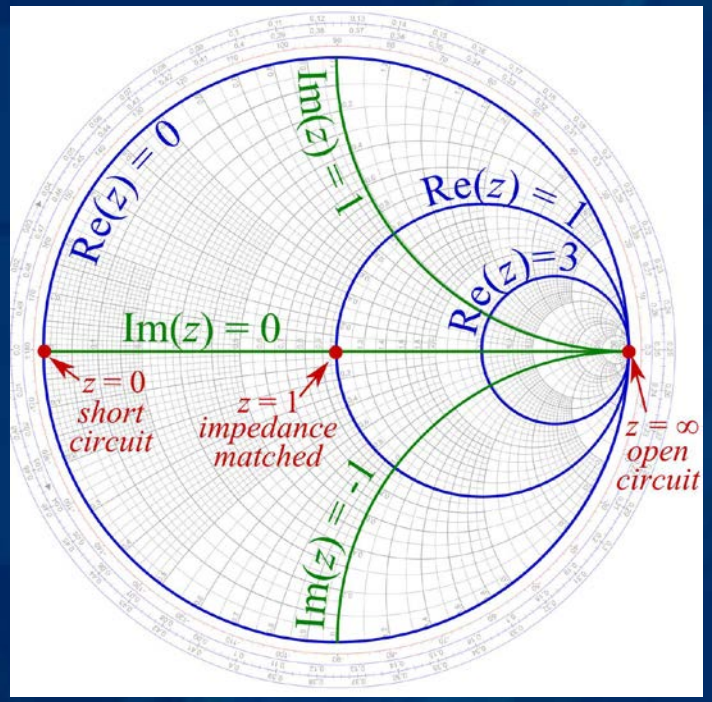
- Miniaturization of the system
- High density interconnects
- Reduction of parasitic effects
- Improved electromagnetic performance
- Design flexibility
- Applications up to 100 GHz



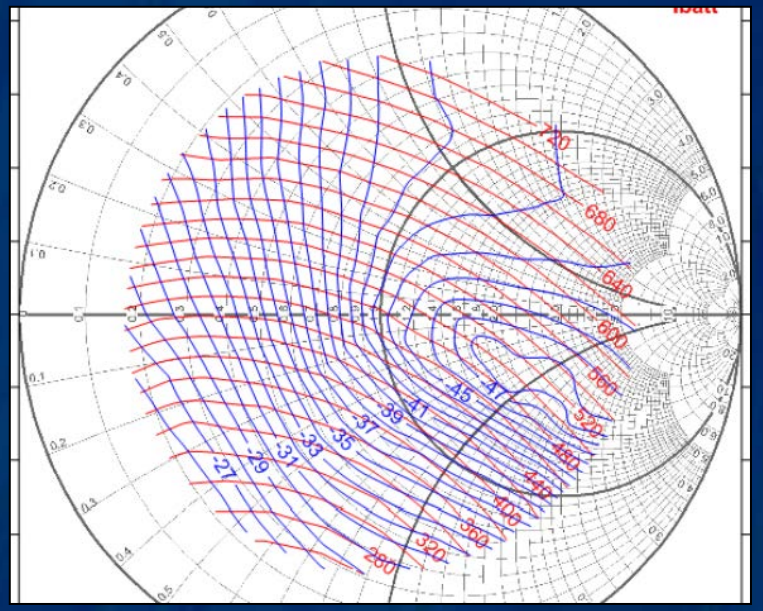
https://ase.aseglobal.com/antenna-in-package/

Challenges in Testing Antenna Drivers

- **Antenna input impedance is rarely 50Ω in the target band**
  - More optimal performance can be achieved using non 50Ω impedances
  - Varying input parameters can result in contour lines on the Smith chart
  - Matching PA (Power Amplifier) output impedance to antenna impedance minimizes reflections back into the device



Smith Chart



Typical Antenna input impedance optimization plot

Why We Need a New Test Methodology

- **Currently external circuitry is used to enable wafer-level die testing.**
  - Interfacing external circuitry to the die follows a circuitous path through multiple distinct materials
  - Transitioning between these multiple materials directly results in loss of dynamic range. This has the following detrimental consequences:
    - Increased impedance mismatch
    - Additional parasitic effects
    - Worse insertion loss
    - Reduced signal integrity
    - …
- **Takeaway: Existing methods are sub-optimal. They are:**
  - High cost (due to the need for external circuitry)
  - Have observable performance impacts resulting in loss of test precision.

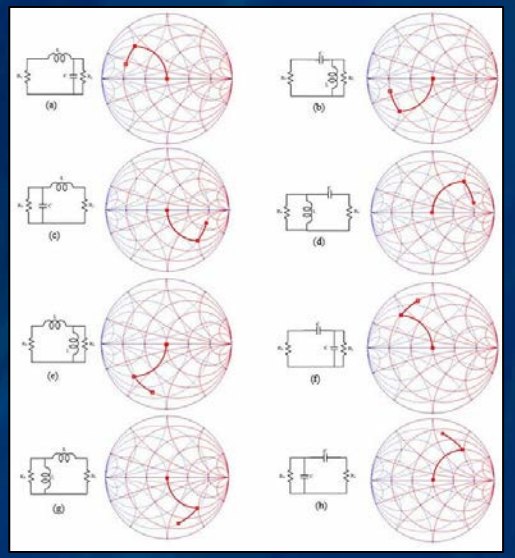
Impedance Matching

Why is Impedance Matching Important?

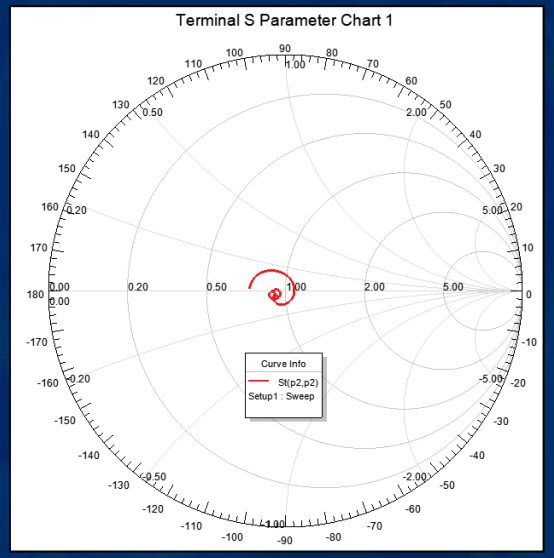
- **Impedance matching is essential to maximize the transfer of RF power or signal from the source to the load.**
- **An RF trace can be used to match two impedances between source and the load.**
- **Impedance matching can be defined in two types:**
  - Net Impedance – (R ± 0jX)
  - Complex Impedance – (R ± jX)
  - Where R is the resistance and X is the reactance (reactance can be capacitive or inductive).

Toward a Solution – Pyramid Probes

- **Pyramid Probe transmission lines can be matched to customer requested input impedances**
- **pProbe Unique Capabilities:**
  - Non-50Ω transmission lines
  - Complex impedance matching through discrete component networks
  - Impedance transitions in transmission lines
  - Transitions can occur very close to DUT



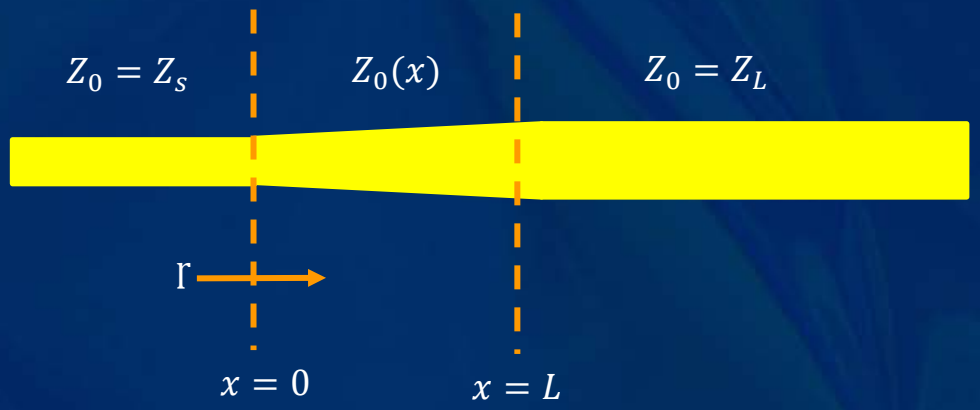
Complex impedance matching with discrete components



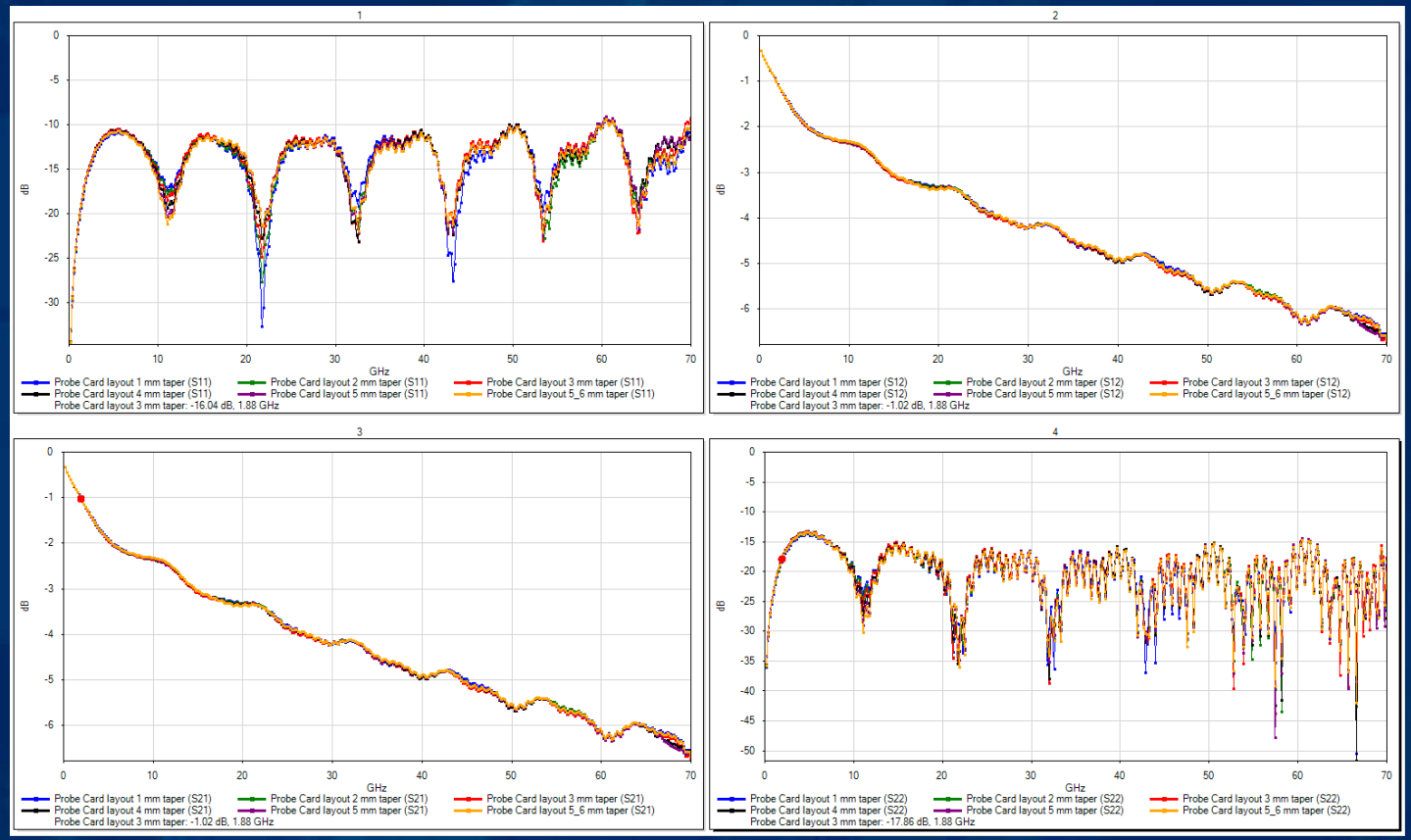
Transmission line impedance matching

Impedance Matching – Taper Approach

- **Impedance matching using a taper approach is often used for wide frequency bandwidth (0-81 GHz).**



Tapered Impedance Match



Experimental Data Results

Complex Impedance Matching

- Complex impedance (R ± jX) consists of resistance (the real part), and reactance (the imaginary part) and is responsible for the reactive power of the circuit.
- Reactance can be inductive, capacitive, or both, and is a frequency dependent parameter.

Challenges with Complex Impedance Matching

- Achieving wide bandwidth (E.g., 35-50 GHz)
- Long transmission line effects
- Challenges with passive components – Introduces parasitic effects

Complex Impedance Matching Structures

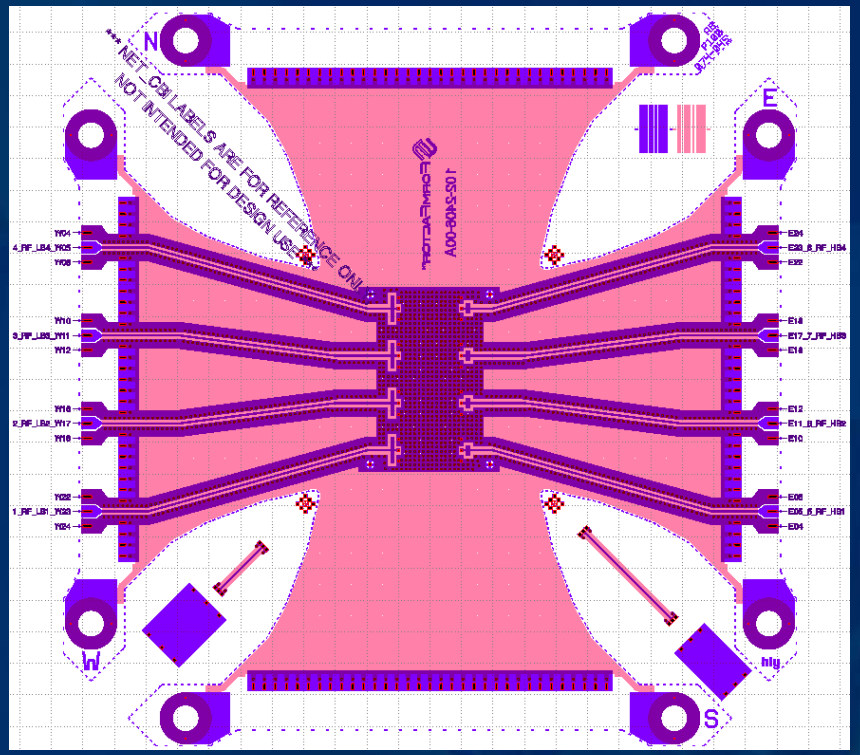
Square Capacitive Section

Circular Capacitive Section

Multiple Capacitive Section

Results

Design


N
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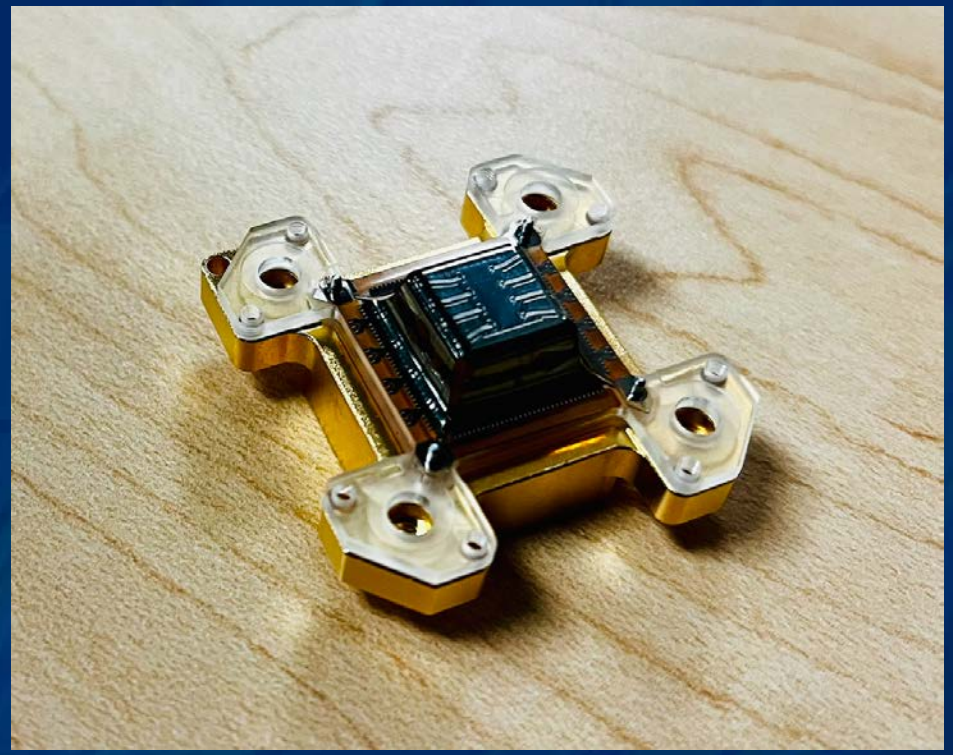
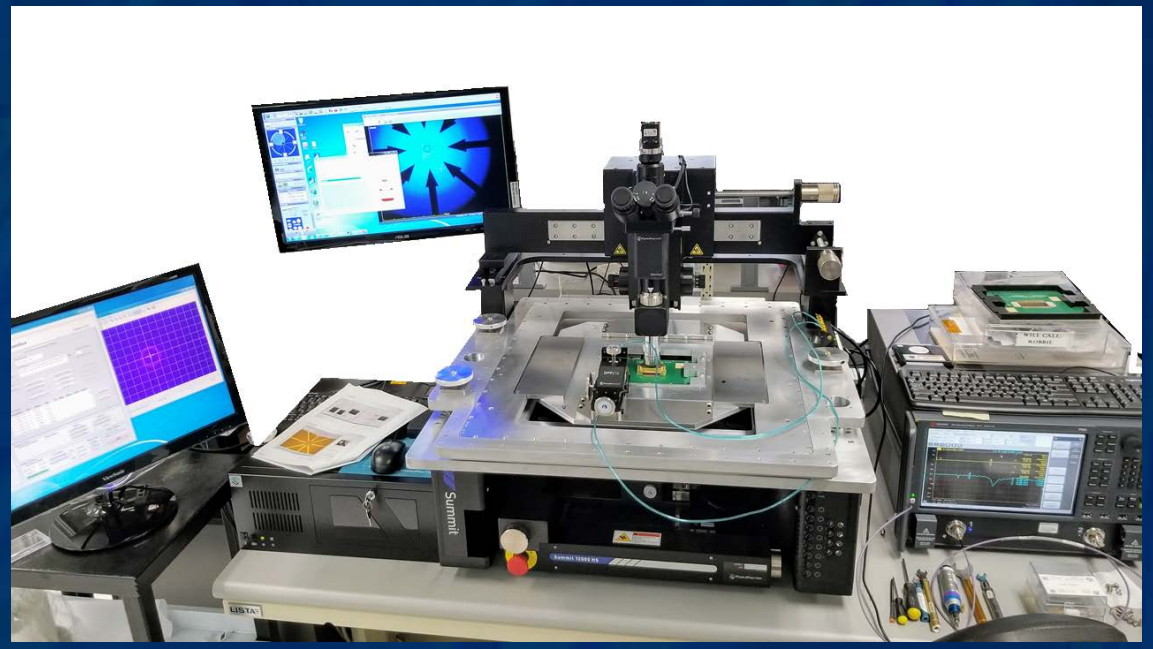
*** NET_CB LABELS ARE FOR REFERENCE ONLY
NOT INTENDED FOR DESIGN USE ***

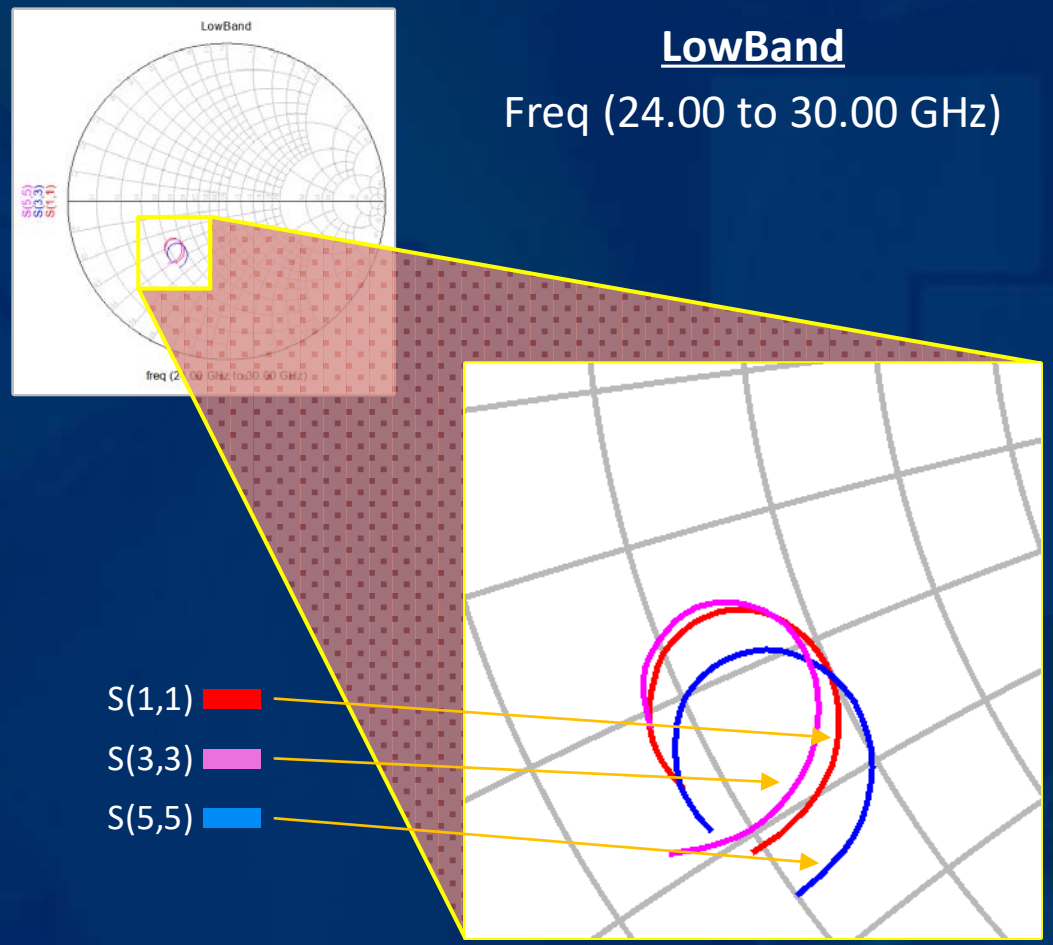


Test Setup

- **FFI Summit 12000 semi-auto station**
- **Keysight PNA with 4-port capability**
  - 50 MHz – 67 GHz
  - 201 points
- **Use the Keysight eCal for cable calibration**
- **Use eLRRM for Probe Calibration**
- **ISS: 106-682-00**
- **Core: RFC**

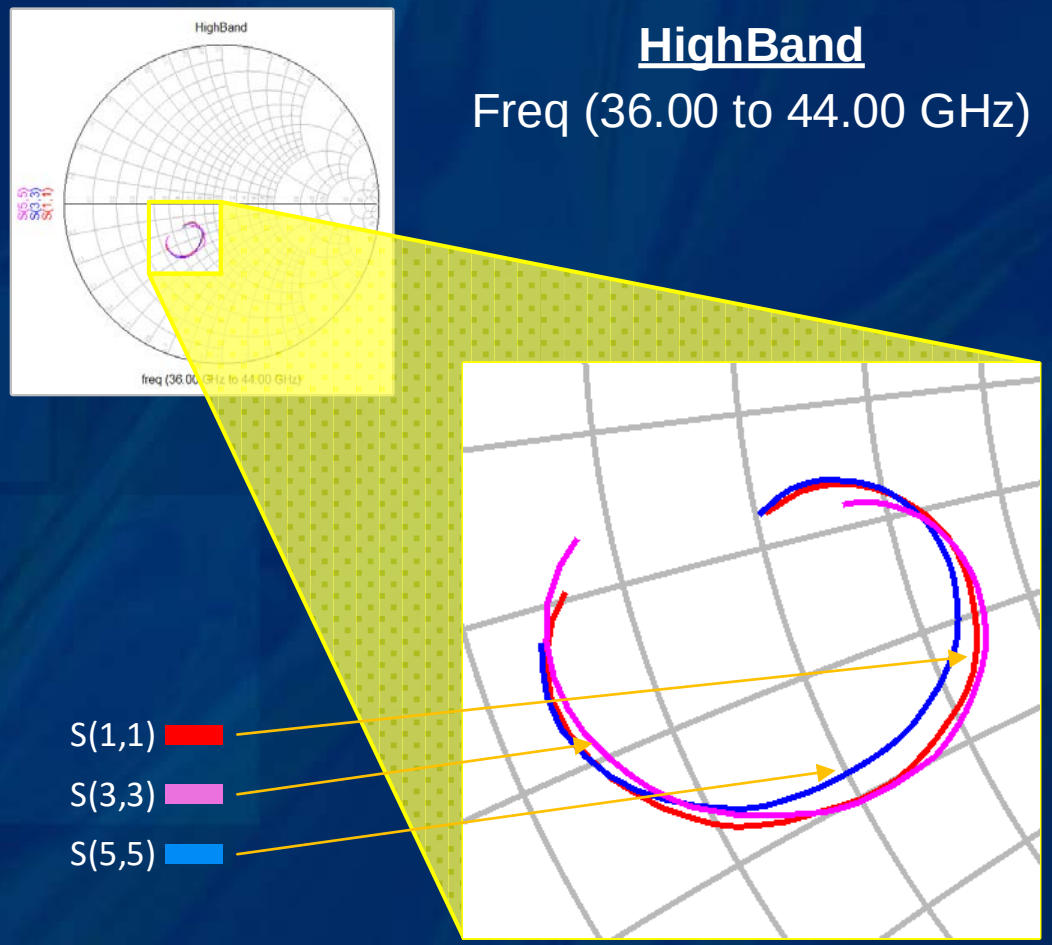


Measurement Results



LowBand

Freq (24.00 to 30.00 GHz)



HighBand

Freq (36.00 to 44.00 GHz)

Conclusion

- **We have proven that with Pyramid probes complex impedance matching is possible.**

- **This offers significant benefits including:**
  - Eliminating the use of external circuitry
  - High-performance efficiency
  - Cost reductions

Questions?

Focusing on a New Challenge within Advanced Vertical Probe Card Guide Plate Drilling

Chris Stokes
Oxford Lasers

4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

Overview

- Introduction
- Motivation
- Measuring Guide Plate Key Metrics
- Sources of Error
- Solution and Results
- Summary
- Follow on Work

Introduction

Oxford Lasers specialize in the manufacture of advanced vertical guide plates :

Over 20 years experience in guide plate production

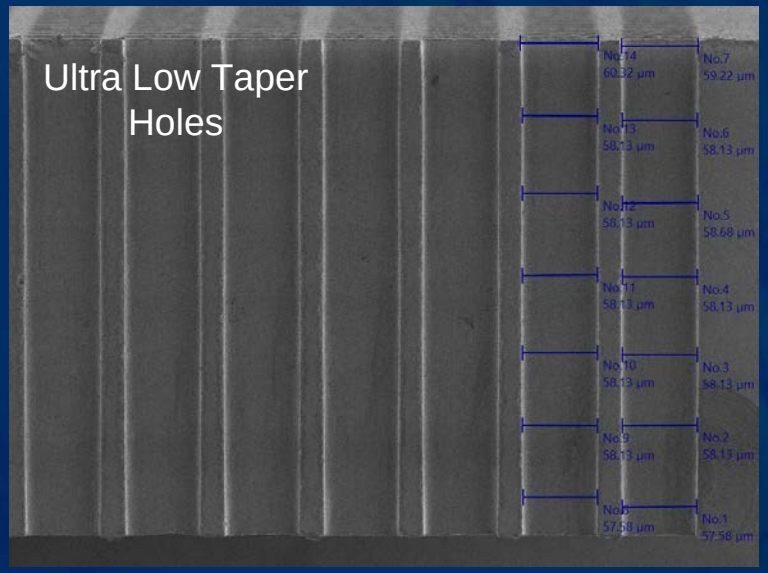
World Class subcontract micromachining facility

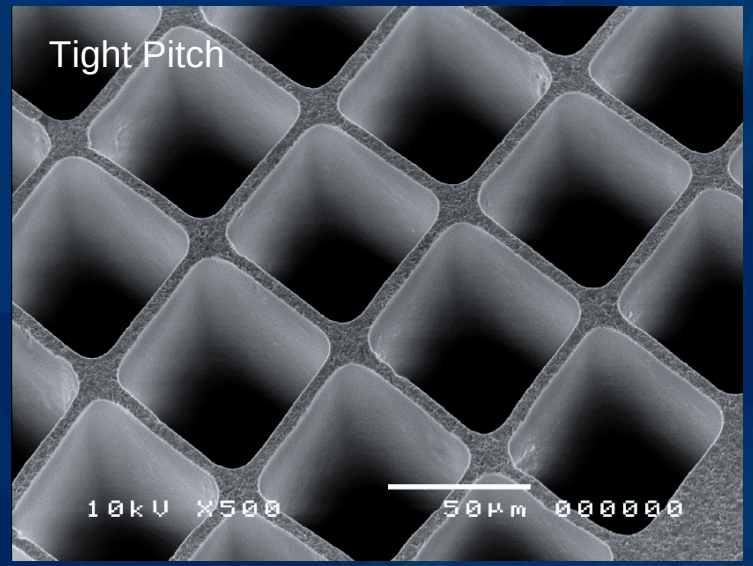
Manufacturer of production laser tools

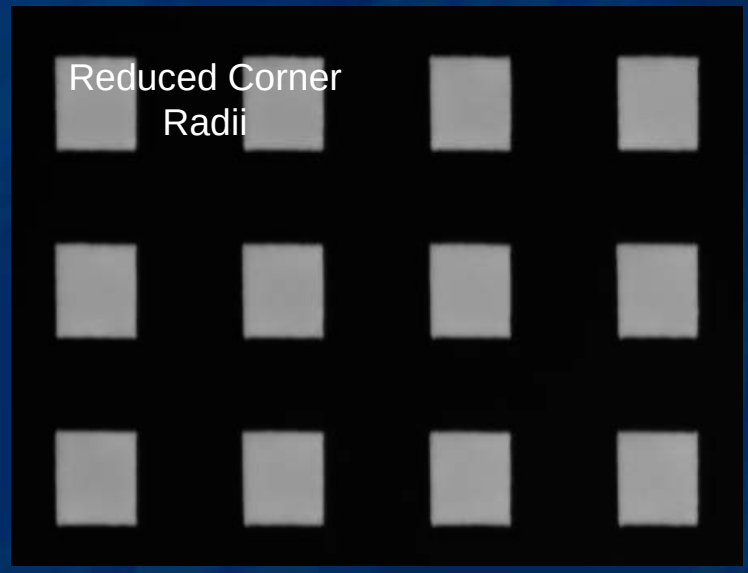
Laser Micromachining :
Ceramics, Polymers, Metals and Glasses

Introduction

Examples of laser micromachining for Wafer Test:







Motivation

Trends in Vertical Probe Cards :

1) **Smaller Holes < 30 microns** ✓
2) **Tighter Pitch < 10 microns between holes** ✓

The focus of this presentation will be the improvement of guide plates for advanced Probe Cards :

In particular the need for improved positional accuracy

Position Error Improvement

What are we trying to improve ?

Here we are looking to improve the error in the position of the drilled micro holes when their actual position is compared to drawing.

This position error can be :

a) Relative to alignment holes on the guide plate itself or

b) Relative to the individual micro holes themselves

Current Requirements : < 3 microns

Future Requirements : < 1 micron

Sources of Error

1) Drilling Tool : thermal stability of mechanical design

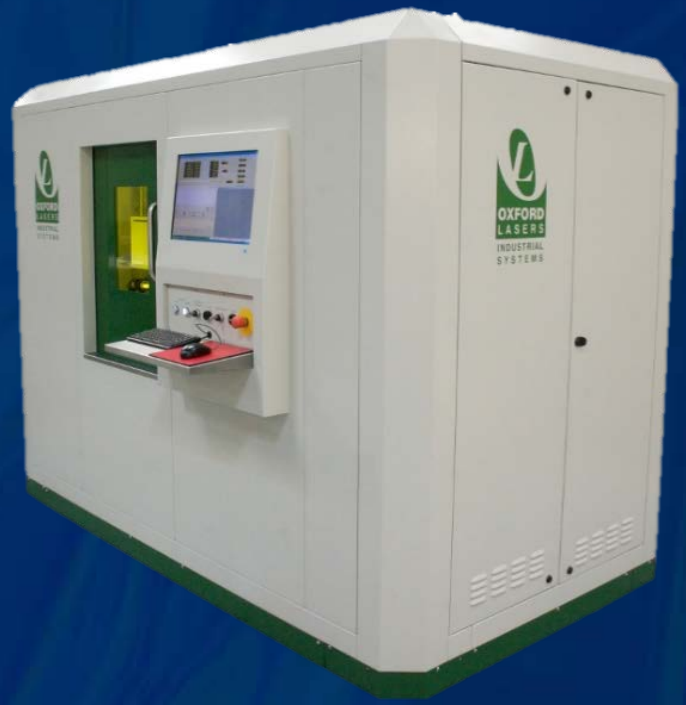
2) Temperature : stability of room temperature

3) Laser Source : pointing stability

4) Motion Control : stage accuracy

5) Calibration : calibration of the laser drilling tool

6) Calibration : calibration of the measurement tool



Types of Error

1) Random Errors

Example : Repeatability Errors :- Ensuring any motion system(s) return to the same point in space (i.e. bidirectional repeatability)

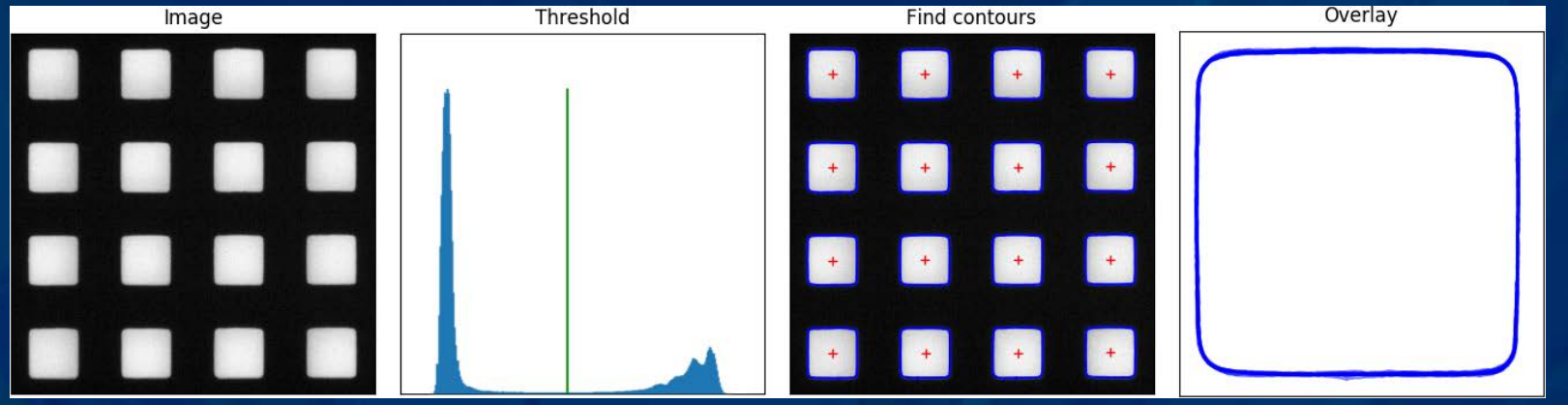
Note : This type of error cannot be compensated nor calibrated for, as its not predictable

2) Systematic Errors

a) Linear Errors : Example - Thermal expansion effects

b) Non-linear Errors : Errors that do not follow a straight line as you traverse the guide plate

Measuring Key Metrics



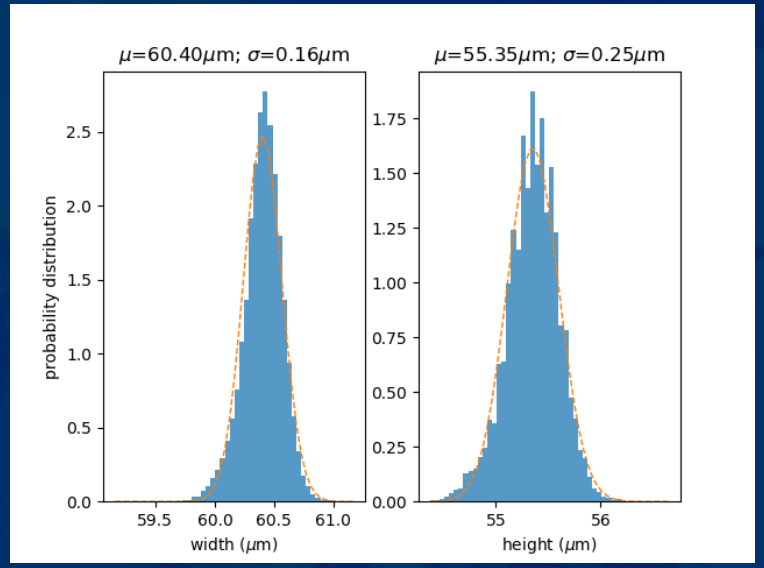
Capturing Holes | Thresholding | Locating Centroids | Contour Plots

Measuring key metrics for every hole – informs tool maintenance

Metrics to measure, size, position, corner radii, taper

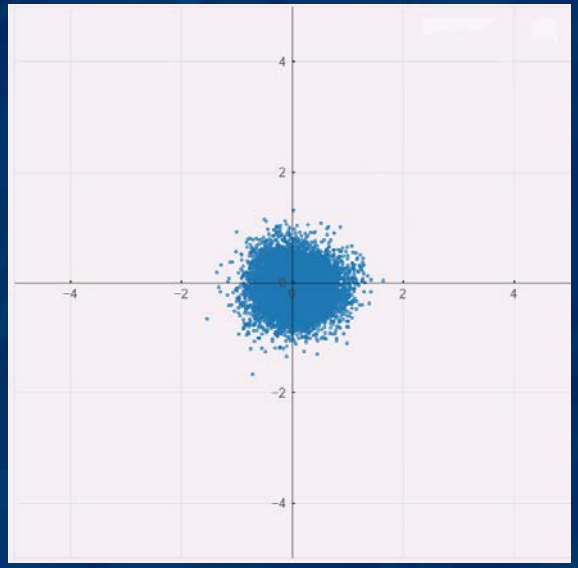
(See presentation given at SW Test 2017 for more detail on the above)

Measuring Key Metrics



Hole Size

(< 0.3 microns)



Position Error

(< 3 microns)

Solution

Through proprietary software which has been developed over many years – we have been able to improve positional accuracy

Continuously monitor positional data across multiple guide plate designs, 24/7, across all manufacturing tools

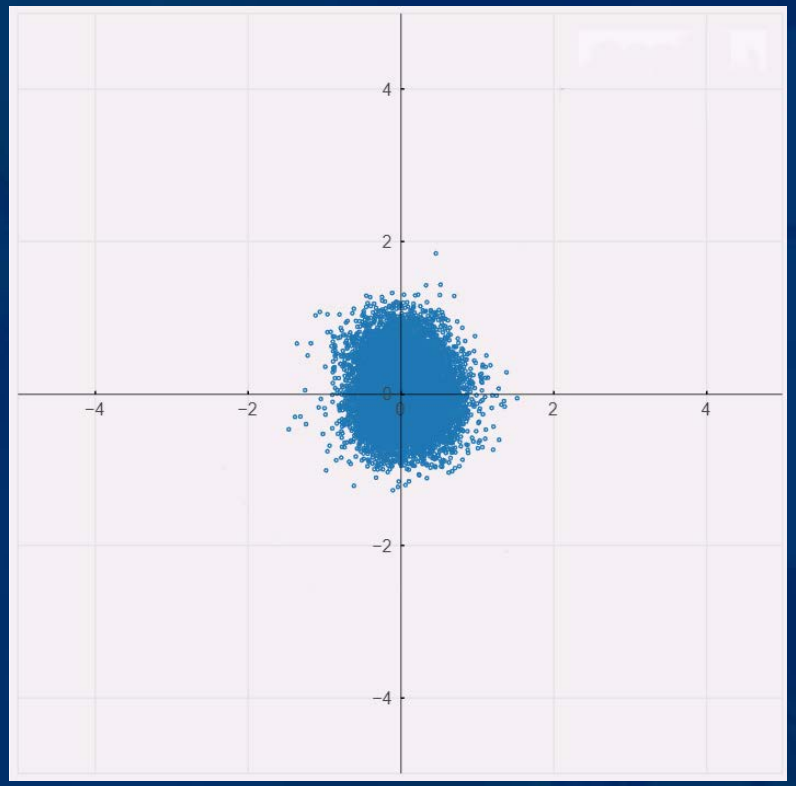
Analyse position errors for a) random and b) systematic error forms

Update hardware to correct for position errors

Feed the resultant data back into the tools to allow correction of hole position

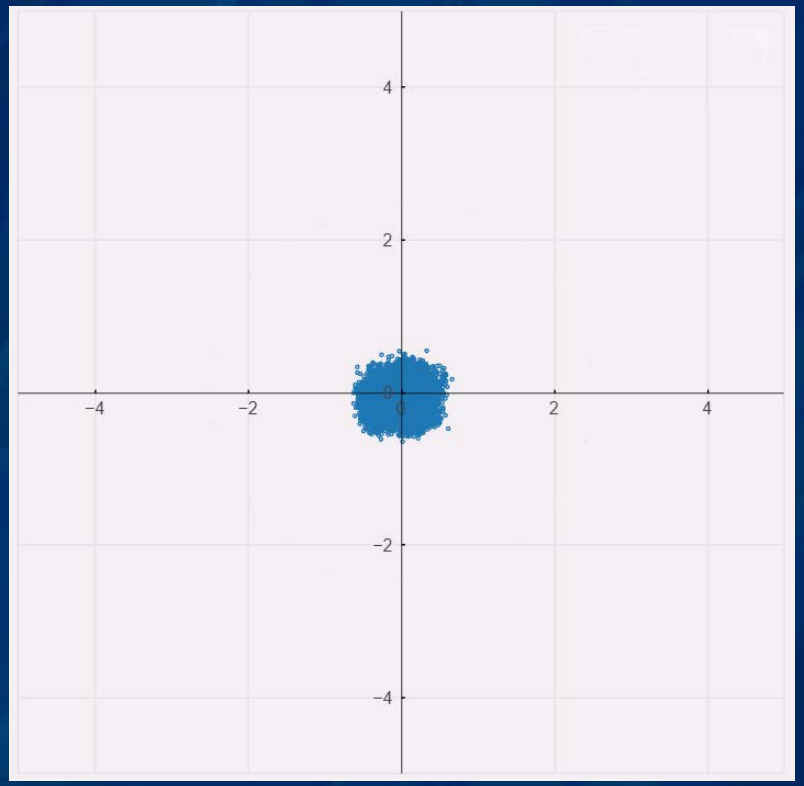
Results

Before



Less than 3 microns error

After



Less than 1 micron error

Summary

1) It has been shown that it is possible to improve micro hole positional errors to below one micron

2) This will enable the probe card designer to better control the probe needles, this being particularly important as probe pad or bump size reduces

Follow on Work

1) Monitor the improvements longer term to identify any other sources of error

2) Implement these new techniques into production guide plates

Thankyou

My thanks for this work go to :

From Oxford Lasers :

Simon Tuohy
Etienne Pelletier
Dimitris Karnakis
Mike Gaukroger

Thank you for your Attention