SWTEST ASIA
PROBE TODAY, FOR TOMORROW

Innovations in Testing for Truly Known Good High Bandwidth Memory Stacks

FormFactor™

ADVANTEST®

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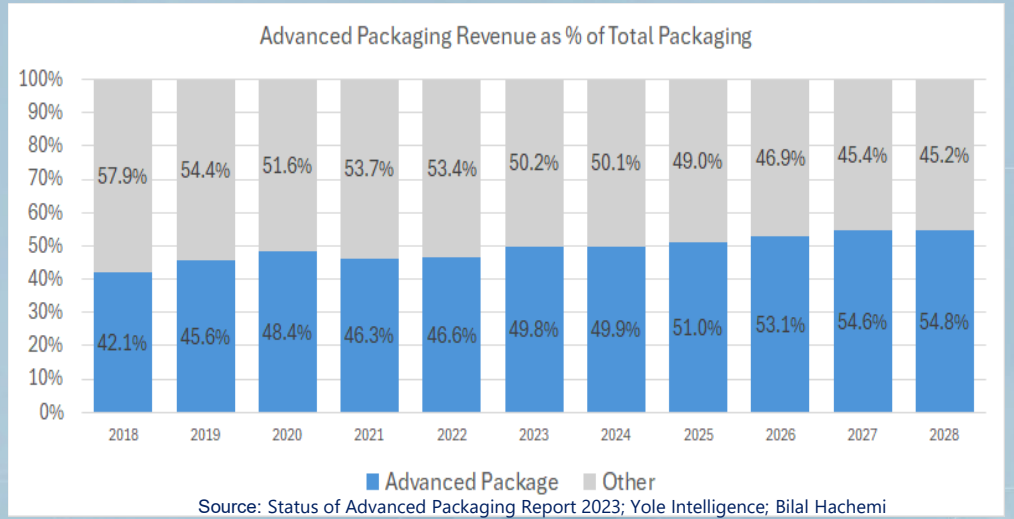
Agenda

- **Advanced Packaging Market Trend and Complexity Trend**
- **High Bandwidth Memory and SoC Die Yield Impact Analysis**
- **HBM Test Insertion and Known Good Die test method Discussion**
- **Die Carrier + Advantest Handler Test solution**
  - DC thermal performance
  - Electrical performance (SI/PI) simulation result
  - Scrub mark and contact repeatability study
  - Die level KGD test scalability roadmap
- **Summary, Acknowledgement**

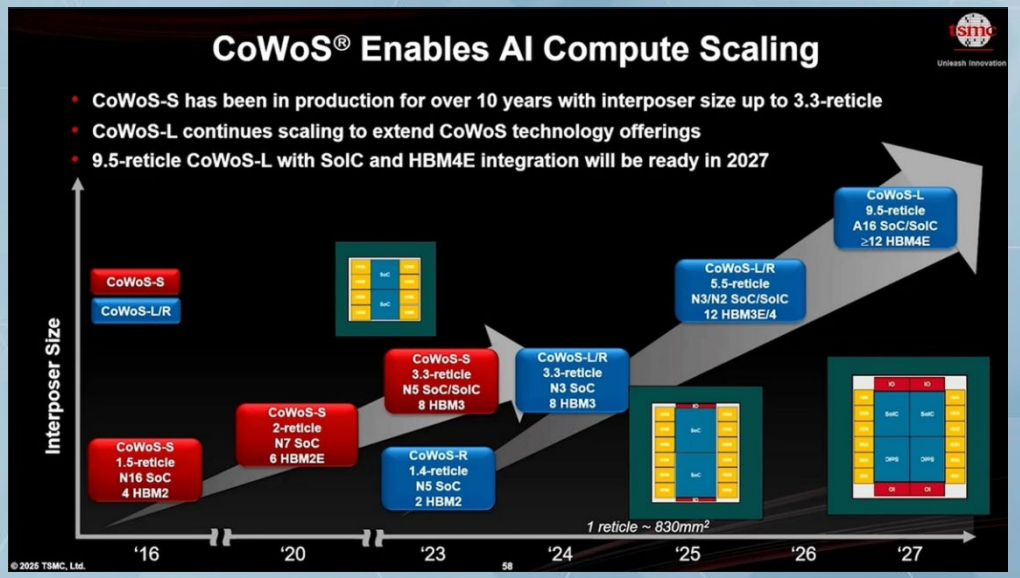
Advanced Packaging Market Trend

Forecasted 2025 >50% IC fab by Advanced Packaging

- **Advanced Packaging Revenue Growth of CARRG 12.7% as a Percent of Total Packaging Revenue ('18 – '28)**
  - More chips in the package → higher values being added
  - Advanced Packaging offers more features & computing power than individual IC packages – driving market growth
- **Advanced Packaging Complexity Trend:**
  - 1 SoC + 4 HBM → 4 SoC + >12 HBM
  - HBM Core stack: 4 → 16
  - Package size 1.5 → 9.5 reticle: increasing number of transistors and they all need to be tested



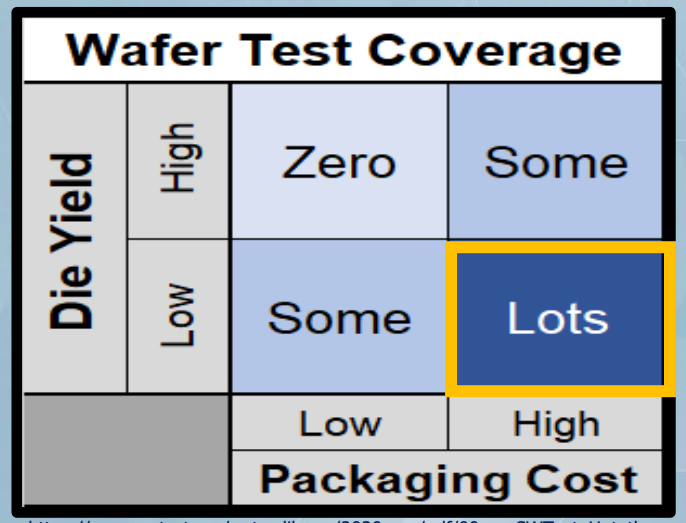
Source: Status of Advanced Packaging Report 2023; Yole Intelligence; Bilal Hachemi



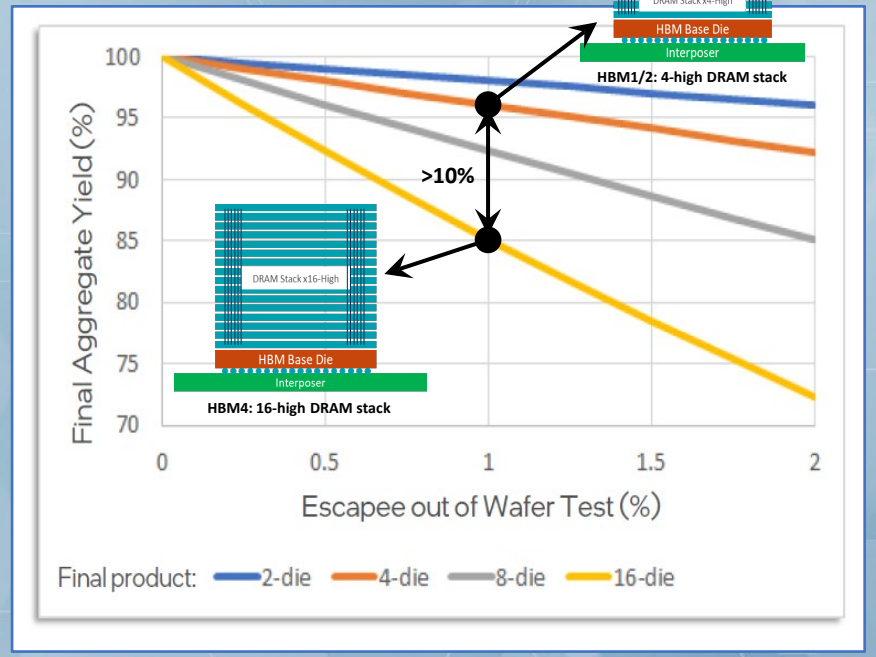
Source: https://www.techpowerup.com/336064/tsmc-outlines-roadmap-for-wafer-scale-packaging-and-bigger-ai-packages

Advanced Packaging Demanding More KGD Test

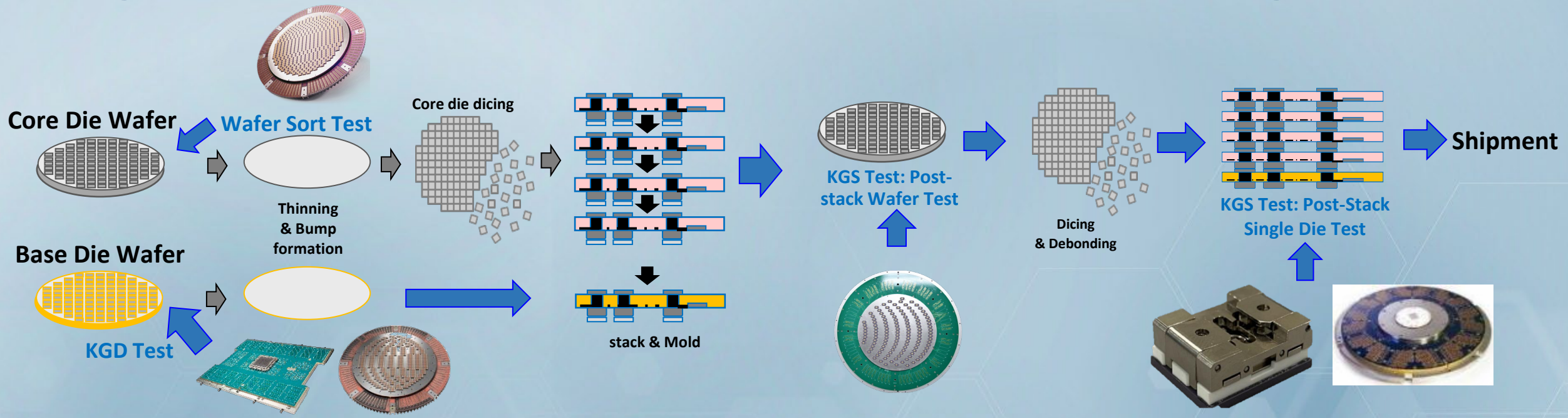
- **Multi-chiplet products require near-Known Good Die constituent chiplets**
  - This requirement becomes more important as the number of chiplets in the chip increases
- **Matching of constituent performance bins is also important**
  - Performance of the multi-chiplet System-in-Package is determined by the lowest-performance chiplet in the stack
  - Limits selling price in performance applications
- **Cost vs. test coverage optimization comes down to math**
  - Earlier defect detection helps save packaging costs
  - Higher complexity → high packaging costs
  - Higher complexity → lower yields



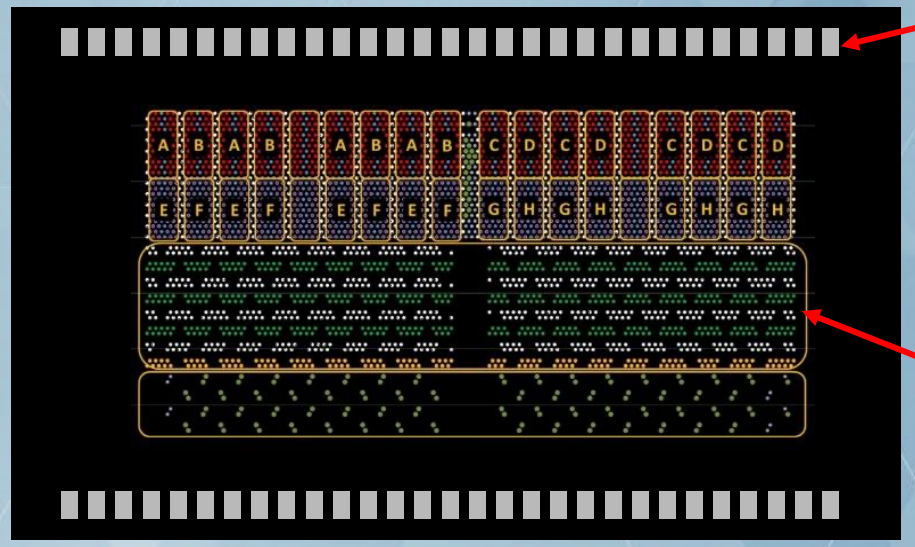
https://www.swtest.org/swtw_library/2020proc/pdf/00pm_SWTest_Untethered_Keynote_Slessor_FormFactor

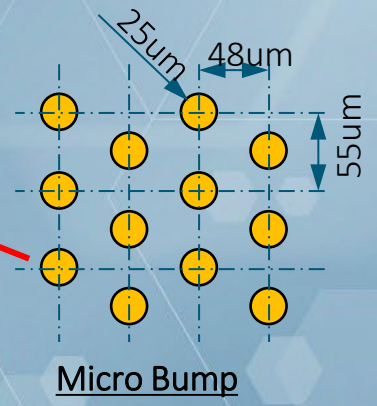


High Bandwidth Memory Test Flow & Challenges



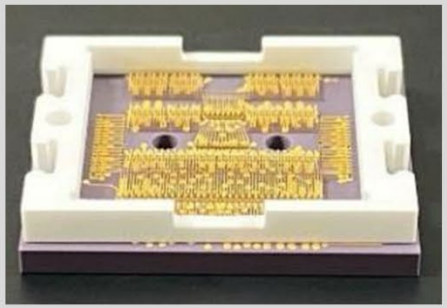
	Micro-bump probing test	DFT pad probing test
Pros	• Best test coverage • Real performance data	• No damage to ubumps • Highest test efficiency
Cons	• Connection reliability concern on ubump • Low test efficiency • High test cost	• DFT required design in HBM • Test coverage gap



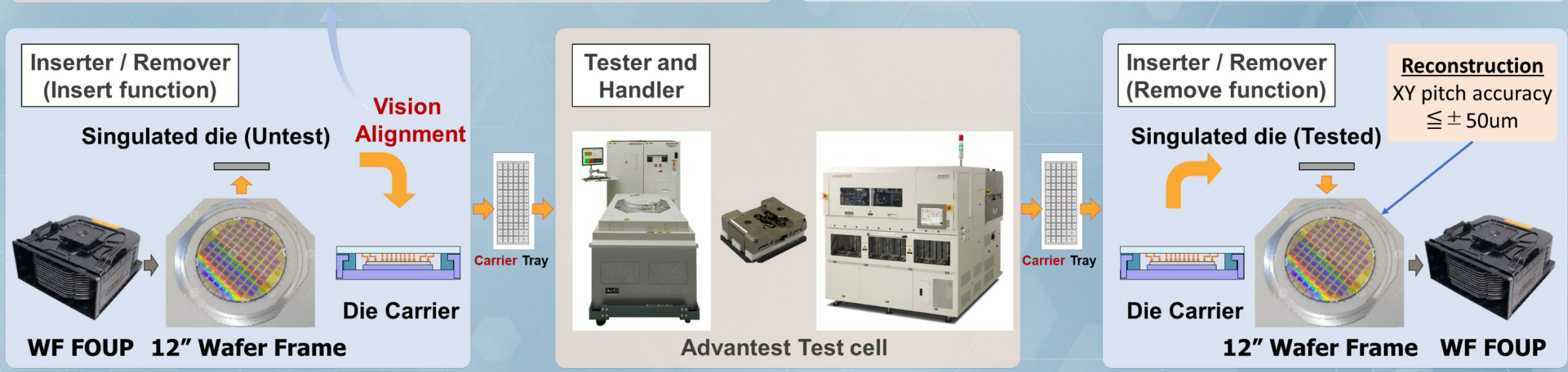


HBM test cell solution by “Die Carrier”

- Die Carrier (Interposer , Lid , Probe)



- Inserter/Remover



Key Challenging on Current Test Process

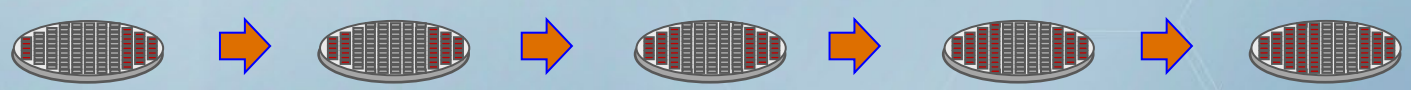
KGS Test: Post-stack Wafer Test

Test flow #1 → Test flow #2 → Test flow #3 → Test flow #4 → Test flow #5

Post-stack Wafer Test

Test efficiency:

80% → 75% → 70% → 65% → 60%



- ✓ Failure Die is carried together to next test process
- ✓ Test efficiency becomes getting worse along with each test process
- ✓ Need multiple contact for retest/each test processes (mechanical stress)

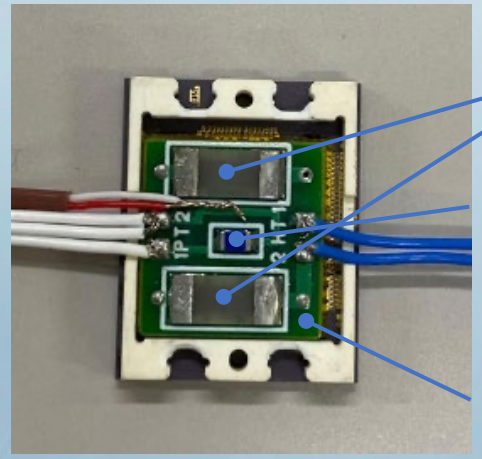
Post-stack Single Die Test

Test efficiency:

100% → 100% → 100% → 100% → 100%

- ✓ **Failure Die can be rejected** on each test processes
- ✓ Test efficiency can keep **100%** (larger through put)
- ✓ Only **1-insertion** (pack into die carrier) during entire test processes (less mechanical stress)

DC Thermal Structure Overview

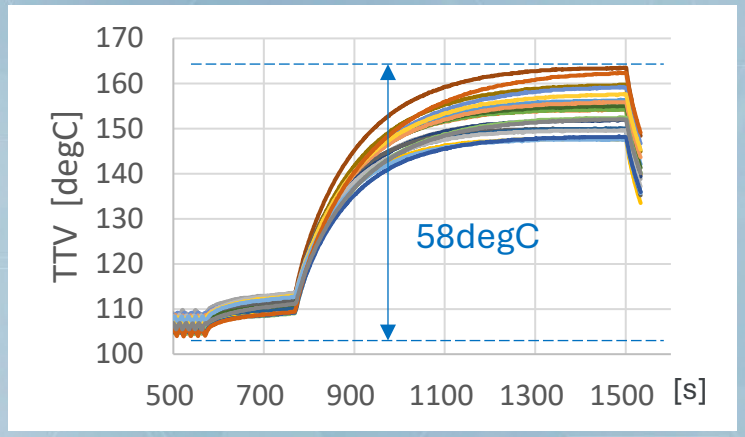


Current handler

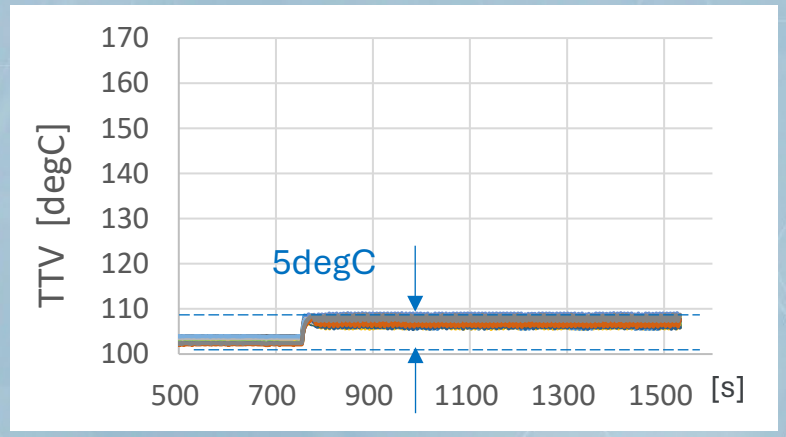
New Gen handler

Item	Thermal Performance		
Handler	Current	Next Gen	
Parallelism	64	128	256
Heat generation	2.2W	40W	20W
temperature	105℃	105℃	
Tj rise(all Die)	≦5℃	≦3℃	

➢ **TTV temperature rise comparison w/ 2.2w heat generation**



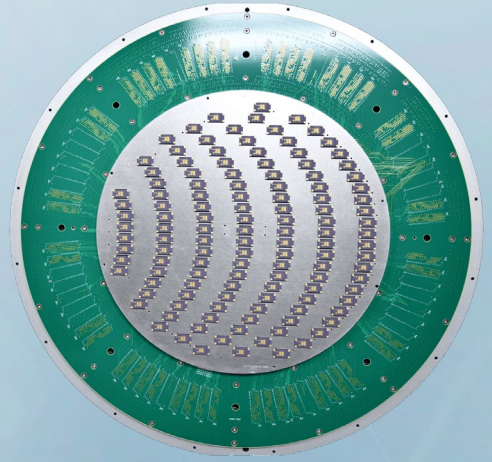
without T-pusher control

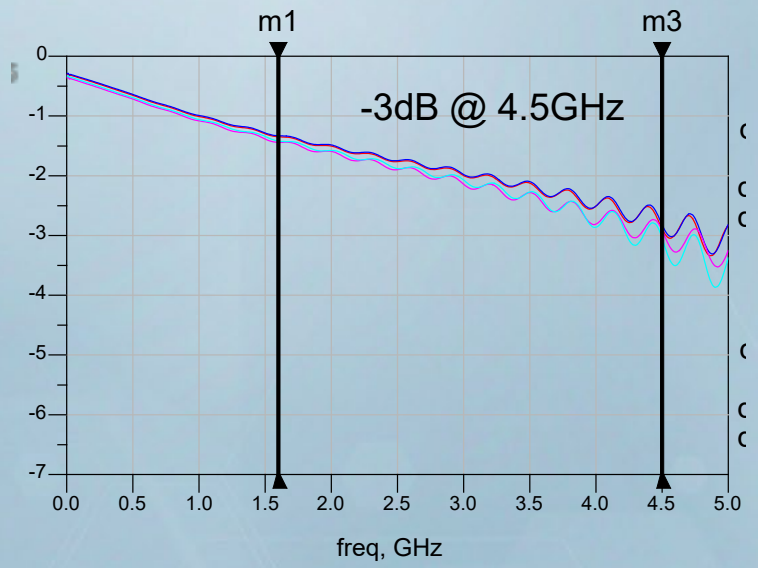


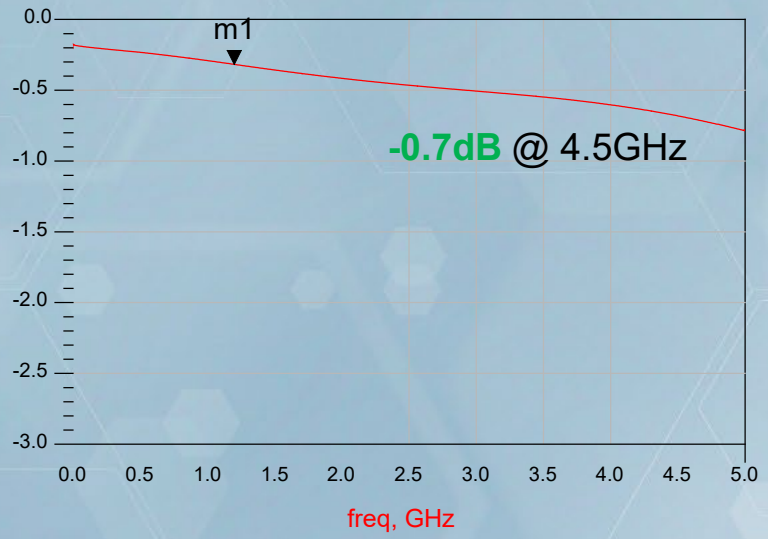
with T-pusher control

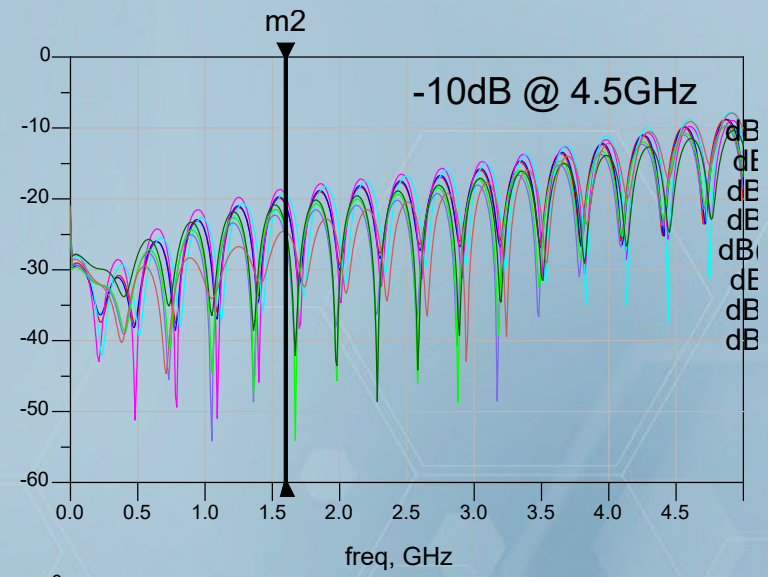
Die Carrier: >2x Better Electrical Performance

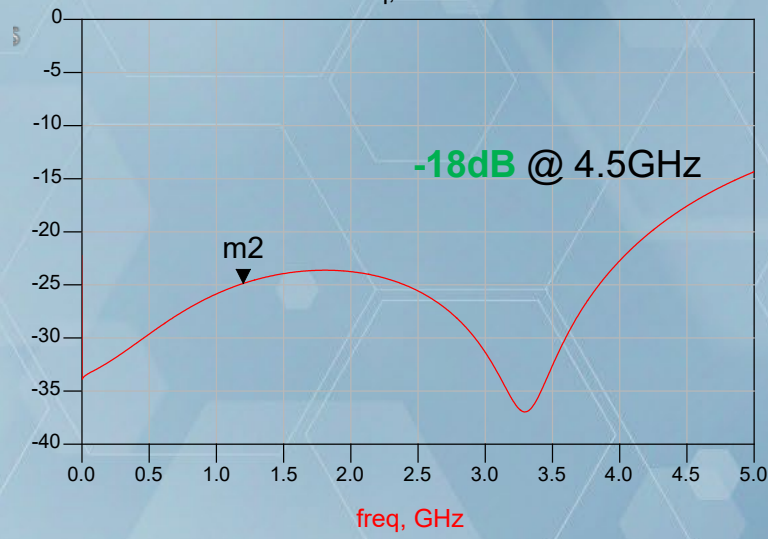
By Eliminate >200mm PCB Trace







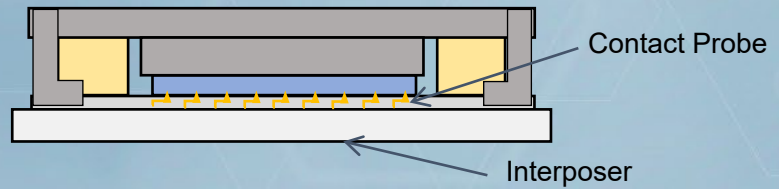


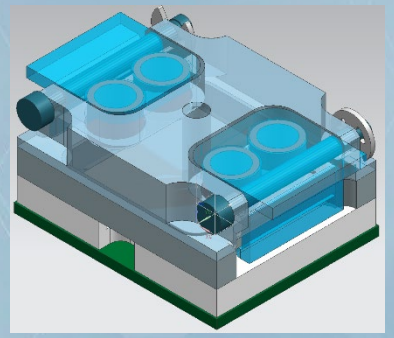


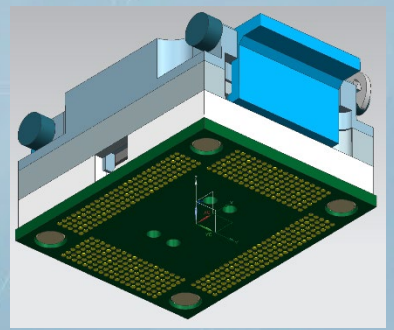
Carrier Structure and SI/PI Simulation Result

Carrier structure

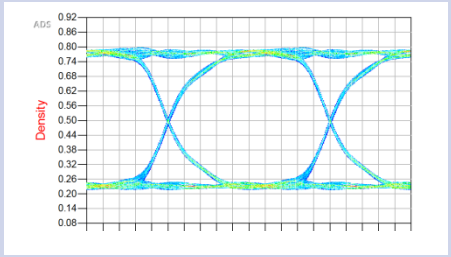
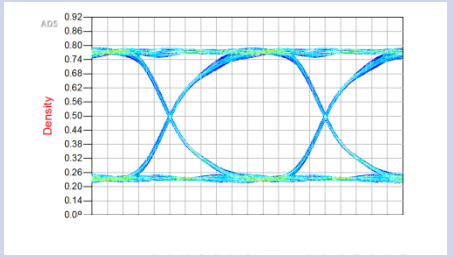
- **Structure**
  - Contact to HBM device : MEMS Probe
  - Contact to test socket : Interposer
- **Pros**
  - High electrical performance can be expected
  - Similar pad scrub behavior with wafer test



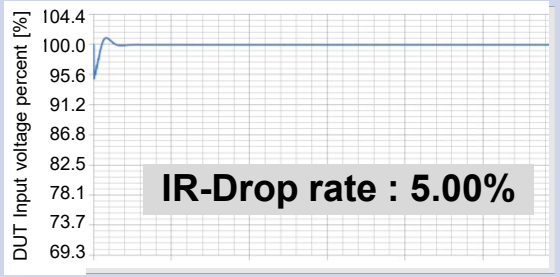
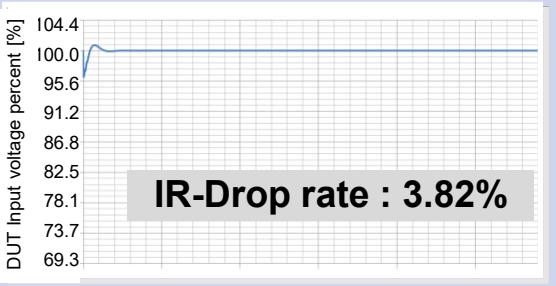




SI/PI Simulation result

2.0Gbps ODT_50	2.4Gbps ODT_50
Eye height opening rate : 92.8%	Eye height opening rate : 90.1%
	

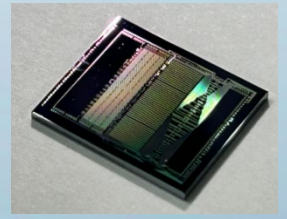
T5503HS2 DUT's Input signal (Write cycle)

C(k) setting : C(2)	C(k) setting : C(4)
	

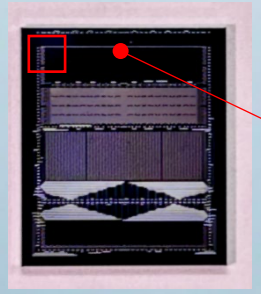
T5503HS2 Power supply simulation (IR-Drop) results in 64DUT

Die carrier Repeatability Evaluation Results

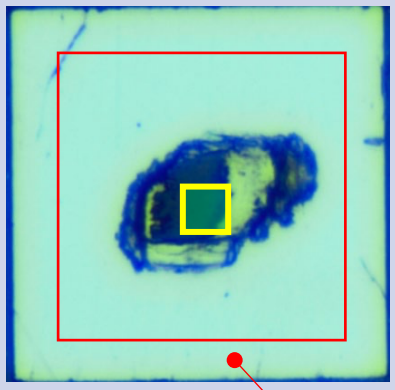
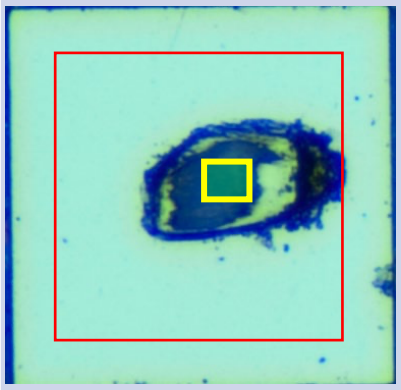
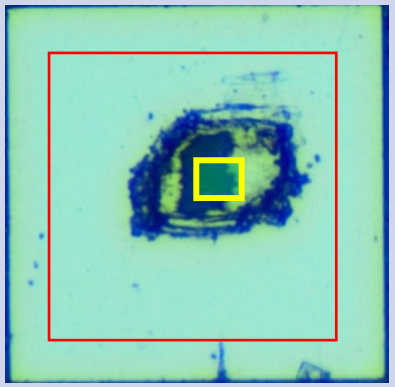
Dummy Die
11 x 13 x 0.8mm



Front view

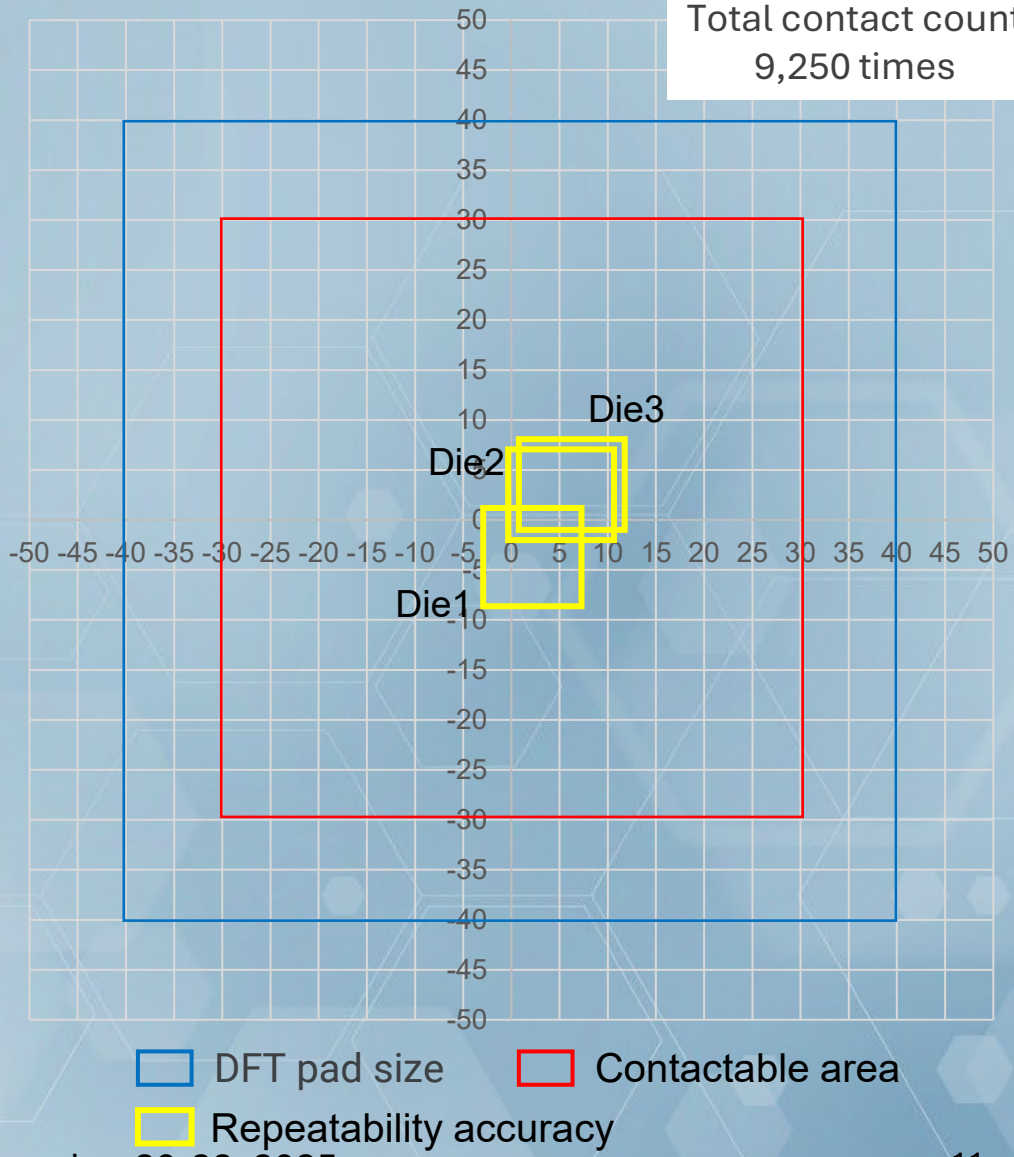


DFT pad 505pcs

Count	Sample 1	Sample 2	Sample 3
100			
500			
Final	1,100 	6,600 	1,550 

DFT pad
80umx80um

Total contact count
9,250 times



Die Level Test Solution Scalability

HVM@HT

1. Using Die Carrier solution for HVM @HT
2. Using **Inserter/Remover** for die insert
3. Correlation between RT and HT

HVM @RT

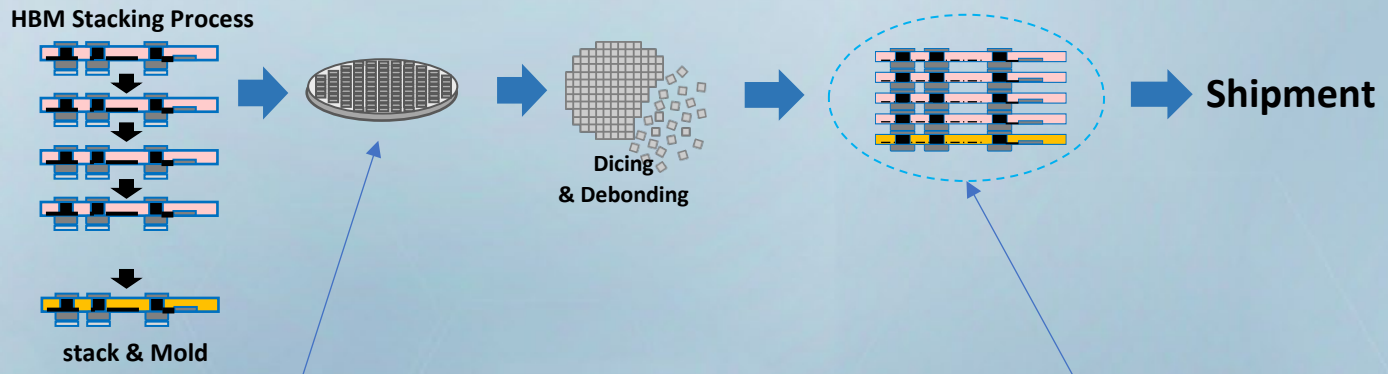
1. Using Die Carrier solution for HVM @RT
2. Using **Inserter/Remover** for die insert
2. Correlation between Manual and HVM

Manual Test

1. Using Engineering system for validation
2. Using **Manual JIG** for die insert
3. Correlation between Wafer Test and Die level test @RT

Inserter/Remover

HBM Singulated Stack Die Test Solution



Post-stack Wafer Test

Source: Accretech

Post-stack Single Die Test

Product Features:

- Compatible with conventional probe
- Offer same high-speed performance as HFTAP*
- Cold and Hot temperature capability
- Design with Advantest handler and tester build in vision alignment feature

*HFTAP : High Frequency Test At Probe

Product Benefits:

- Offer **truly** known good stack/die test solution
- Enable quality screening post HBM stack wafer dicing
- HBM KGD test capability up to **4GHz**
- High parallelism test (limited to handler and tester resource)
- Excellent thermal control up to **40W**
- Keep **100% test efficiency** with removing failure die
- **1-insertion** during entire test flow (less stress)
- Engineering/HVM setup ready

Summary

Technical Advantage – Die-Level Testing

- Singulated die testing allows full-speed, multi-temperature screening before stacking
- 1-insertion via die carrier achieves complete test coverage (DC, functional, etc.) in a single insertion
- Supports high parallelism, improving overall throughput without compromising test quality
- Engineering setup to HVM scalability

Scalability and Future Applications

- The short transmission path of the die carrier architecture enables reliable multi-GHz test performance
- Well suited for wafer-level high-speed memory testing and future chiplet architectures

Acknowledgement

- **FormFactor**
  - Abdelrahman Awad
  - Jim Tseng
  - Kevin Tran

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  - Toshiyuki Kiyokawa
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  - Atsushi Nakadate

Questions?

Thank you