POSTER #SWTA24-46

3D-IC FABRICATION WITH TSV AT THE DIE LEVEL FROM 2D-IC

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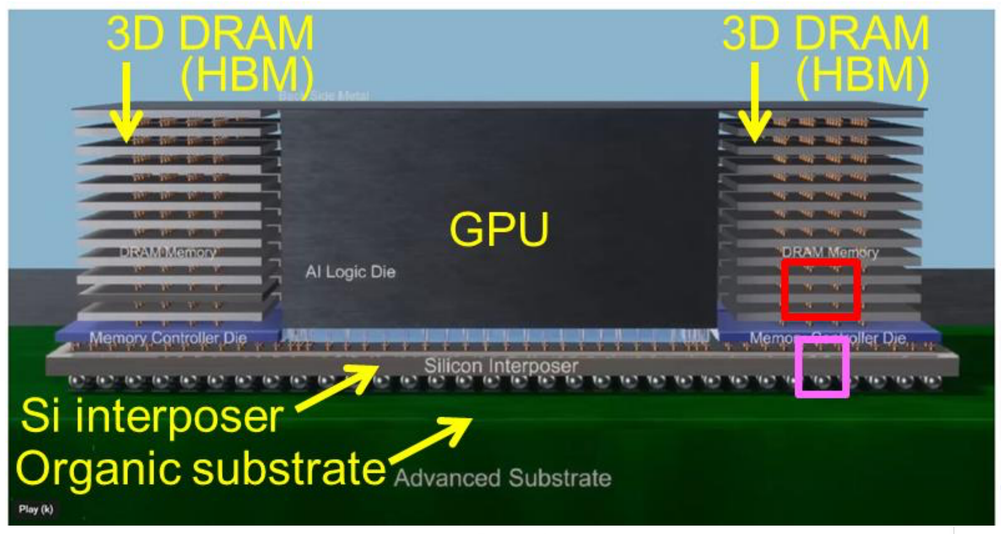
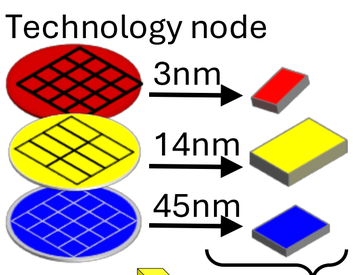
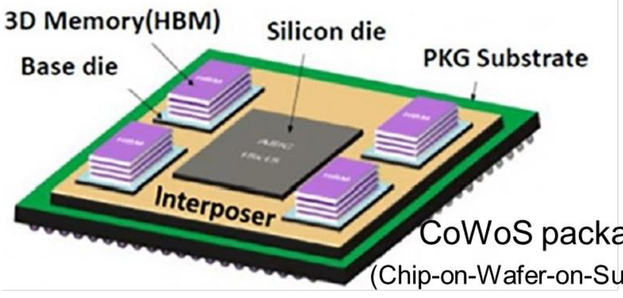
INTRODUCTION

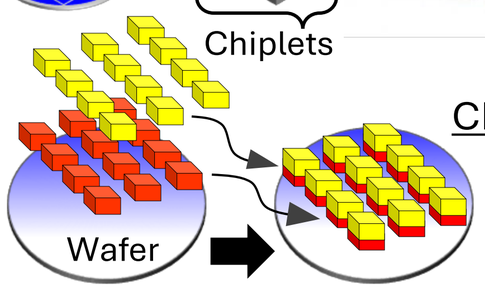
https://www.youtube.com/watch?v=-egYoxajTz0





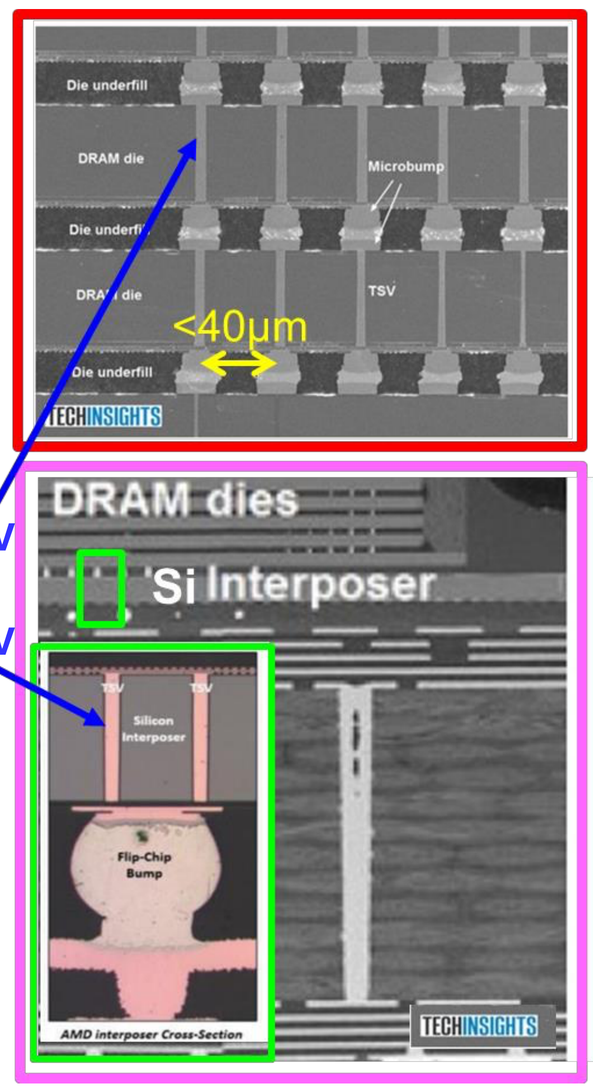


CoWoS package
(Chip-on-Wafer-on-Substrate)



Chip-to-Wafer 3D stacking
(Chiplet integration)

What is chiplet?

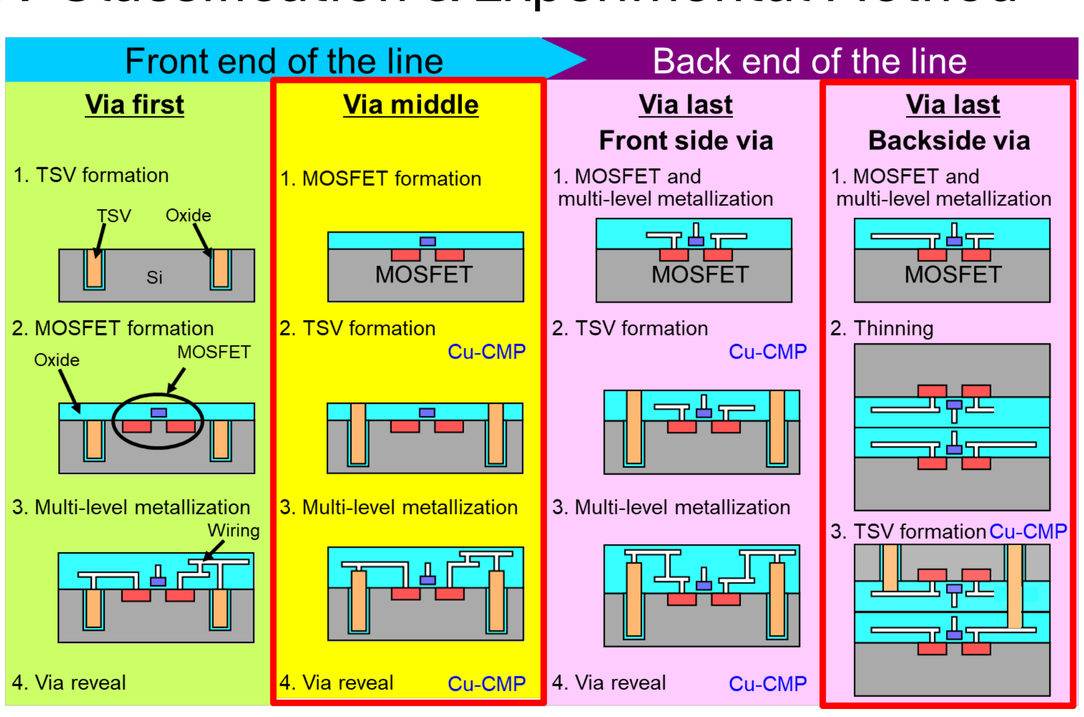


3D Integration/TSV is pioneered since 1994 in Tohoku Univ. by Prof. Koyanagi et al., "Vertical Buried Interconnection" & "Wafer Bonding"

HBM is originated from IEDM 2000 K.W. Lee *et al.*, "Three-Dimensional Shared Memory Fabricated Using Wafer Stacking Technology"

World 1st demonstration of Chip-to-Wafer 3D integration is given by IEDM 2005 T. Fukushima *et al.*, "New Three-Dimensional Integration Technology Using Self-Assembly Technique"

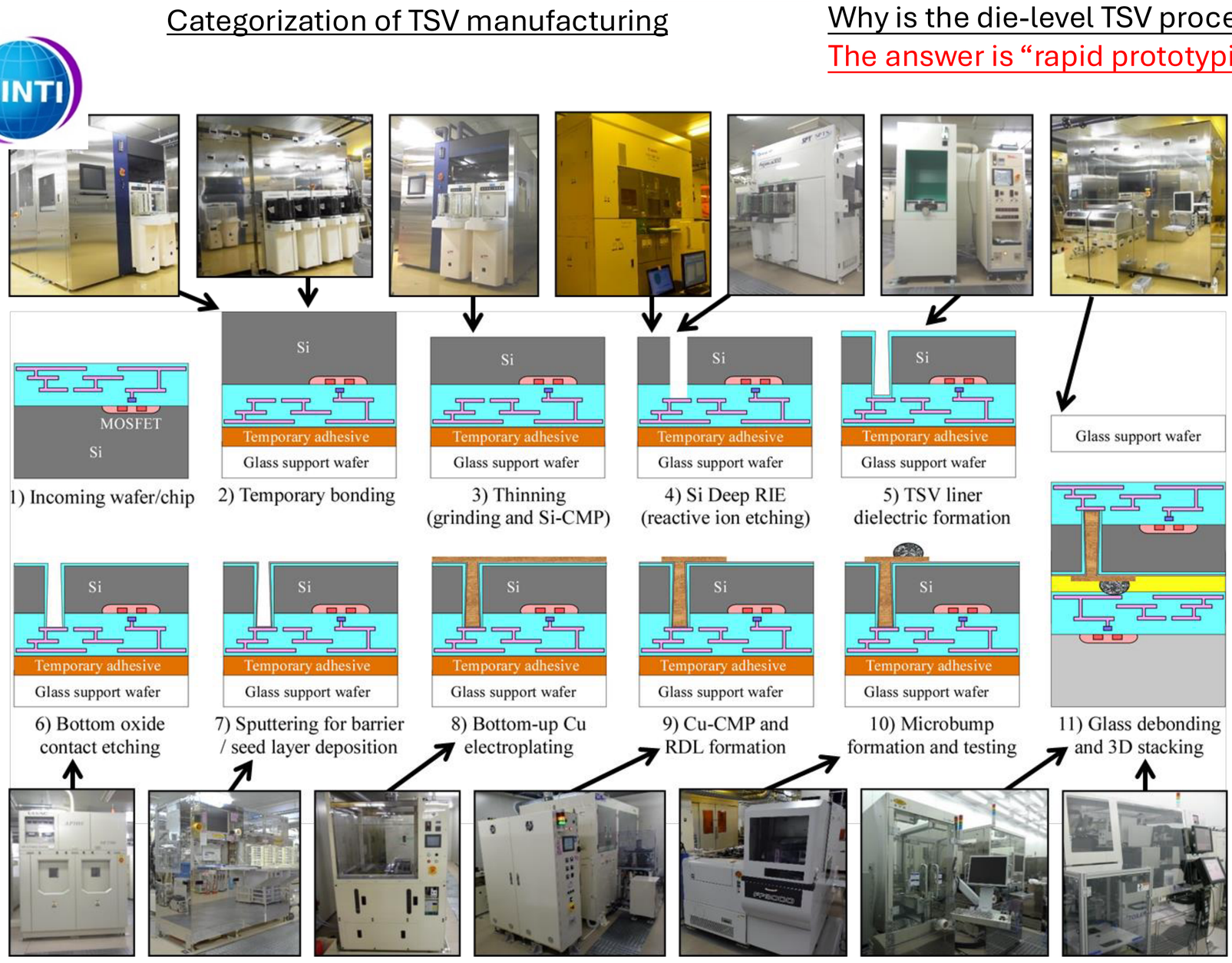
TSV Classification & Experimental Method

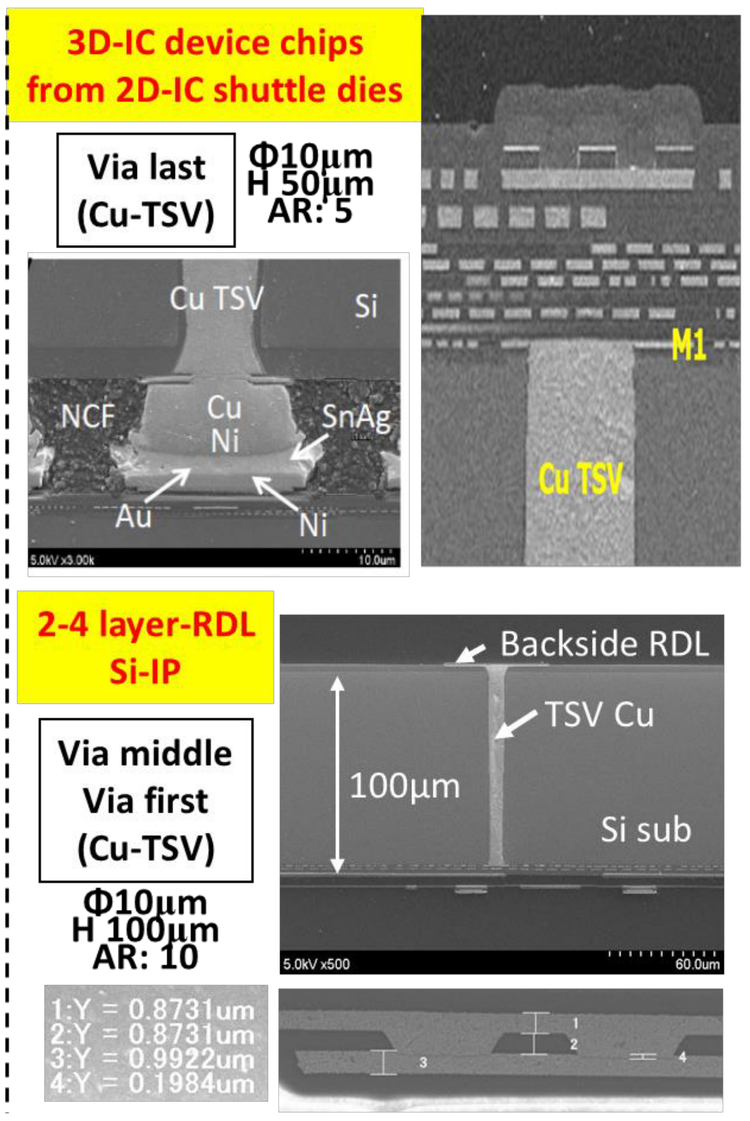


Categorization of TSV manufacturing

Via-last die-level TSV Process

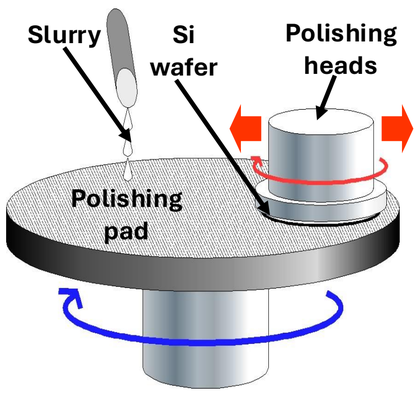
Why is the die-level TSV process required?
The answer is "rapid prototyping".

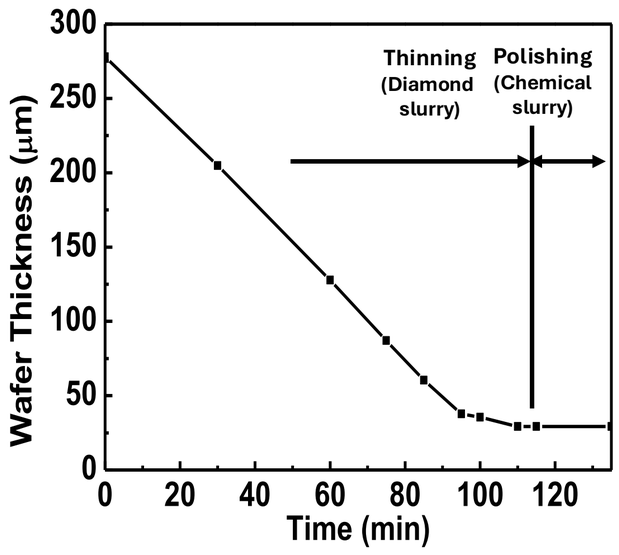




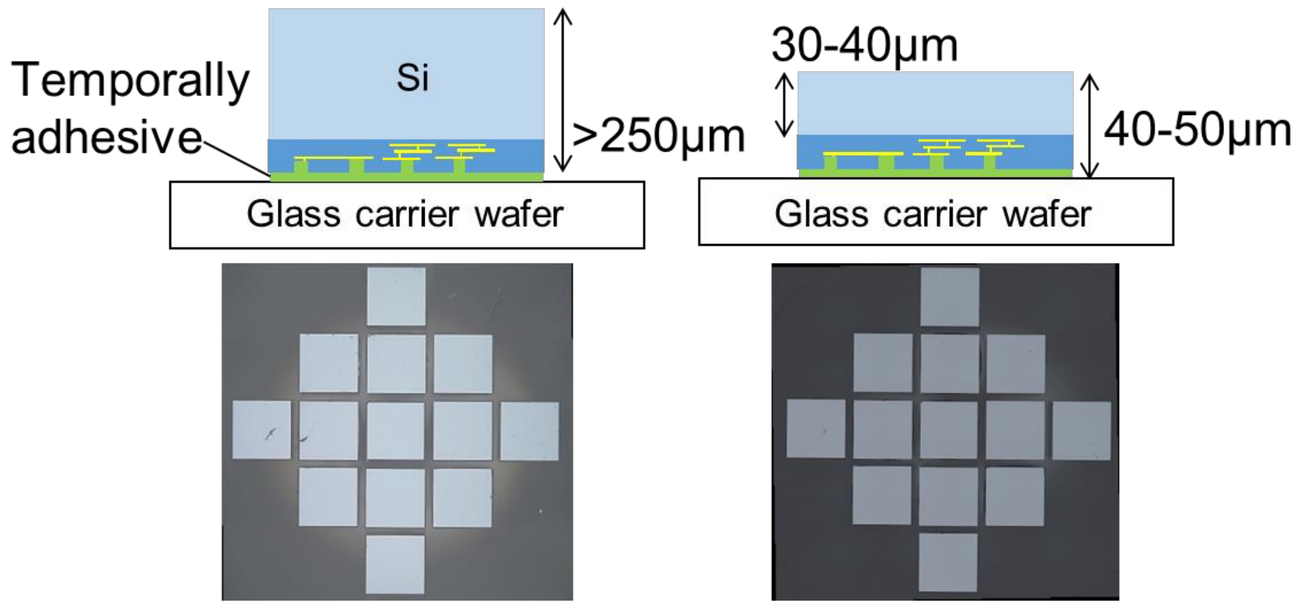
Via-last Wafer-level TSV Process @ GINTI (Global INTegration Initiative) "Tohoku's ϕ300-mm-Wafer 3D-IC Prototyping Cleanroom"

RESULTS & DISCUSSION 1: Wafer and Chip Thinning



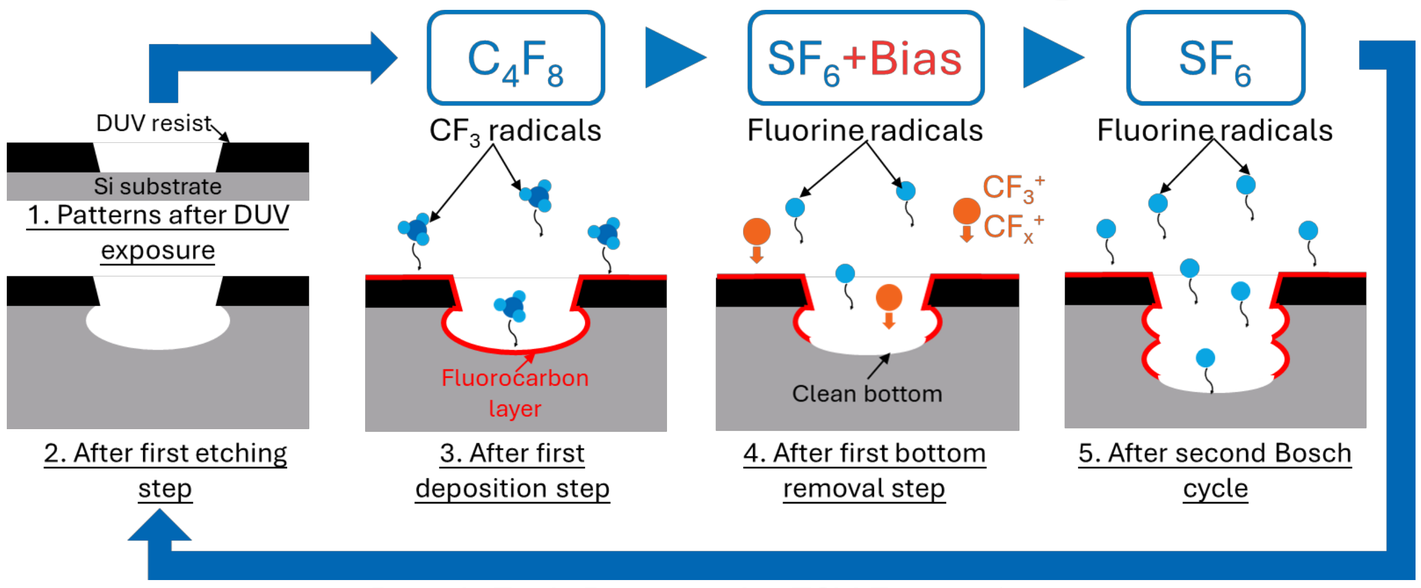


Mechanical coarse/fine grinding + CMP
(Chemical Mechanical Polishing)



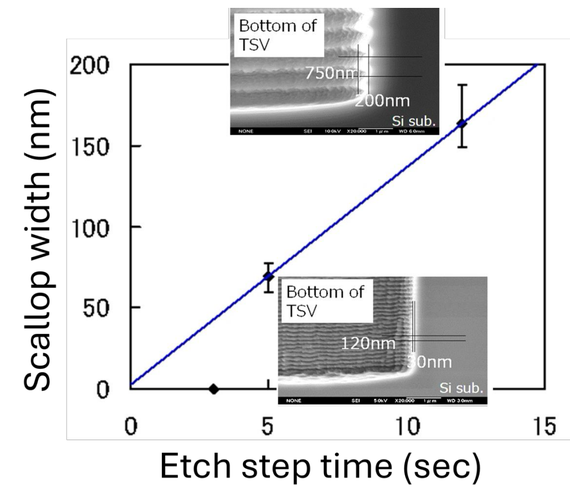
Multichip thinning

RESULTS & DISCUSSION 2: Bosch Etching

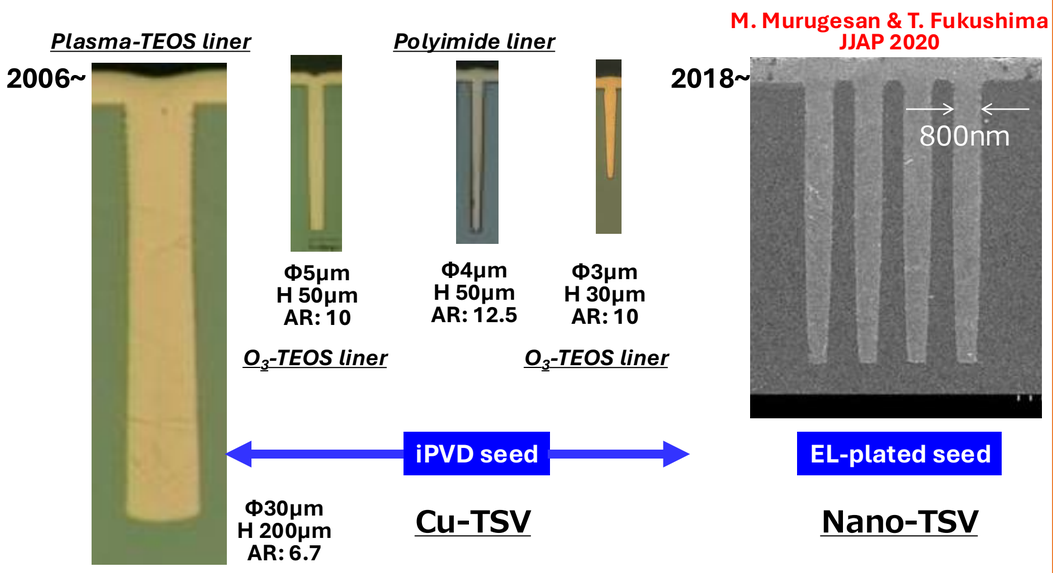


Bosch Etch Process for TSV Formation

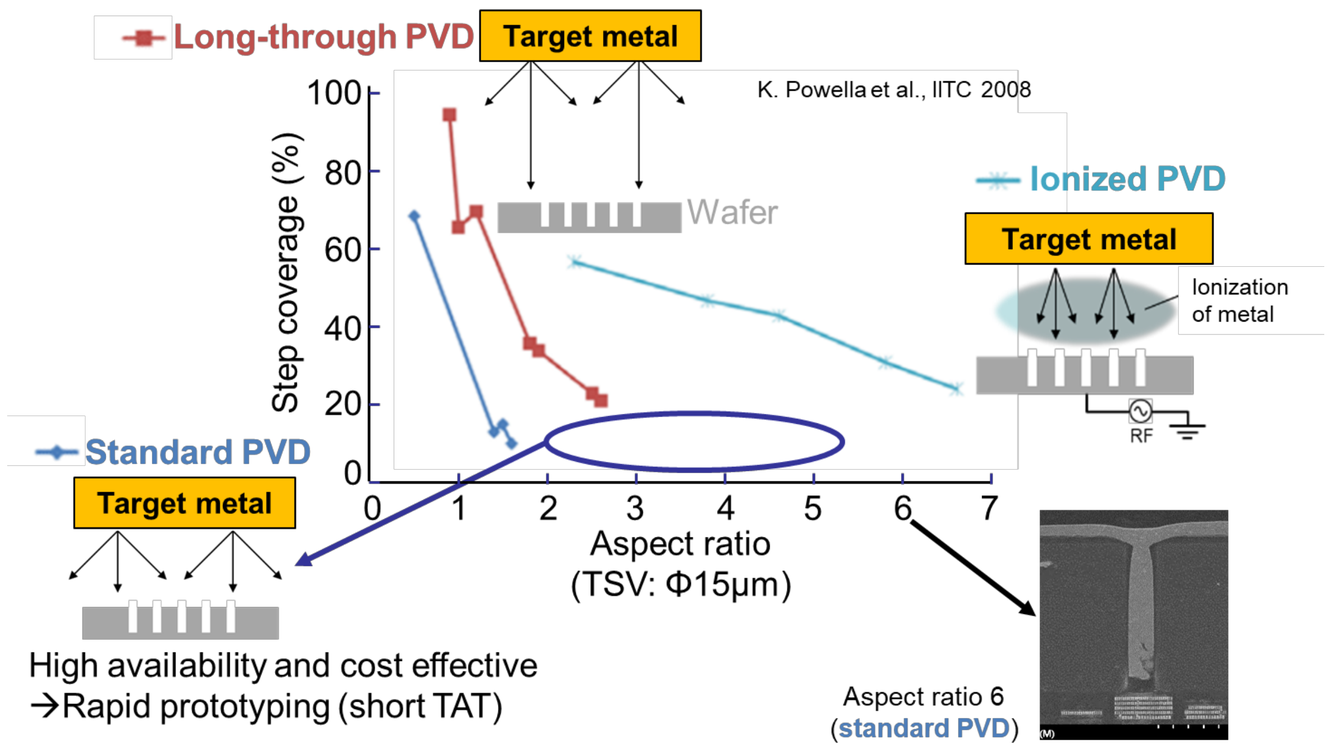
Cycle step	Deposition	Etching	Etching
Gas flow rate (sccm)	SF_6:1 C_4F_8:50	SF_6:50 C_4F_8:1	SF_6:50 C_4F_8:1
Active time (s)	8	8	8
Pressure (mTorr)	20	20	20
Substrate	20	20	20
Temperature (℃)	80	80	80
ICP power (W)	450/13.56MHz	450/13.57MHz	450/13.58MHz
Platen RF power (W)	0	26/380kHz	26/380kHz
Bias (V)	0	110-126	110-127



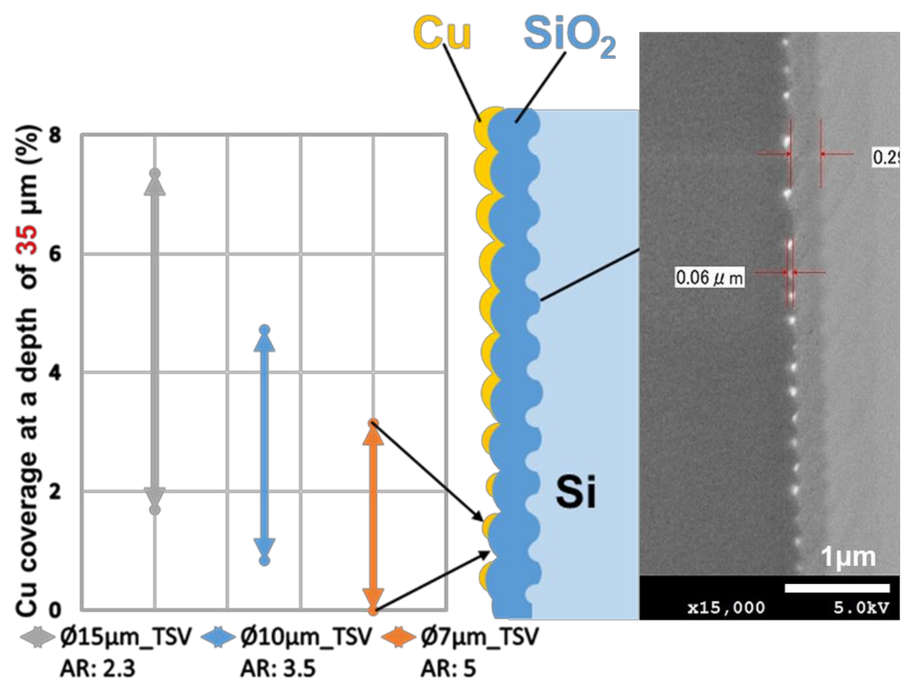
Relationship between etch step time and scallop width



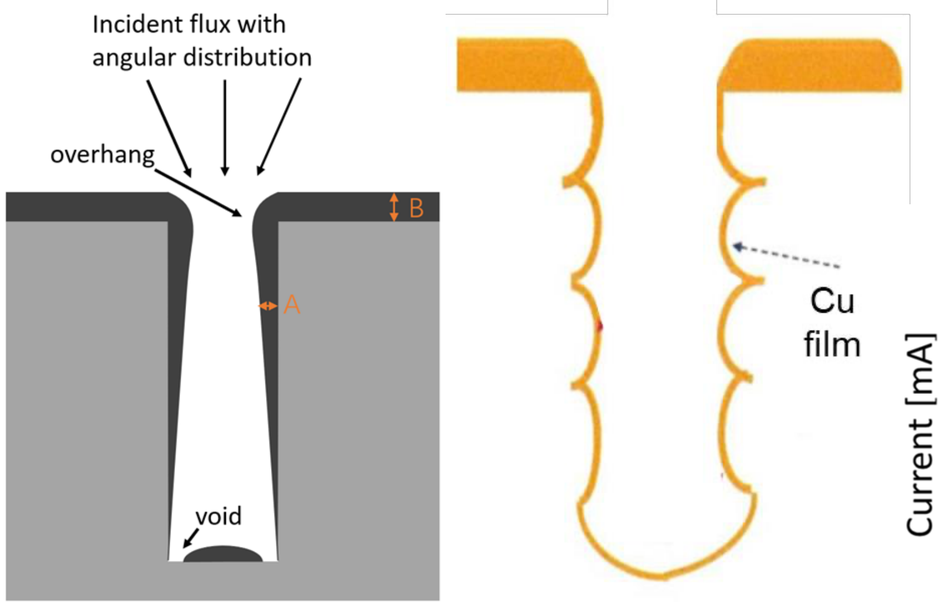
RESULTS & DISCUSSION 3: High-Aspect-Ratio Sputtering & Cu Filling Bottom-up Electroplating



Sputtering Technology for High Aspect Ratio Via Holes

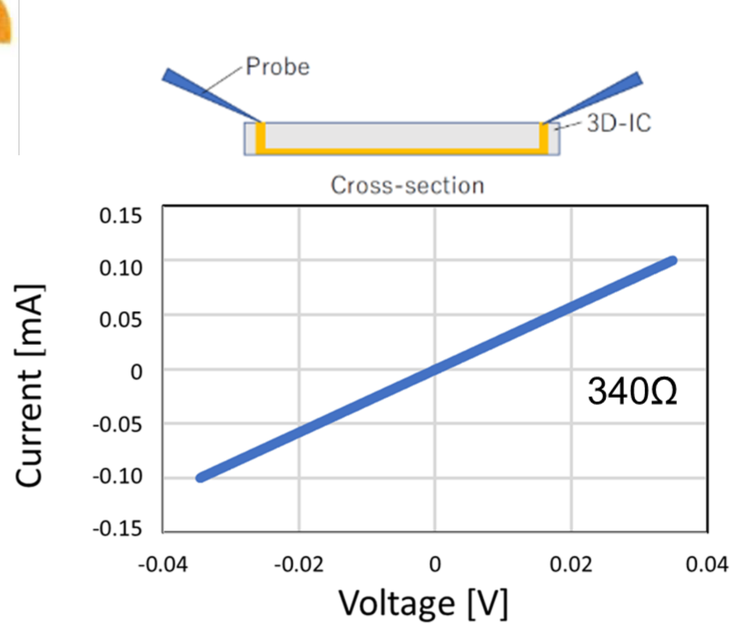


Seed layer thickness in different diameter at depth of 35μm by standard PVD tool

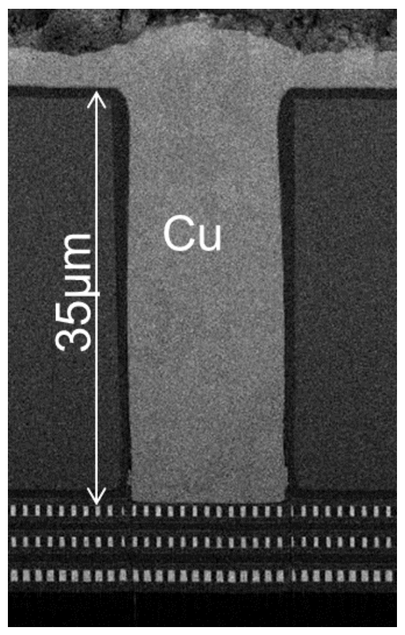


Difficulty in conformable Cu film deposition by sputtering for high-aspect ratio TSV

Scalloped feature from via-hole etching

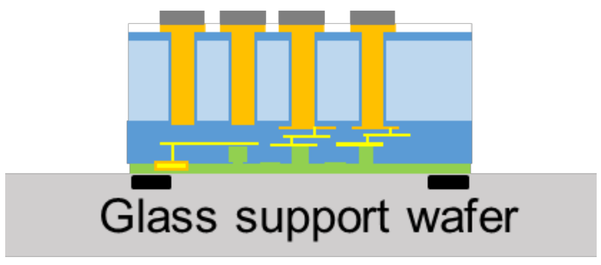


Electrical characteristic of a pair of TSVs in a 3D-IC

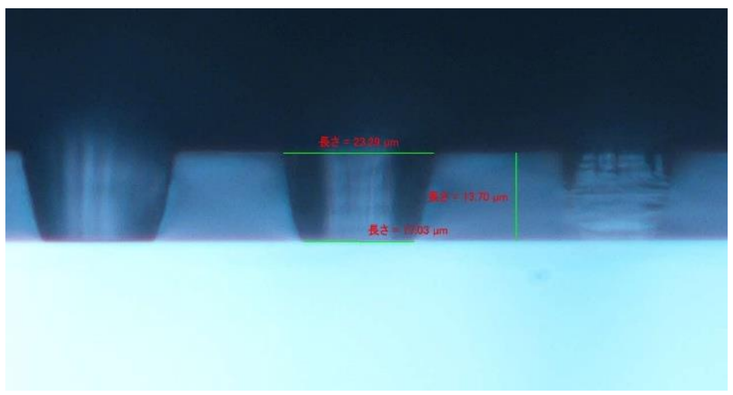


A cross-section of a Cu-TSV formed in a shuttle service 2D-IC at the die level with standard PVD (AR: 3.5)

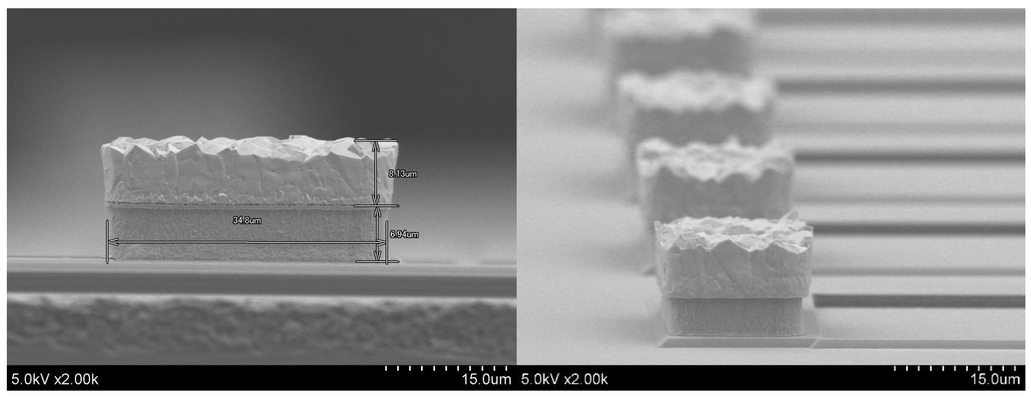
RESULTS & DISCUSSION 4: Solder Microbump Formation & Bonding



Spray lithography for micro-bump formation

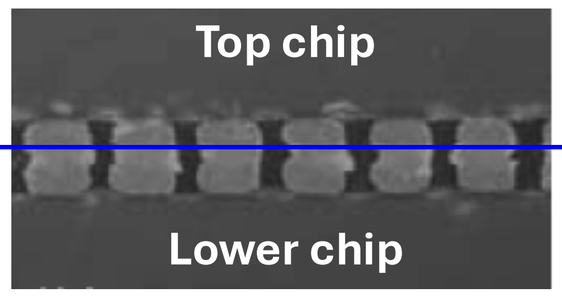


Cross-section of Spray-coated photoresist



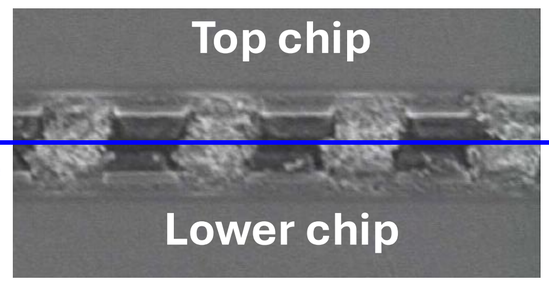
Solder/Cu μbumps on a shuttle chip

(a) Fine-pitch microbump



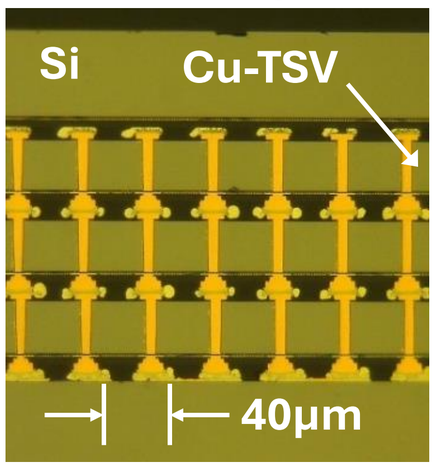
10μm-pitch Cu/Sn μbump bonding for 3D-IC (IEICE2011)

(b) Ultra fine-pitch microbumps



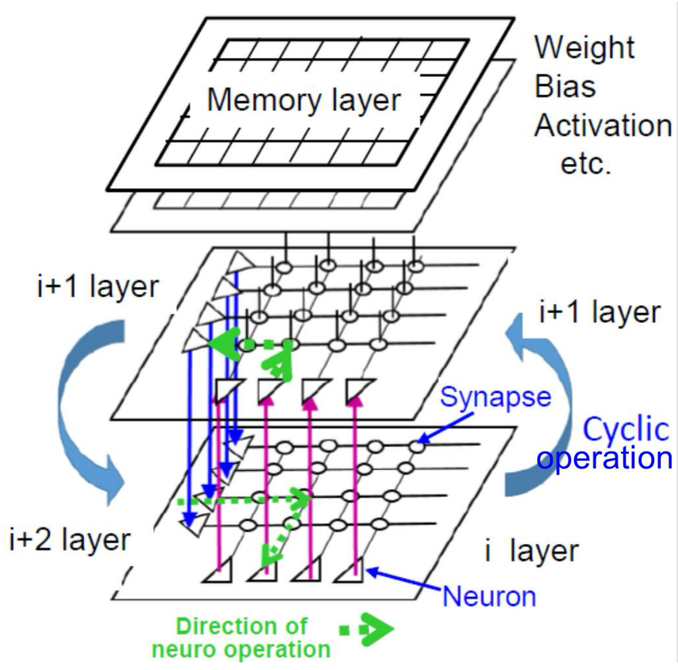
5μm-pitch In/Au μbump bonding for 3D-IC (IEDM2011)

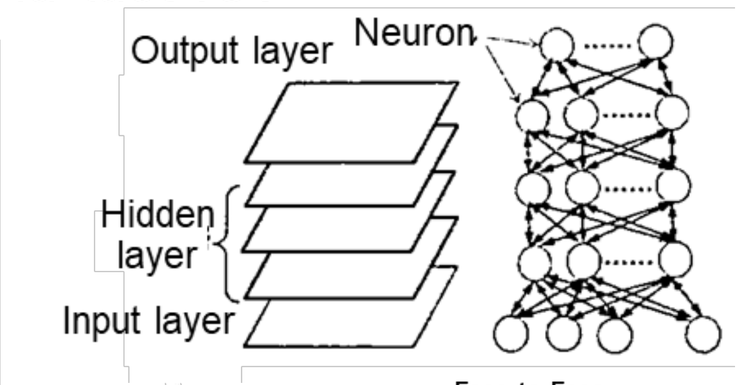
(c) Multi-layer stacking with thin dies

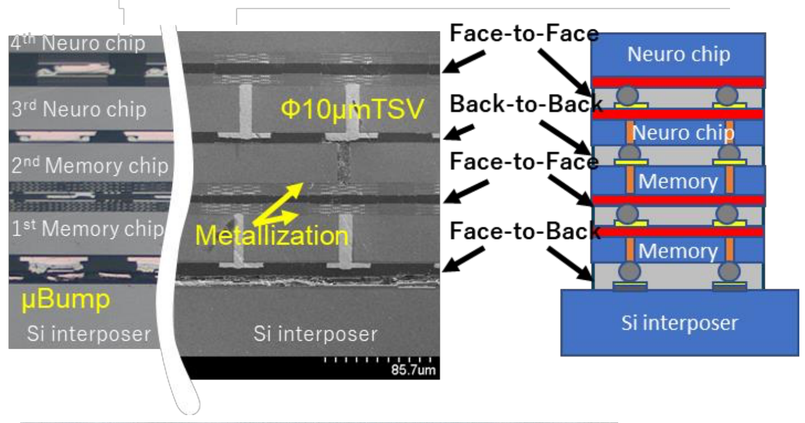


40μm-pitch Cu/Ni/SnAg μbump bonding for 4-layer DRAM with Cu-TSV (3DIC2014)

3D-IC Prototyping based on Via-last TSV

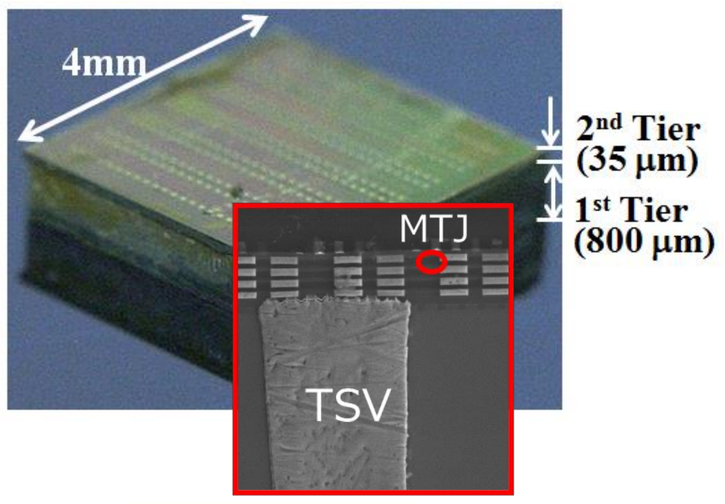




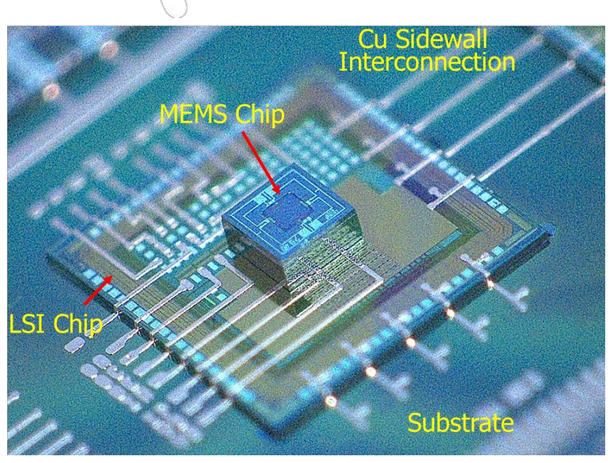


To do AI calculation, traditional 2D-IC has to expand area and conventional 3D-IC has to increase # of stack layers, cyclic operation enables the huge number of multiply-accumulate processing required for deep learning with a small number of layers.

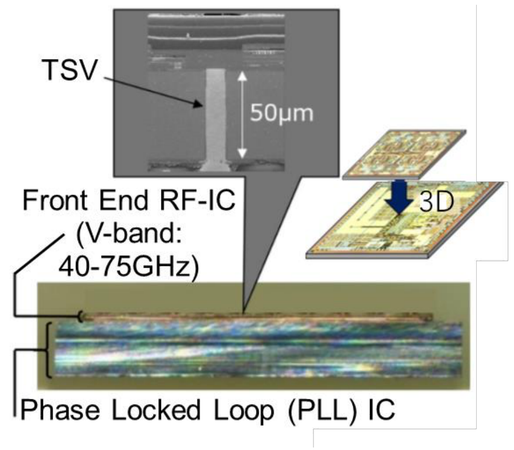
Neuro chip-on-DRAM:
Kiyoyama, Fukushima & Koyanagi *et al.*,
3DIC 2021 (Best Paper Award)



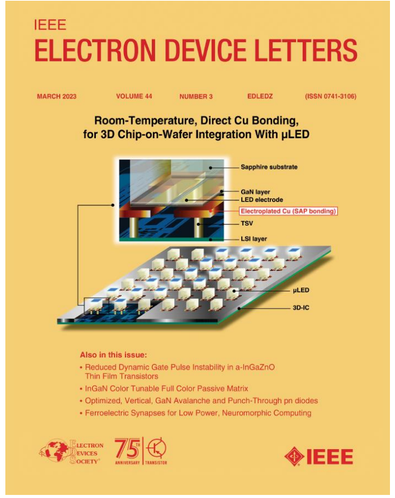
MRAM-on-Logic:
T. Tanaka et al., VLSI Symp., 2012



MEMS-on-CMOS chip:
T. Fukushima *et al.*,
IEEE T-ED, 2017



SiGe RFIC-on-Control IC:
Mitsubishi Electric, T-Micro, and Tohoku Univ. 2021



μLED array-on-Logic
T. Fukushima *et al.*,
IEEE EDL, 2023

CONLUSION

This research focuses a via-last die-level TSV formation process designed for small-batch, research-friendly, and short TAT (turnaround time) 3D-IC fabrication. This multi-die-level processing offers greater flexibility and cost-effectiveness compared to traditional wafer-level approaches. The utilization of standard magnetron sputtering, not ionized PVD, for seed/barrier layer deposition further enhances cost-efficiency and accessibility. This die-level approach demonstrates the potential for low-cost and rapid prototyping of 3D-ICs, enabling researchers to explore novel architectures and functionalities with greater ease and efficiency.

Useful Links for Technical Posters

- https://www.lbc.mech.tohoku.ac.jp/

- https://www.youtube.com/watch?v=3zPtmCtSOJg