

Process of Integrating MLOs Manufactured on Digital Lithography Systems



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Materials RF

INTRODUCTION

- High end advanced packaging (AP) is needed to answer generative AI demands with more die/chiplet integration, more HBM, high bandwidth and high density interconnections.
- Test intensity, test complexity and probe card demand increases as AP becomes widespread, making AP one of the main

Tech industry electronics Packaging & Test Wafer production Device design 22% 62% 16% 2023 **Fabless** ~\$530B Fabless players 37% Open wafer foundries IDMs Assembly 63% & Test wafer foundries Suppliers EDA & IP

drivers for the probe card market [1].

Alignment marks New test structures L/S patterns feature size Various additional patterns

- The maskless exposure's processing pipeline electronically processes the vectorized data and corrects for distortion during write-time, based on pre-measured and real-time acquired alignment information before it gets sliced up into stripes.
- These are digitally sampled and delivered to the FIFO-buffered exposure head controller. During exposure by the maintenance free laser light source, the head engine already generates the successive stripe in the throughput-optimized processing pipeline [2].

RESULTS & DISCUSSION

- MLE was employed on a multiexposure head LITHOSCALE® to prove the suitability of the technology for MLOs in fine pitch probe cards. **Targeting** the application requirements, newly developed "LTC 9320-E76B next Fujifilm Electronic gen" by Materials, negative tone, low temperature cure dielectric polyimide was evaluated.
- Operating at two wavelength (λ≈375 and 405 nm) the broad process windows matrix setup

→ Regular VIA enable homogenous ECD in subsequent integration of MLOs.

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ensures the efficient process

CONEVAIGHTING. & OUTLOOK

- MLE is a versatile technology finding applications in probe cards, photonics, MEMS, next-generation advanced packaging, and many new, emerging markets!
- EVG's digital lithography equipment, LITHOSCALE®, is designed to facilitate rapid R&D prototyping & expeditious transition from to HVM!

REFERENCES

- G. Periera: Advanced Packaging Pushing the Boundaries of the Semiconductor Probe Cards Market, Podium Presentation at SW Test USA, June 2024.
- K. Varga: Digital Lithography Enhances Fine Pitch Probe Cards Performance, Podium Presentation at SW Test USA, June 2024.

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