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Addressing High-Speed Devices: Strengthening and Advancing MEMS Probe Cards

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Overview

- **Introduction / Background**
- **Objectives / Goals**
- **Optimization Approach for Spring Type Probe**
  - Methods / Key Data / Results
- **Optimization Approach for Buckling Type Probe**
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- **Results**
  - Valid by Customer /Discussion of Results / Relevant Findings
- **Summary / Conclusion**
- **Follow-On Work**

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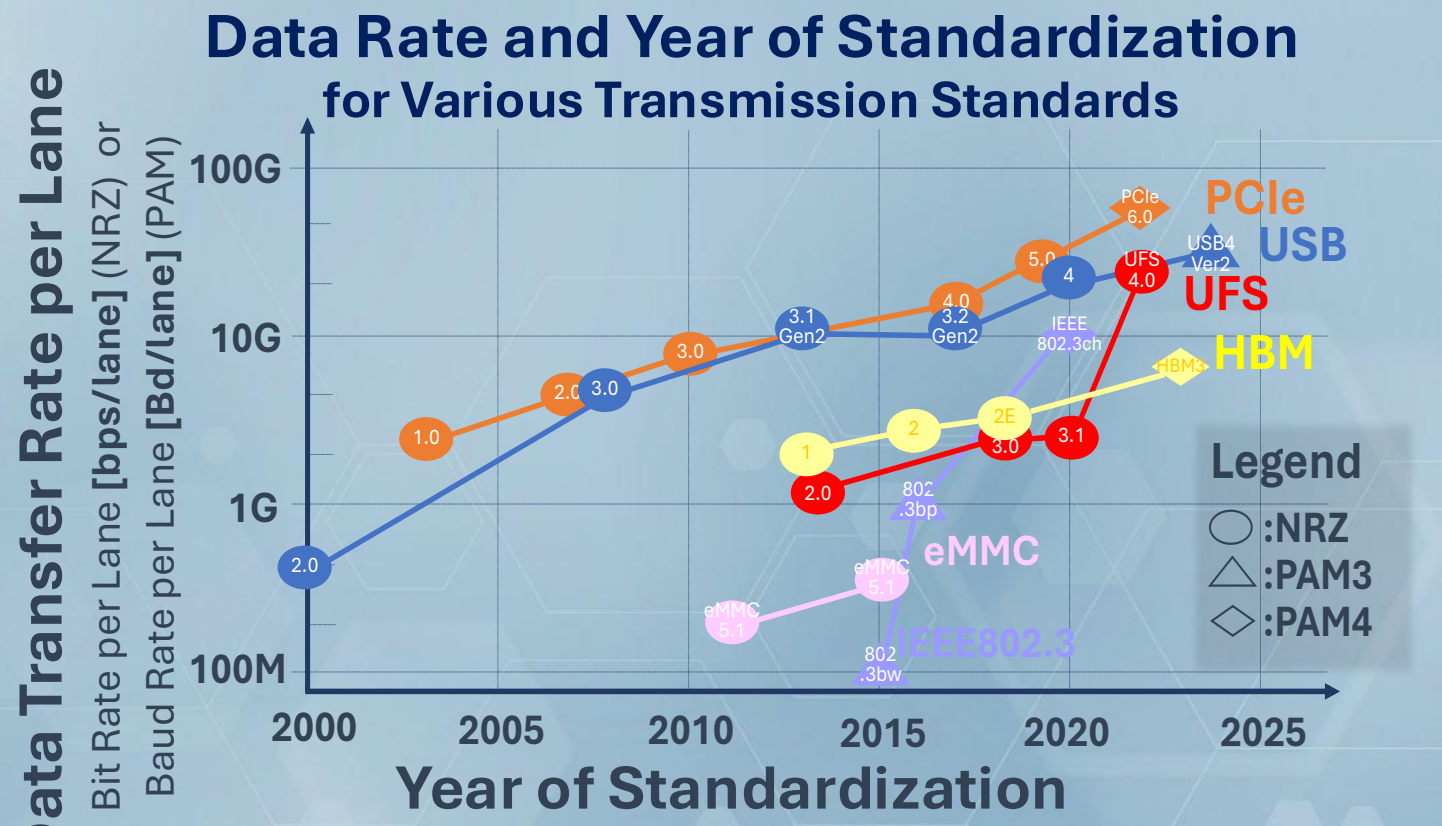
Introduction / Background

- **The Data Transfer Rate has been increasing year by year.**
  - Leading to a surge in testing for high-speed devices.
  - The demand for high-frequency compatible probe cards is increasing.



Data Transfer Rate per Lane: Data Transfer Rate per 1lane of Physical Layer , **bps:** Bit per second, **Bd:** Baud Rate (Symbol Rate), **NRZ:** Non-Return to Zero, **PAM:** Pulse Amplitude Modulation, **USB:** Universal Serial Bus is a versatile Standards primarily used for data transfer, power supply and so on, **IEEE802.3:** Protocol typically used for Automotive Communication Standards, **HBM:** Protocol for Memory Technology, **PCIe:** for Expansion Bus, **eMMC:** Flash Memory Physical Layer, **UFS:** Flash Memory Standard.

Data Source: [PCIe] PCI-SIG (https://pcisig.com/) **[USB]** The USB Implementers Forum (USB-IF) (https://usb.org/) **[UFS/HBM/eMMC]** JEDEC Solid State Technology Association (https://www.jedec.org/) **[IEEE802.3]** IEEE Standards Association (https://standards.ieee.org/)

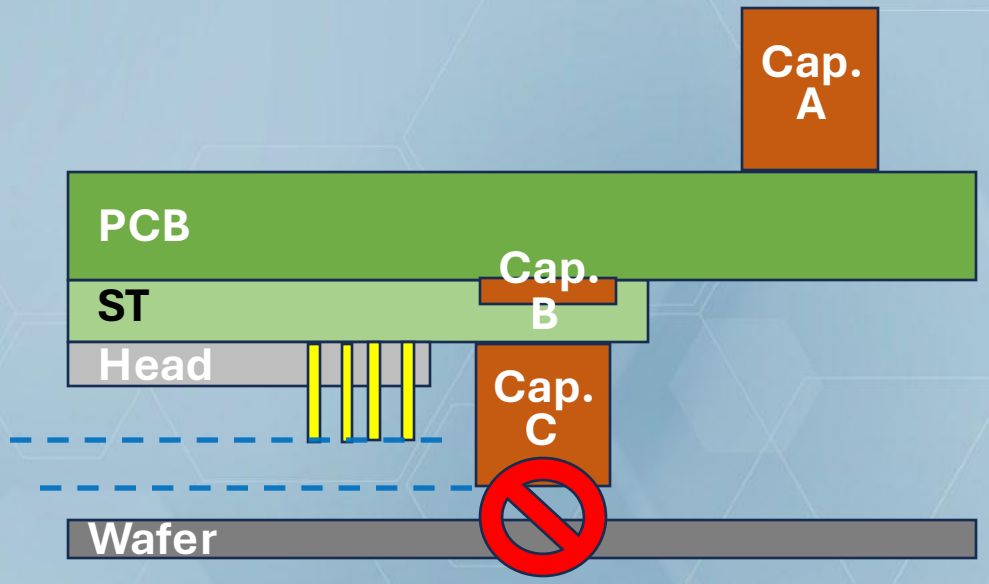
Introduction / Background

- **Structural Challenge for High-Speed Compatibility**
  - In **high-speed** probe cards, **shortening the probe length** may become necessary. However, in many cases, this leads to significant **structural issues**:
    - **Reduced Probe Life**
    - **Excessive Contact Force**
    - **Poor Probe Replacement**
    - **Limited Component Space** *(→details on next page…)*

  - ✓While **high-speed compatibility** is crucial, it is equally important to **balance** probe length with structural functions such as **easy probe replacement** and **component implementation options**, and performance requirements, such as **probe life longevity** and **contact force flexibility**.

Introduction / Background

- **Issue:** **Height restrictions prevent placing components near the probe.**
- **Considerations:**
  1. **Position-A** (e.g., **Capacitor on PCB):**
     ✓Significant SI/PI degradation
  2. **Position-B** (e.g., **Cap in ST~PCB):**
     ✓Size and signal routing challenges
- **Needs:**
  3. **Position-C** (e.g., **Cap near Probe):**
     Use probe of **minimum necessary length** for components:
     ✓Minimize height restrictions
     ✓Better flexibility in placement
     ✓Optimized PI/SI



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Objective / Goals

- **Objective:**
  - Achieving **High-Speed Performance** while maximizing structural benefits such as:
    - **Easy Probe Replacement**
    - **High Flexibility in Component Placement Near the Probe**
    - **Longer Probe Life**
    - **Ease of Adjustment for Optimal Contact Force**
- **Goal:**
  - Achieve **High-Speed** performance by **balancing** Impedance Matching with satisfying the **Structural Requirements** to the fullest extent.

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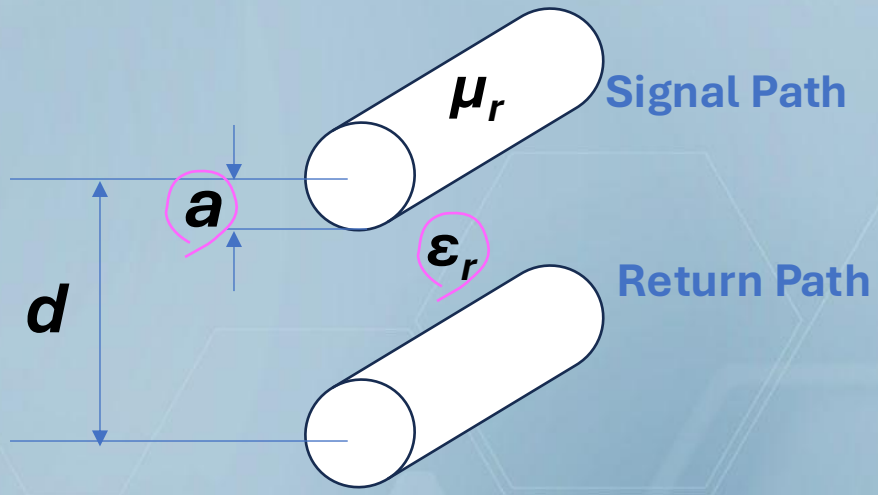
Method: Impedance of Thin Rod Shape

- **Impedance of Thin Rod Shape:**
  - The Impedance(***Z_0***) of the Thin rod depends on:
    - ✓**Pitch(*d*)** of the opposing rod
    - ✓**Radius(*a*)** of the rod
    - ✓**Material parameters(μ_r,ε_r)** between the rods

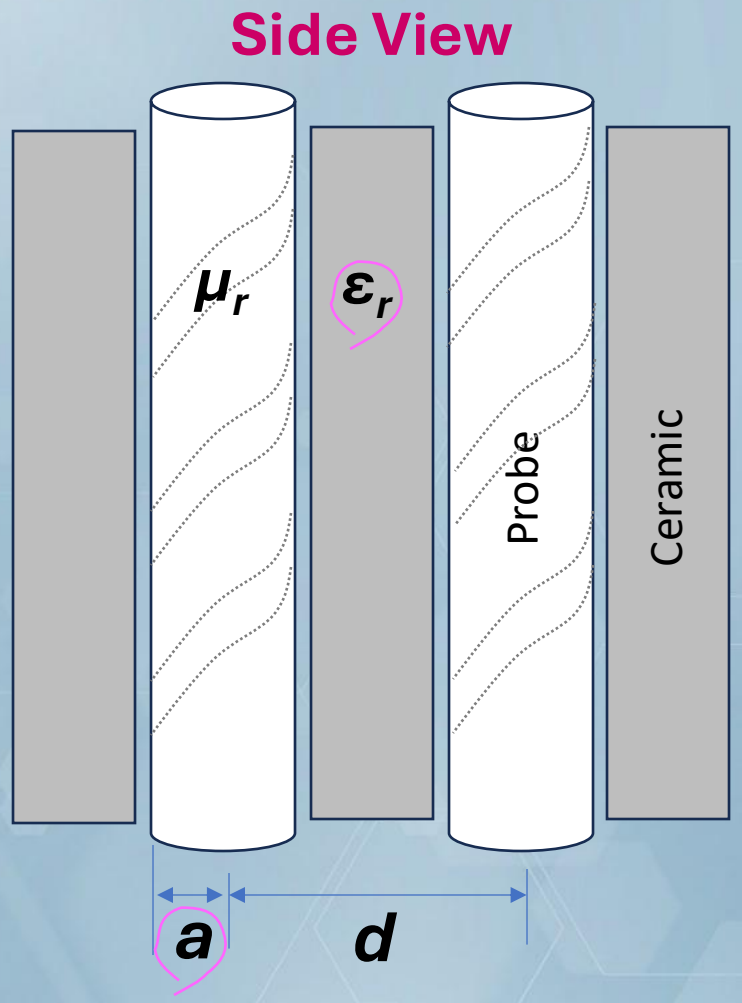


$$Z_0 = \frac{\eta_0}{\pi}\sqrt{\frac{\mu_r}{\varepsilon_r}}\ ln\frac{d}{a}$$

d : Pitch of the opposing rod
a: Radius of the rod
μ_r : Relative Permeability
ε_r : Relative Permittivity
η_0 : Intrinsic Impedance of Free Space ~ 377Ω

Method: Spring-Type Probe

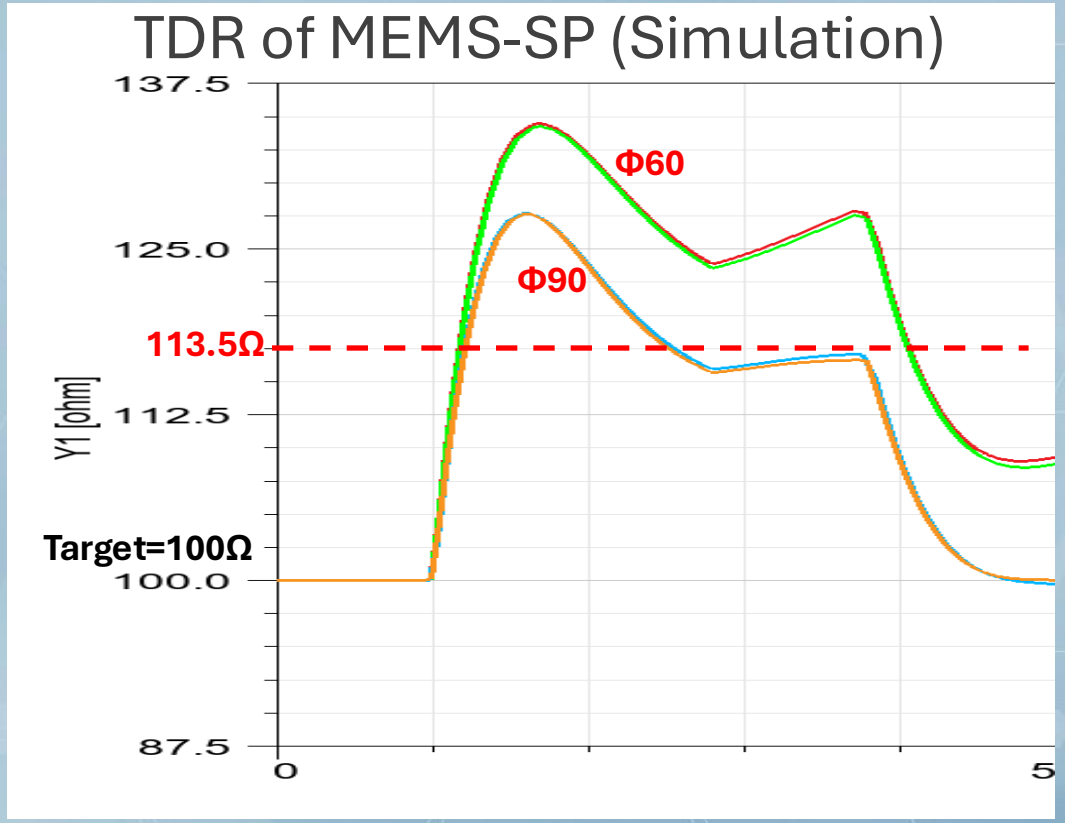
- **Key Parameters:**
  - Impedance(Z_0) depends on not only the **geometrical parameters**(*a,d*) of the signal and ground probes,
  - But also the parameters related to **materials** and **structure**(μ_r,ε_r).
  - Pitch: 80μm to 150μm.
- **Strategy:**
  - **Optimize** the **structure** and **materials** for layout and pitch.



$$Z_0 = \frac{\eta_0}{\pi}\sqrt{\frac{\mu_r}{\varepsilon_r}}\ln\frac{d}{a}$$

Key Data: TDR of Spring Probe

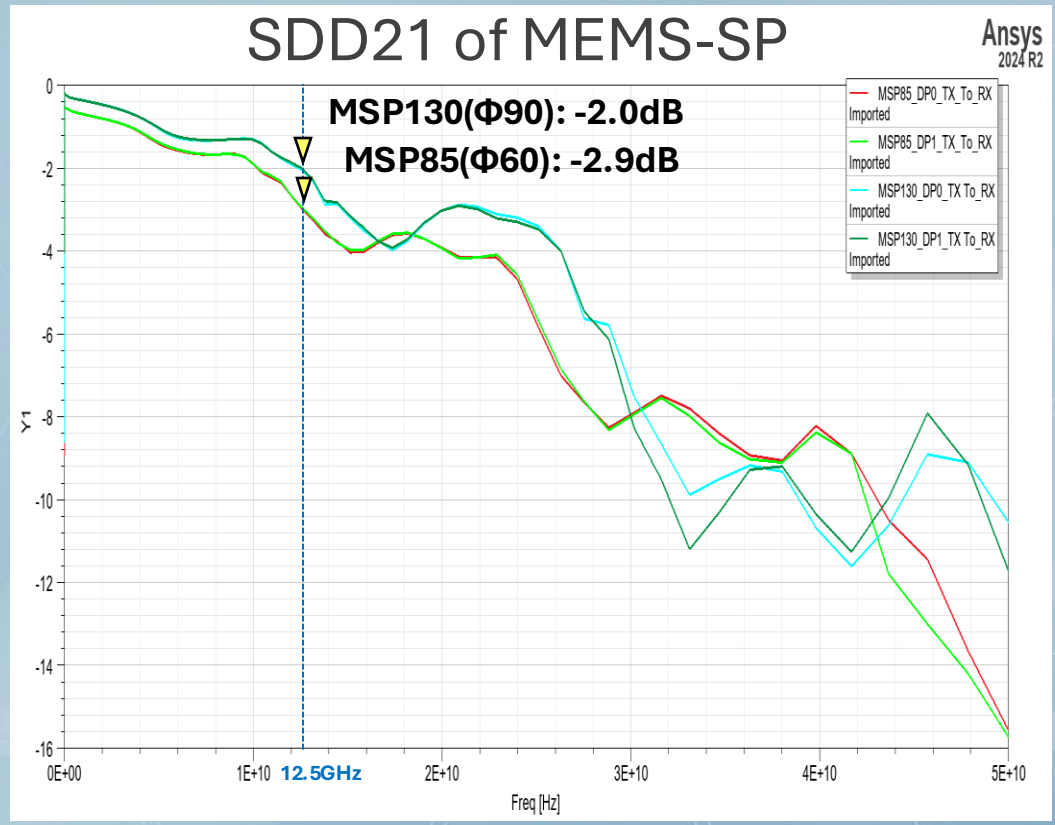
- **TDR of Spring-Type Probe:**
  - Modeled with **customer's UFS array** configuration.
  - Used two different probe diameters for 80μm(Φ60) and 130μm(Φ90) pitch.
- **Results:**
  - The differential impedance for the thicker probe at **130μm pitch(Φ90)** was **113.5Ω,** better than Φ60.



***TDR：** Time Domain Reflectometry

Results: S-parameters of Spring Probe

- **Measured Differential S-Parameter (SDD_{21}) of Spring-Type Probe:**
  - **Differential Insertion Loss** (**DIL, SDD_{21}**) measurement of the spring probe are shown in the graph.



- **Results:**
  - **Φ90: -2.0dB**
  - **Φ60: -2.9dB**

  Good performance obtained for UFS 4.0(23.2Gbps)

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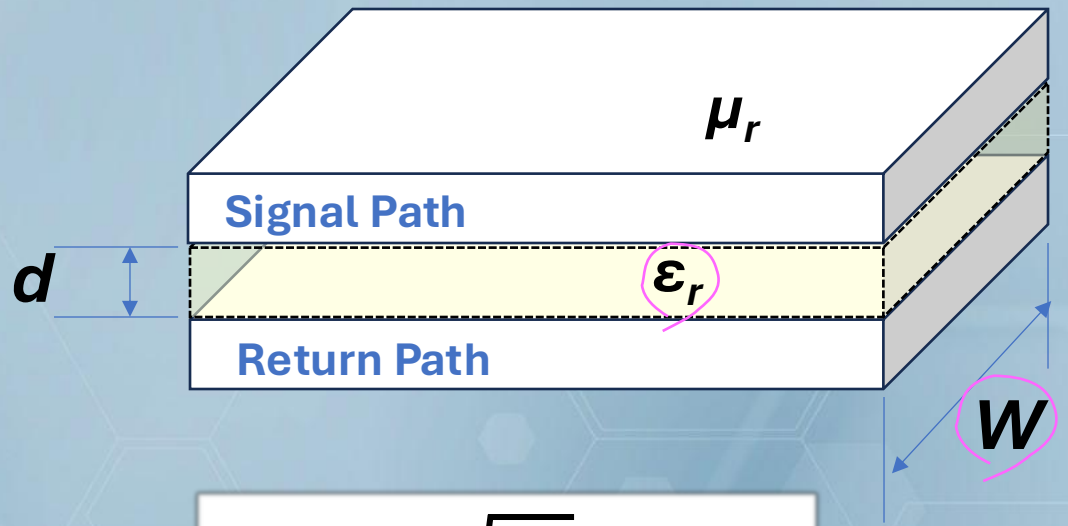
Method: Impedance of Flat Shape

- **Impedance of Flat Shape:**
  - The Impedance(Z_0) of the Parallel Plate Conductor depends on:
    - ✓**Width(*W*)** of the plate
    - ✓**Distance(*d*)** of the opposing plate
    - ✓**Material parameters(μ_r,ε_r)** *of* the plates and insulator

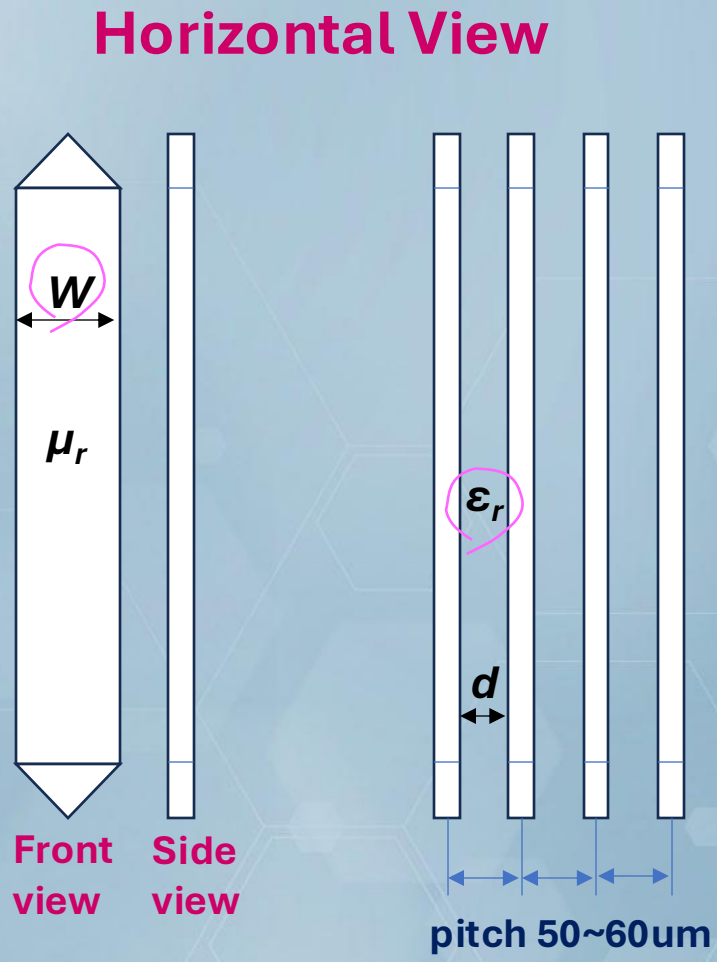


$$Z_0 = \eta_0 \sqrt{\frac{\mu_r}{\varepsilon_r}} \ln\frac{d}{W}$$

d *: Distance between parallel plates*
W *: Width of the parallel plates*
μ_r *: Relative Permeability*
ε_r *: Relative Permittivity*
η_0 *: Intrinsic Impedance of Free Space ~ 377Ω*

Method: Buckling-Type Probe

- **Key Feature:**
  - **Flat Shape:**
    - ✓ To optimize parasitic capacitance between probes, the area is expanded.
  - **Material and Structural Adjustments:**
    - ✓ Adjusts dielectric properties to achieve impedance matching.
    - ✓ The structure is optimized by customer pitch specifications.



$$Z_0 = \eta_0 \sqrt{\frac{\mu_r}{\varepsilon_r}} \ln\frac{d}{W}$$

d : *Distance between parallel plates*

W : *Width of the parallel plates*

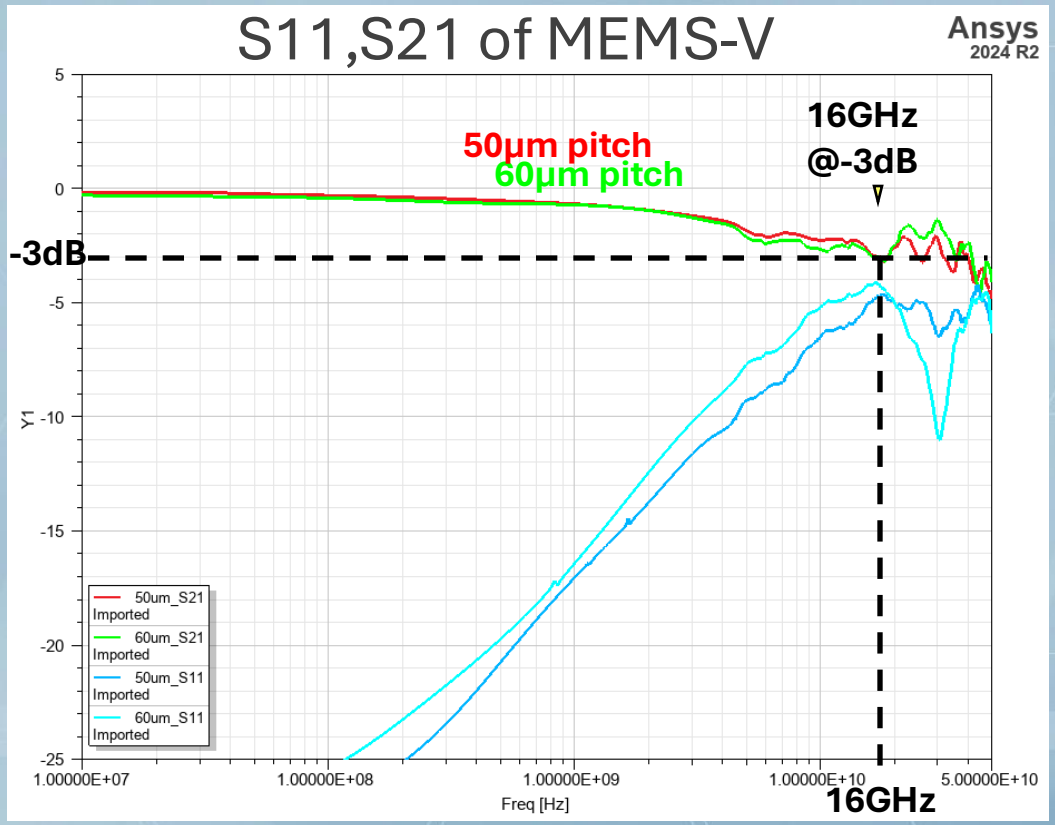
μ_r : *Relative Permeability*

ε_r : *Relative Permittivity*

η_0 : *Intrinsic Impedance of Free Space ~ 377Ω*

Result: S-parameters of Buckling Probe

- **Measured S-parameters of Buckling-Type Flat Probe:**
  - **Reflection coefficient(S_{11})** and **Transmission coefficient(S_{21})** are shown in the graph.
  - The **S-parameters** characteristics show **good performance** at both **50μm and 60μm pitch**.
- **Results:**
  - **Frequency Response:** -3dB at16GHz (for both 50μm pitch and 60μm pitch)



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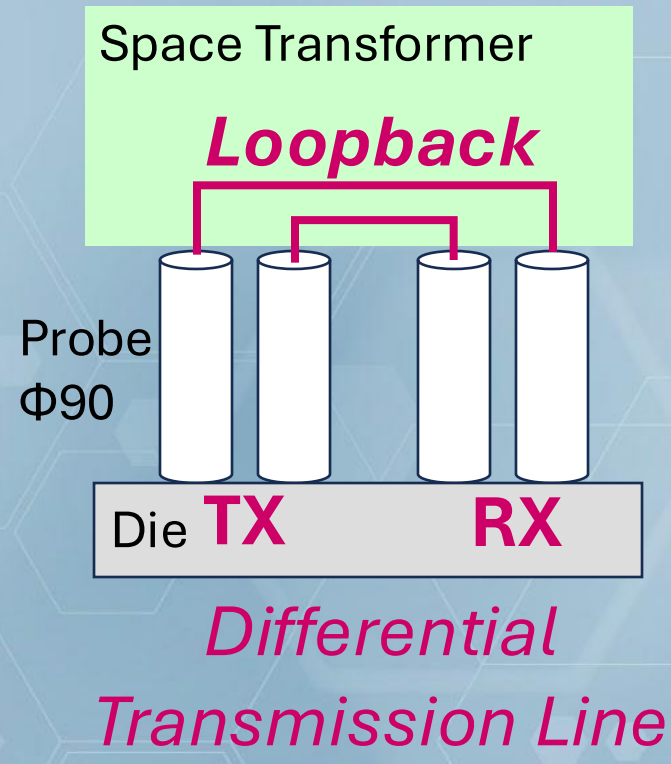
Results: Validation by Customer

- **Customer Validation via Loopback Testing using Optimized Probe Cards.**
  - Optimized probe cards have successfully achieved **23.2Gbps(UFS4.0) Loopback Test** with Φ90 probe at temperatures ranging from **-40℃** to **+135℃**.
  - Equipped with both **Φ90 and Φ60 Spring Probes**.
  - **Pin Count : >10,000pins (20Multi.)**
  - Utilizing **optimized minimal length probes** allowed us to avoid the following issues :
    - ✓Reduced Probe Life
    - ✓Excessive Contact Force
    - ✓Poor Probe Replacement
    - ✓Limited Component Space



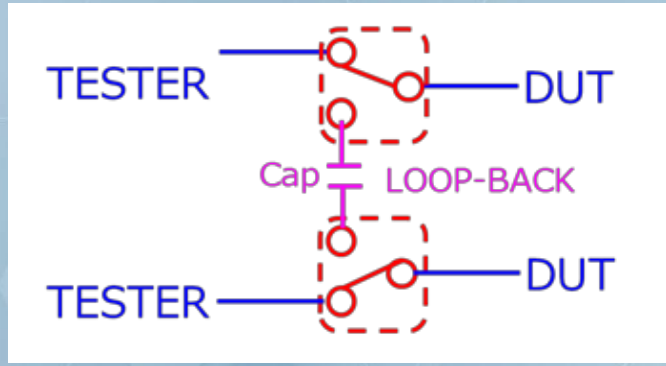
Discussion of Results

- **Achievements:**
  - **High-speed performance with optimized materials and structures**
  - Maintained probe replaceability and component placement
- **Challenges and Future Directions:**
  - Advanced high-speed testing requires more than probe improvements.
  - Optimizing the entire signal path is crucial.
  - **Key challenge: Efficiently placing components near the probes**
- **Exploring Critical Components:**
  - **Study on improving critical component placement near the probes** (Details in the next slide)

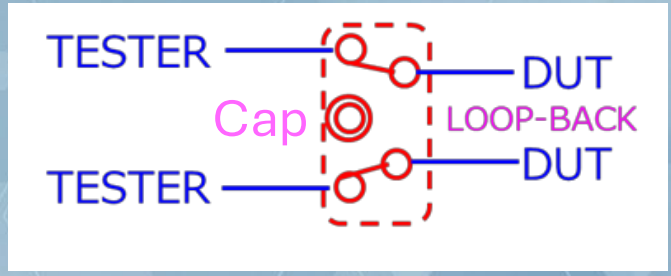
Relevant Findings and Innovations

- **Specialized Relay for Loopback Test**
  - **Function:**
    - ✓External Loopback Relay for switching between Tester-path and Loopback-path.
  - **Key Feature:**
    - ✓**Single Packaged Relay**, called **"M Contact Relay"**, featuring a built-in capacitor,
    - ✓Instead of the **usual Total Three Components** (Two packaged relays and one external capacitor).
  - **Expected Benefits:**
    - Reduced implementation area.
    - Advantageous for **SI** by placement **near the probe**.

Conventional
(Two Relays and One Cap.)



"M contact Relay"
(Single Packaged Relay with built-in Cap.)



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Summary /Conclusion

Balancing *Structural Integrity* and *Signal Integrity* (*SI^2*) for High-Speed Test by MEMS Probe Cards.

1. **Structural Challenges and Solutions**
   - Utilizing **minimal length** probes that satisfy for **structural requirements**.
2. **Strategies for SI/PI**
   - Realizing high-speed performance by **optimizing materials and structures** for impedance matching.
3. **Customer Validation**
   - **Successful** 23.2Gbps (UFS4.0) **Loopback Test** at -40℃ to +135℃.
   - Over 10,000pins, 20Multi, with MEMS Spring Probe Card.
   - Enabling single **probe replacement,** optimal **contact force** and **longevity**.

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Follow-On Work

- **Enhance balance between *Structural Integrity* and *Signal Integrity* (SI^2) for advanced High-Speed Testing.**

- **Explore advanced component placement strategies.**

Question?