

Modeling and Simulation of ATE DUT Boards for Large Pin Count Applications

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Overview

- Industry trends and ATE challenges
- PCB DUT board mechanical modelling and Young's Modulus measurement.
- PCB DUT board stiffener and importance of the ATE docking mechanics.
- Simulation and measurement examples
- Conclusions

Industry Trends

- Two industry trends are pushing ATE test cells to have large channel counts and larger DUT Board PCB sizes:
 - Larger DUT package pin counts (e.g. High-Performance Computing ICs) with high power requirements
 - Large multi-site configurations to reduce cost of test (e.g. 32 sites).



IEEE ECTC 2024 5.5X 3.3X 1.6X 1.7X SoC + 12 HBM3/4 1.4X CoW size: 66x68 mm² Body size: 97x95 mm² Passed PoC + TCC1000 4 SoC + 8 HBM3 CoW size: 54x50 mm² 04 2025 Qual Pass 2 SoC + 4 HBM3 1 SoC + 2 HBM2E 1 SoC + 8 IO Die Body size: 78x72 mm² CoW size: 39x34 mm² Passed Extreme test including CoW size: 39x34 mm CoW size: 34x27 mm² Body size: 100x72.5 mm² TCC2500 Body size: 55x55 mm² Body size: 90x90 mm **Risk production** In production Qual pass Fig. 1 CoWoS-R Development

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AMD Ryzen Threadripper GPU

ATE Challenges

- How to address these industry challenges?
 - Increase the spring pin density and quantity (e.g. 8000 pins or more)
 - PCB routing becomes more challenging.
 - DUT board docking force increases.
 - Increased mechanical precision alignment requirements.
 - Larger DUT board PCB size
 - Higher manufacturing costs.
 - Larger manufacturing inaccuracies at pogo via area.

V93000 pogo block density increase





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V93000 DUT board size increase

PCB DUT Board Mechanical Modeling is Hard



- A PCB DUT board is a composite material which makes its modeling not trivial since it depends on:
 - Layer count and PCB stackup.
 - Layout structures (copper density)
 - Dielectric material mechanical properties.
 - Copper thickness.
 - Temperature
- Another option is to use a measurement-based modeling approach.

Megtron 6 example

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Part No.	Water Absorption (%)	Poisson's Ratio	Flexural Warp (MD) (GPa)	Flexural Fill (TD) (GPa)	Peel Strength (1 Oz. Cu) (kN/m)
R-5775(K)/R-5670(K)	0.14%	0.2	19 GPa	18 GPa	0.8 (Cu:H-VLP) kN/m

Measurement of PCB Young's Modulus

Setup



Procedure:

- motorized driving of gauge onto sample piece
- read-out of respective force-displacement value-pairs at specific positions

Challenges:

- not directly measurable
- calculation from other, appropriate quantities that are directly measurable (*force/displacement, geometrical dimensions*)

Limitations:

- propagation of various measurement errors into final values
- one- vs. multi-point measurements (*statistical approaches*)

Results for PCB Young's Modulus





Measured PCB:

- 6.5 mm thickness, Megtron 6 dielectric
- 27 layers

This data is for one specific measured PCB sample

PCB DUT Board Stiffener and ATE Docking

- The DUT board stiffener is a critical part of the DUT test fixture assembly.
- Its mechanical modeling is easier since it is a solid metal part.
- But its important to understand that the ATE testhead interface docking mechanism will also have a direct impact on the mechanical behavior of the stiffener/ DUT test fixture.
- But to model this interaction requires details on the ATE testhead which are not readily available.





Simulation Example

- In this simulation example we want to simulate the deflection of the PCB DUT board due to a single ATE pogo block.
- For this experiment a pogo block with 150 N total force was used. This is more than twice the force of the V93000 highest density pogo block (VHD).
- The objective is to develop guidelines for the minimum thickness required on ATE DUT boards for high-pin count ATE configurations.
- Two models are compared:
 - DUT PCB board plus stiffener only.
 - DUT PCB board plus stiffener docked to a simplified model of the ATE test fixture interface.



Simulation Results

- The ATE testhead interface has a significant impact on the mechanical behavior of the ATE test fixture.
- To improve the mechanical simulation results it is important to include the key features of the ATE test head docking infrastructure and also the correct boundary conditions.

Simulation without the ATE Docking interface



Simulation with the ATE Docking interface

0.092 mm

Simulation to Measurement Correlation







Good correlation achieved by using a measurement-based model for the PCB and including part of the ATE test head docking mechanism.

Extrapolation to Another PCB DUT Board



In this example we use the previously measured PCB Young's modulus for a different PCB test fixture with 3.5 mm thickness and a different stackup/dielectric material.

Simulation without the ATE docking interface

0.08 mm 0 190 0 192 0 193

Simulation with the ATE docking interface

Simulation to Measurement Correlation



- In this example the measurement to simulation correlation is worse.
- The main reason is the assumption that we can use the same measured material parameters (25.65 GPa) for a completely different stackup/board thickness.
- To improve this correlation we would need to obtain new measured material parameters using this exact PCB board.
- Note that the large measured deflection value is due to the small thickness of the DUT board and the high force of the pogo block used for this experiment. In a real scenario like wafer probing the deflection is very low due to thicker DUT Board and the bridge beam.

Simulation to Measurement Correlation

Instead of a depth gauge it is possible to use a laser scanner for the Z-displacement measurements. But this approach required careful attention to measurement setup.

DUT board not docked

Keyence LJ-X8000

NEVENCE





DUT board docked

Conclusions

- PCB DUT board mechanical modeling and simulation is not trivial.
- A good mechanical model of the PCB is important.
- It is also important to include the critical features of the ATE testhead docking mechanism and set the boundary conditions correctly.
- This is a similar challenge faced by DUT sockets or probecards.
- These mechanical modeling challenges are further compounded by other requirements like power (e.g. 2 KW), thermal and signal integrity (e.g. 224 Gbps).

Thank You