SWTEST ASIA 2022

An Aging Worldwide Fleet of Parametric Test Equipment Versus the Modern Means of Determining Measurement System Vitality

TECHNOPROBE

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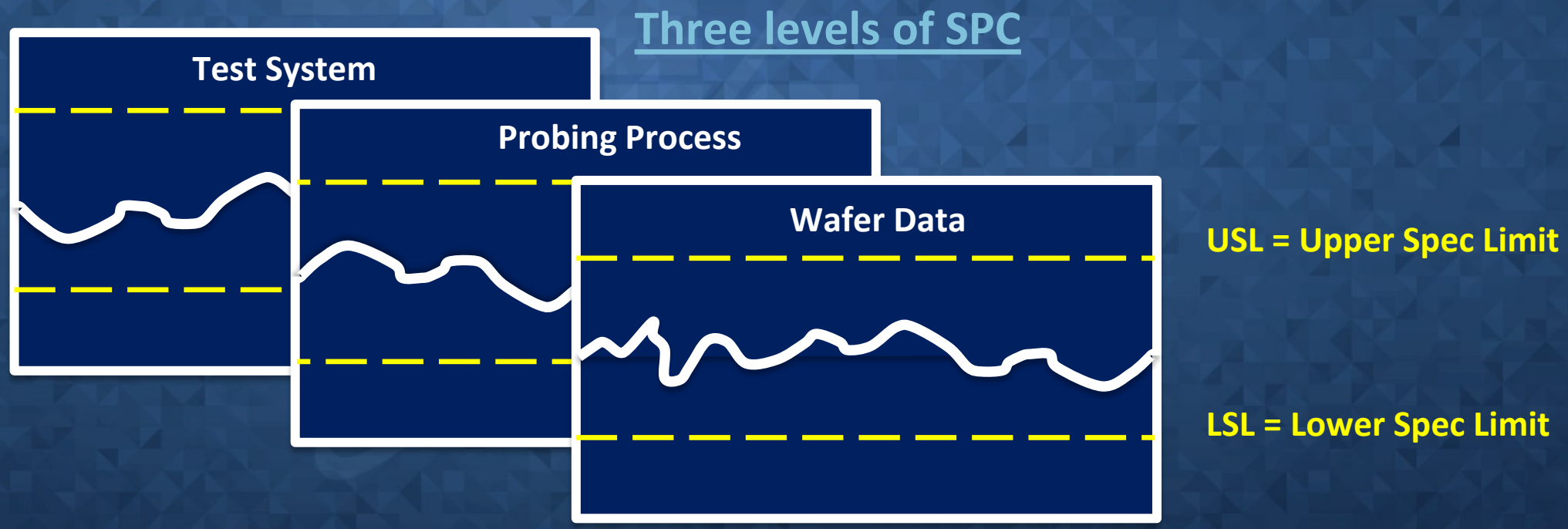
Goals/Objectives

- **Goal:**
  - Evaluate relationship between aging fleet of parametric test equipment versus the modern means of determining measurement system vitality
- **Objectives:**
  - Expand viewer's concept of Statistical Process Control (SPC)
  - Review common failures within test head matrix
  - Explore various designs of test structures and their data
  - Show physical behavior impacting measurement system vitality
  - Review test structure response of a compromised tester
  - Propose need for using control specs and double-sided limits
  - Examine traditional methods for evaluating tester performance
  - Discuss means of utilizing test data to self monitor system vitality

Statistical Process Control (SPC)

Three levels of SPC:

1) **Tester instrumentation accuracy against a known standard**
2) **Probing process attributes like P2P leakage, capacitance, contact resistance**
3) **Run time measurement performance of wafer silicon fabrication data**



Statistical Process Control (SPC) - Expanded

Expanding on wafer level SPC:

1) **Monitoring wafer data variation / stability**
2) **Post processing lot data on a given tester**
3) **Measurement performance across fleet of testers**

Wafer data **Lot data** **Fleet data**

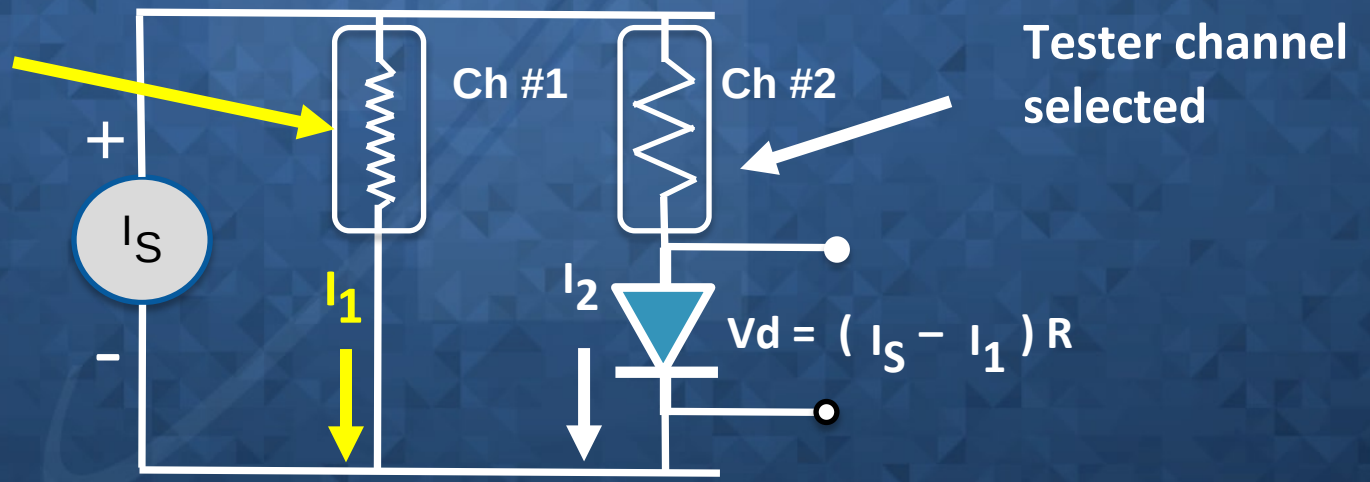
Degradation of Pin Board Contact Relay(s)

Impact due to high resistive short in unused channel:

- Parallel current path will lower applied current at DUT
- Lower current at DUT causes measured voltage to be lower

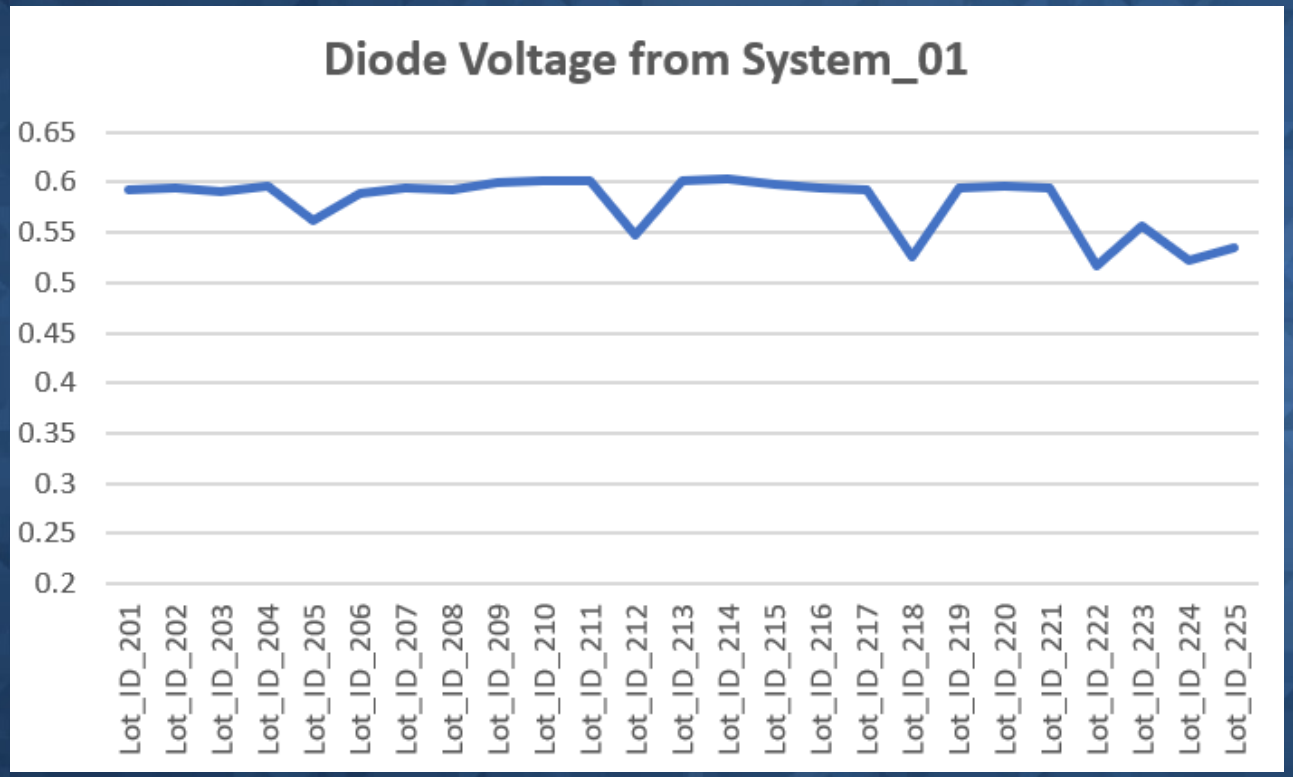
One channel test where the adjacent channel is shorted

Periodically unused tester channel #1 can fail and creates a high resistive short



Parametric test structures and their data

Measurement performance trends reflecting poor parametric test system health



Issue:

Unused tester channel with periodic high resistive short is drawing current away from the diode test structure

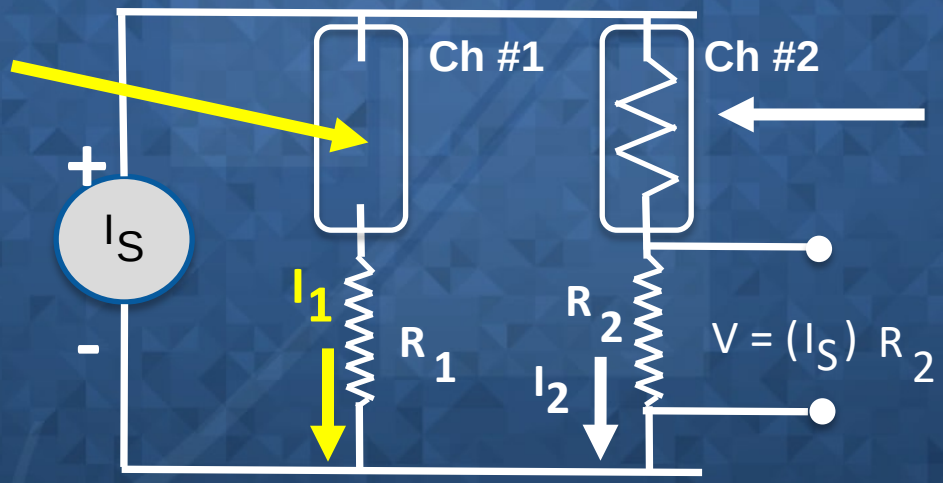
Degradation of Pin Board Contact Relay(s)

Impact due to open channel in parallel structure test:

- Open channel will increase output voltage across DUT

Two channel test where one of the channels used is open

Selected tester channel #1 failed and is completely open



Only channel #2 is properly working

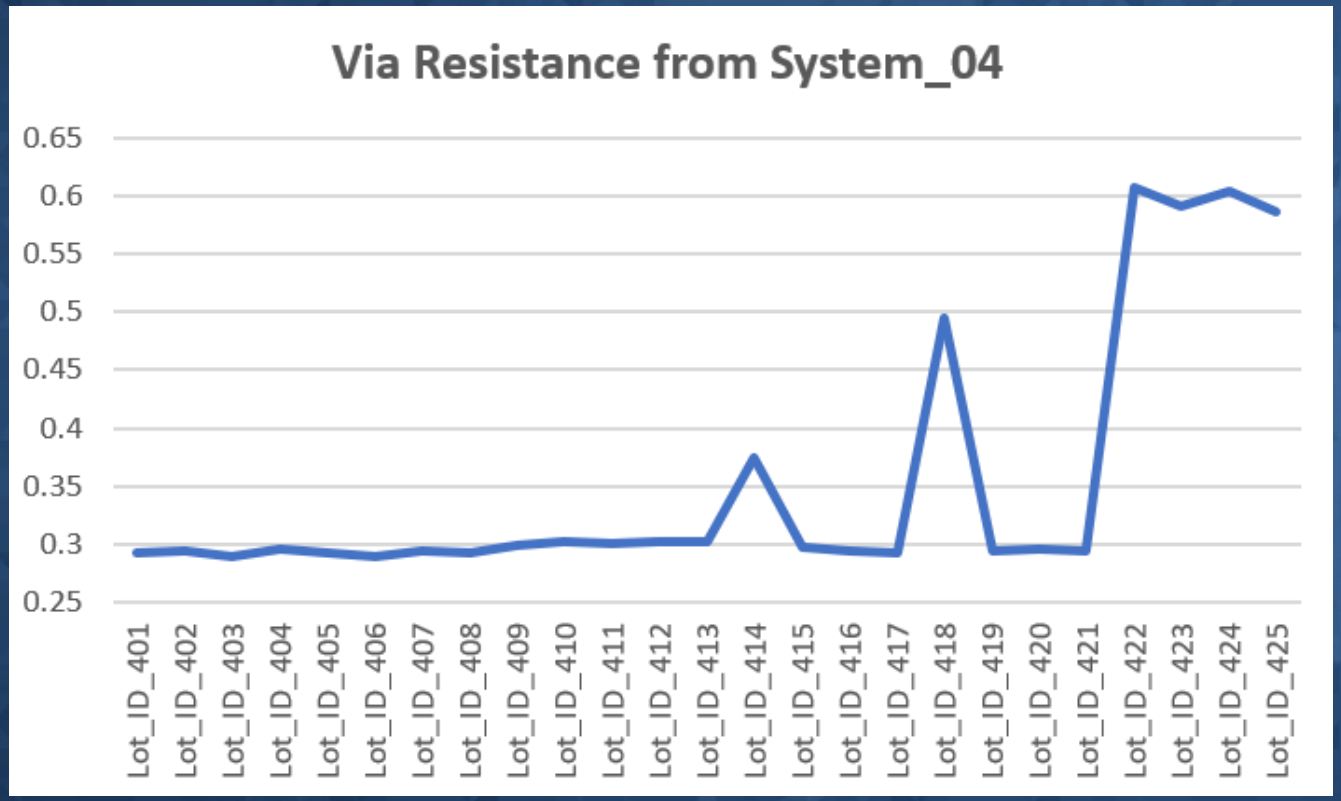
Note:

$R_1 = R_2$

Open circuit, so no draw of I_1

Parametric test structures and their data

Measurement performance trends reflecting poor parametric test system health



In a parallel resistor circuit channel #1 is failing and then goes completely open, which then directs all of the current into resistor R_2

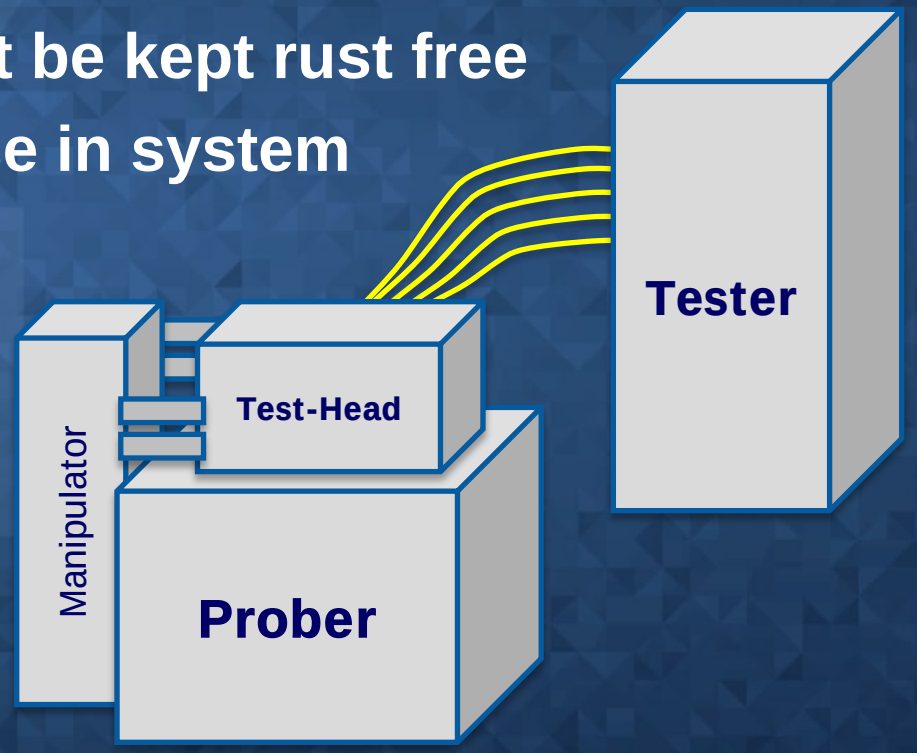
Note:

$R_1 = R_2$

Watch for Degradation of Tester Environment

Components and environmental changes can impact test results:

- Grounds are present on every piece of equipment
- Even the raised metal floor provides a conductive path
- Unpainted surfaces at grounding points must be kept rust free
- Degrading components will increase AC noise in system
- Reference ground must be free of noise



Parametric test structures and their data

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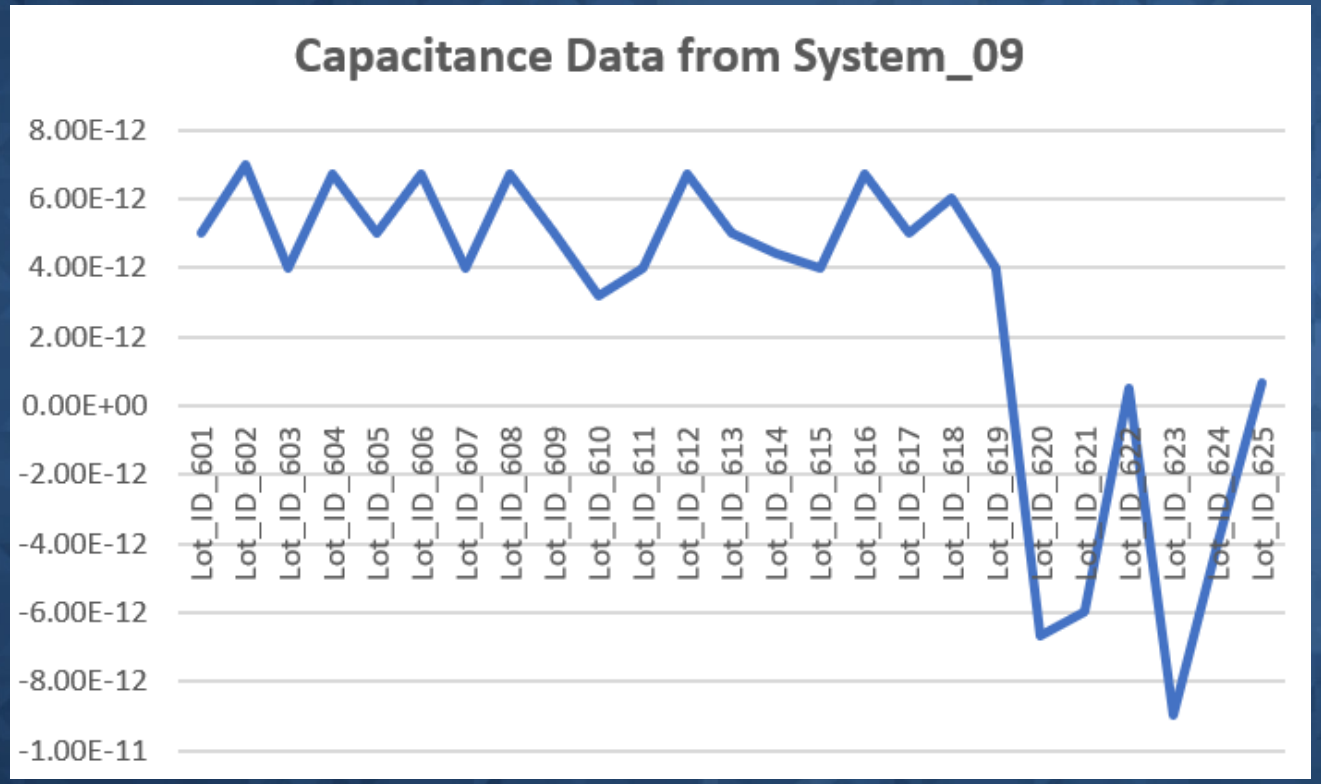


Test system is being impacted by AC noise injection by a failing component in prober or an environmental change

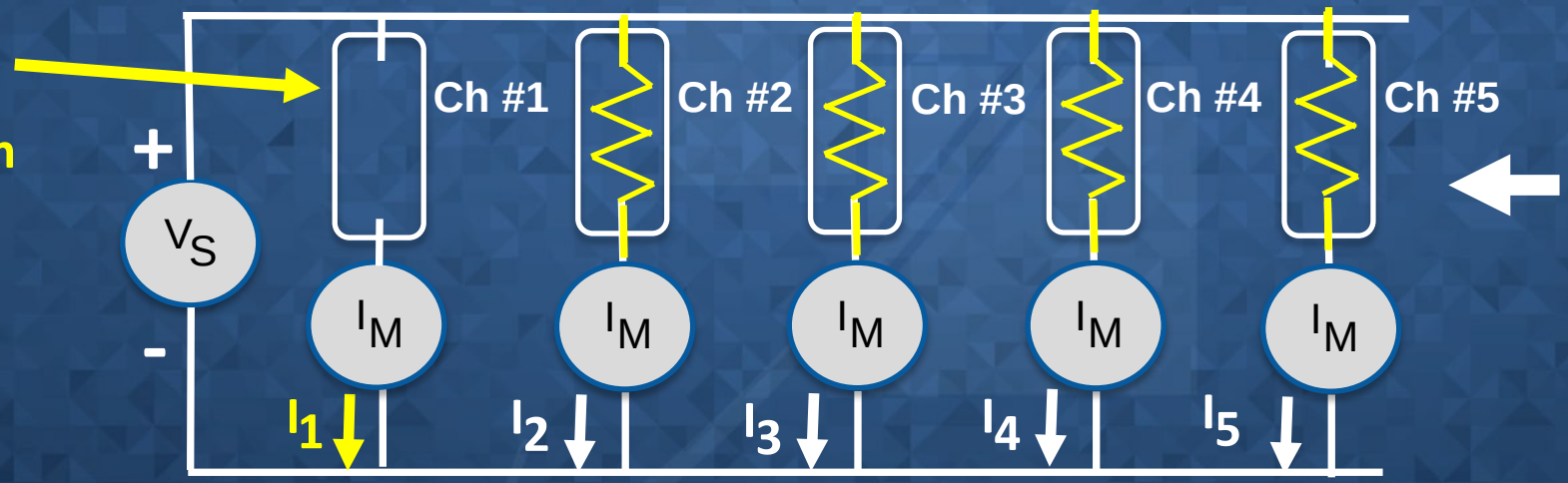
Degradation of Pin Board Contact Relay(s)

Impact of an open tester channel:

- Diffusion leakage current on channel #1 is pA's
- Test failure because channel #1 being open

Diffusion leakage test should have real data

Selected tester channel #1 is open

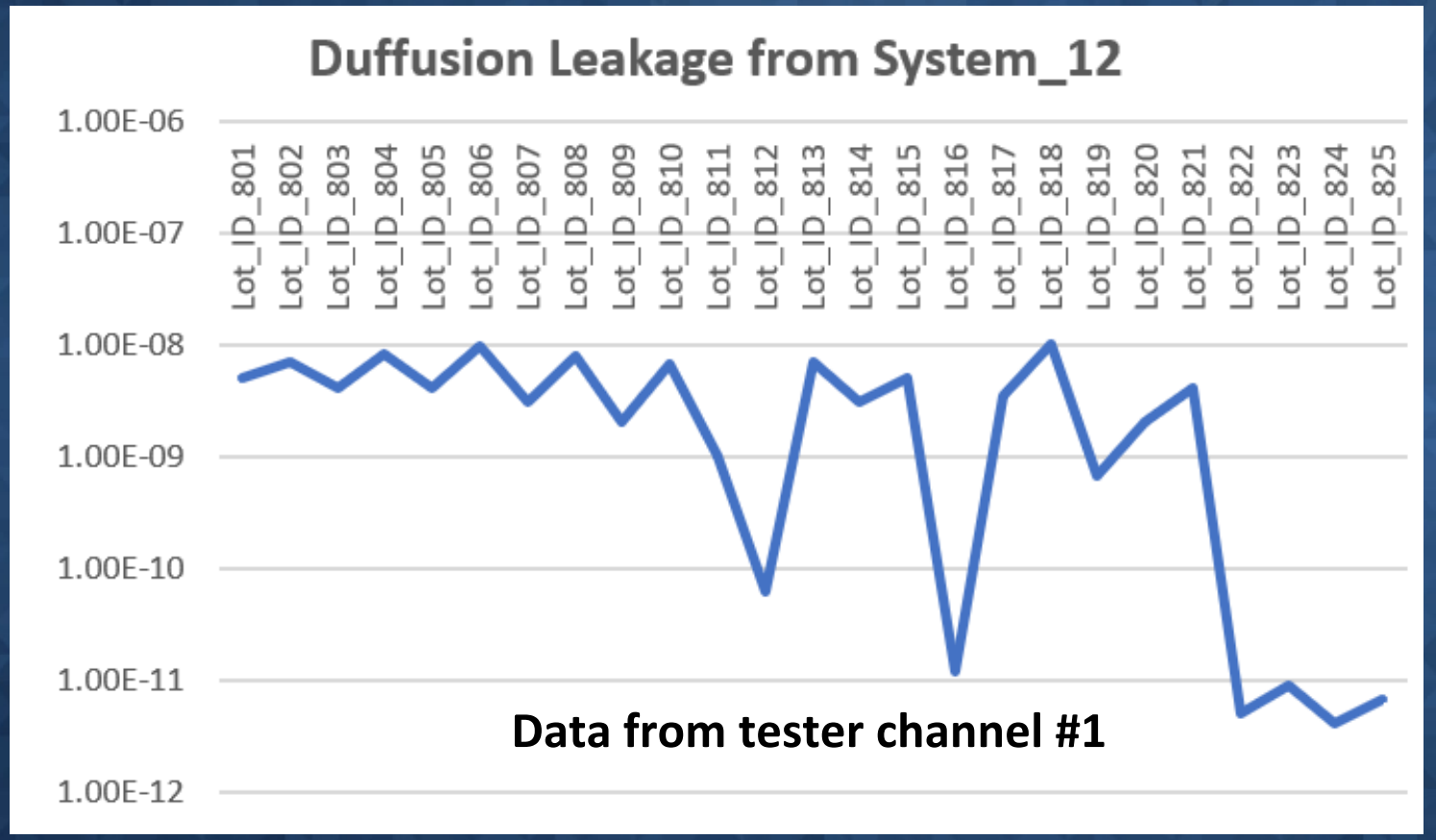


One at a time Channels #1 through #5 are testing transistor diffusions

Expect current readings in nA's

Parametric test structures and their data

Measurement performance trends reflecting poor parametric test system health

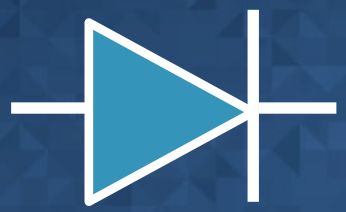


Channel #1 is failing and then goes completely open, so diffusion measurement #1 ends up being an open circuit

Parametric Test Structures and Their Data

- **Measurement performance of simple test structures provides insight into system health (Issue / Response)**

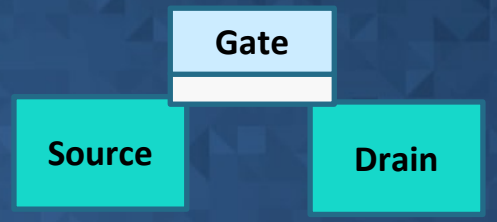
Diode



Very low resistive Contacts or Vias

Capacitor

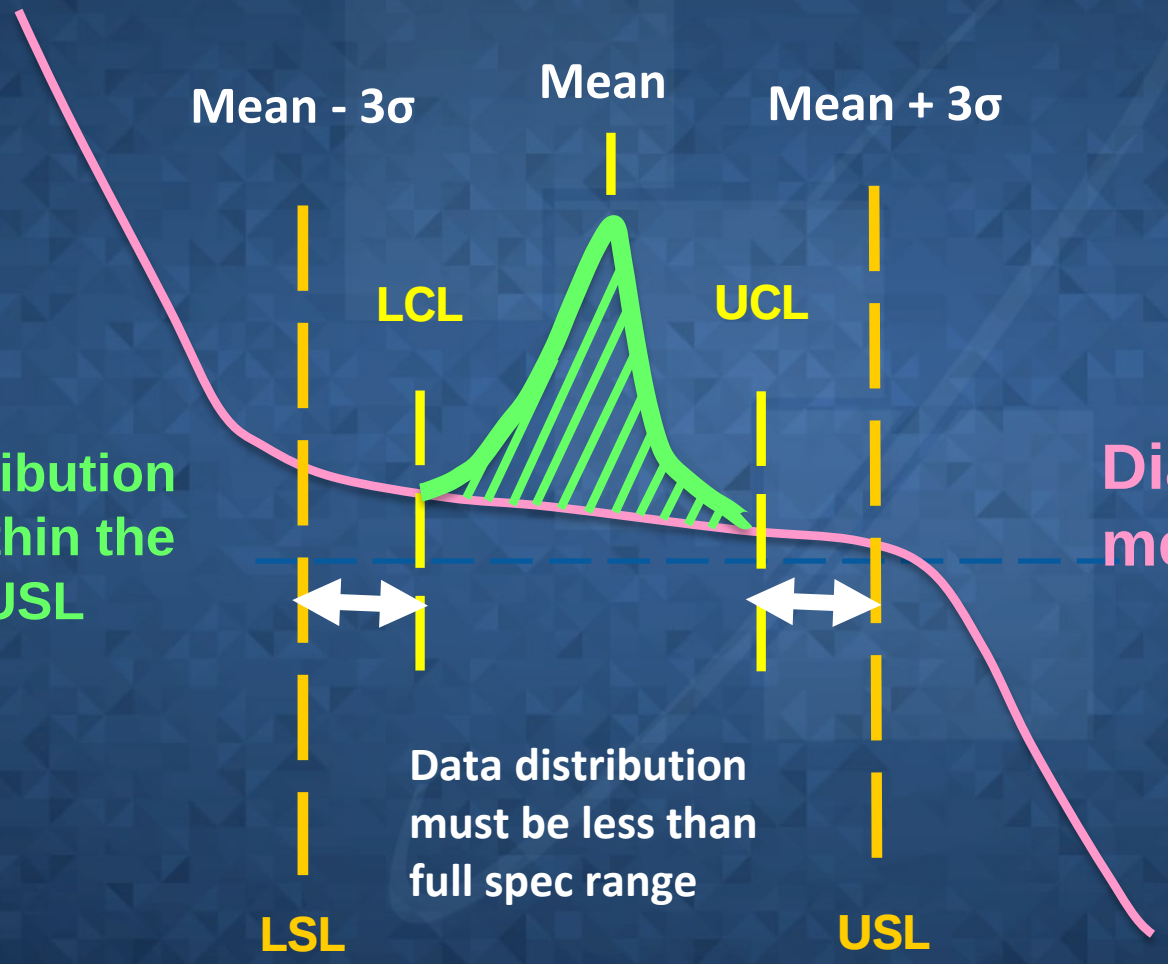
CMOS Transistor



Lower than expected V_d measurement	Higher than expected resistance measurement	Unexpected negative capacitance measurement	Lower than expected diffusion leakage measurement
Highly resistive short in test head	Open in parallel path of circuit	AC noise from failing part or environment	Open tester channel when making test

Parametric test structures and their data

Don’t fall victim to test data measurements which only use single sided limits



Note:
Data distribution is well within the LSL and USL

Diagram of typical measurement response

Abbreviations:
UCL = Upper Control Limit
LCL = Lower Control Limit

Abbreviations:
USL = Upper Spec Limit
LSL = Lower Spec Limit

Examine traditional methods for evaluating tester performance

Common approach:

- Only focus on excursions of data monitoring silicon fabrication process tools
- Strategy assumes a perfectly performing test system that is independent of tool aging and degrading components

Business model:

- Typically only monitoring fab key and control process parameters

Reality:

- Simple test structures are a great indicator of test system fatigue

Opportunity:

- Parametric test engineers have a world-class metrology tool at their disposal which is capable of self evaluating its own system health

Examine Traditional Methods for Evaluating Tester Performance

Fab only approach:

- Focuses on silicon fabrication process excursions
- Engineers only monitor fab key process control parameters
  - Transistor drive current
  - Transistor off current
  - Etch structures
  - Lithographic structures
  - Polish structures
  - Inter-layer oxides
  - Capacitors
  - Contact / via chains

Discuss means of utilizing test data to self monitor system vitality

Challenges for parametric test engineers

- Increase usage of algorithms / automated scripts to analyze data
- Perform periodic deep drives into the sea of test data
- Partition test data by individual, fleet, and site-to-site tester(s)
- Specifically, data mine elementary / robust test structures
- Utilize measurement data available to validate your assumptions
- Migrate towards development of machine learning
- Seeking to achieve 24/365 coverage of parametric tester fleet
- Learn to detect measurement inaccuracies before they grow into data excursion resulting in a visit to the company president's office

Summary

- **Understanding parametric test data signature is critical**
  - Tester channel board relays are good for ten's of millions of cycles
  - However, when they reach their life-time, data signature quickly degrades
  - Therefore, monitoring basic, well behaved parametric test structures will provide a good platform for catching bad tester channels
  - Automating scripts to search through test data looking for measurement trends which produce a step function response is key to monitoring an aging fleet of parametric testers.
- **In closing, achieving a high performing test system is a function of tester health and real-time monitoring**

Thank you for your time

Questions and Answers