

# Validation of 55GHz Octal-site Wafer Test Probecard for 5G mmWave devices



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#### Overview

- Introduction 55GHz Octal-site Wafer Test Probecard for 5G mmWave devices
- Areas for Performance Improvement: Objectives, Methods, Results & Follow-On Work
  - 35  $\Omega$  Impedance Change for MB Signals
  - Probehead Probe Card Alignment
  - DOE and PCA Testing
  - More Compact Site Layout for Improved COT
- Summary and Acknowledgements

#### Validation of 55GHz Octal-site Wafer Test Probecard for 5G mmWave devices

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- In SWTest 2021, we presented a probecard for WLCSP mmWave devices\*\* with some key requirements:
  - 55GHz BW for mmWave MB signals (direct test + loopback)
  - 150um pitch, direct-attach PCB technology
  - Octal site with 600+ I/Os per site
  - Manual Test option for all eight sites
- Design evolved to meet new customer needs, improve usability and test efficiency
  - 35 Ω impedance for mmWave MB signals
  - Better probe head to probe card alignment
  - Denser multisite test pattern
- Each design change requires a different validation process

\*\* SWTest 2021, Session #1 55GHz Octal-site Wafer Test Probecard for 5G mmWave devices; Jason Mroczkowski (Cohu – USA)

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# Why Use Radial Spring Probes?

- Low and consistent cRes
- Long lifetime
- Individual replacement
- Manual Test of singulated WLCSP
- Standardized recipes for probes and cross sections at different pitch / impedance combinations



- Original probe head cross-section and PCB layout optimized for 50 Ω impedance
- 55GHz MB channels changing to 35 Ω impedance, requires:
  - New PCB layout with DUT-launch trace structures matched to 35 Ω
  - New probe head design supporting both 35 Ω and 50 Ω signal impedances
  - PCB impedance transformer from 35 Ω to 50 Ω
- Without modification, the performance will be degraded



New coupon board layout implemented with 35 Ω matching

Next step is to simulate performance and identify further optimizations required



Initial simulation results for loopback path show that only changing PCB layout creates multiple impedance discontinuities in signal chain:

DUT @  $35\Omega \rightarrow$  Probe @  $50\Omega \rightarrow$  PCB @  $35\Omega \rightarrow$ Probe @  $50\Omega \rightarrow$  DUT @  $35\Omega$ 





Performance is even worse than before starting redesign!

- Requirement: reduce impedance of probehead cross-section to match 35Ω PC trace impedance
- Possible solution: reduce gap between cViper 0.15mm pitch signal probe and ground probe(s) using larger diameter probe
- Problem: Signal pin probe and ground probe behind signal pin are at maximum diameter due to spacing, and cannot be enlarged
- Preferred Solution: Increase diameter of ground probes shown circled in red





- New wider Ground probe compares with original cViper signal / Ground probe:
  - Same 3.1mm test height and compliance range
  - Same crown tip dimensions and geometry
  - Same spring force at test height
  - Wider barrel diameter
  - Wider plunger diameter
  - Equivalent or better Cres performance





302069563 Cres vs. Cycle Count

- Simulations of RFMB Loopback with model of new cViper Ground probe show more uniform impedance match and improved Return Loss
- Minimum cViper Impedance: ~42 Ω
- Reduced stripline trace width to better match cViper impedance







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- Final addition: space transformer on PCB to return to 50 Ω at connector
- 35 Ω cViper stackup + PCB redesign for 35 Ohm was implemented and measured
- Measurements (including probe head and cables) confirm that simulated performance is achieved

S11 - DUT Side -  $35\Omega$ 

Frequency (Hz)



35Ω

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50Ω

#### **35 Ω Impedance Change for MB Signals: Next Steps**

- Customer requesting further performance enhancements
- Additional probe/cross-section changes expected to provide better than -15dB RL up to 75GHz



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# Probehead – Probe Card Alignment: Objectives and Methods

- Objective: ensure that probe head can be removed and exchanged between PCBs without requiring manual realignment process
- Methods:
  - Monte Carlo analysis of stack-up tolerances in existing design
  - Implement more robust alignment pins with reduced alignment error
  - Add fiducial features on PCB to improve drilling accuracy of alignment holes
  - Simplify assembly to reduce errors across multiple site locations





#### Probehead – Probe Card Alignment Improvement: Methods

- **1.** Holes to verify alignment with PCB fiducials
- **2.** Simplified, more robust and asymmetric alignment pins
- **3.** Single-piece Probe Retainer Plate for improved alignment consistency across all sites
- **4.** Improved tolerances in key areas affecting alignment





### **Probehead – Probe Card Alignment: Results**

- New test PCB layout created with fan-out to tester pads; allows full electrical testing using either:
  - Flying prober
  - Probe Card Analyzer (configured with 93k Probe Card Interface)
- Includes fiducial features to improve accuracy for drilling alignment holes
- DOE process used to verify interchangeability of multiple PCBs and probe heads
- Zeiss visual inspection used to verify accuracy of feature placement



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#### **Probehead – Probe Card Alignment: Results**

- Measurement of pad locations vs. alignment hole locations shows X-Y offset resulting from incorrect drilling process
- Distribution of pad locations is within required tolerances
- Correcting drill offset issue results in expected alignment on all pads



# **Probecard Analyzer (PCA) Implementation**

- ITC Probilt with custom PCI for mmWave probe card design
- Provides full Probecard testing coverage prior to shipment
- Probecards evaluated on PCA and correlated to internal probehead testing
- 90% reduction in test time for targeting accuracy, contact resistance and planarity measurements





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#### **Probehead Layout: Objective**

- Original Probehead layout created was 1x8 with 3 skipped die between sites
  - Required for routing of RF direct connection and loopback paths
- Problem: reduced touchdown efficiency at edge of wafer
- Goal: production-optimized layout 1x8 with 1 skipped die
  - Simplified layout required
  - Benefit of improved touchdown efficiency and lower COT





29 die  $\rightarrow$  15 die span = 48% shorter

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#### **Probehead Layout: Methods**

- Agreed simplified schematic and performance goals with customer, e.g. minimize losses on IF receive path
- New probehead layout optimized to meet bowing requirements
- PCB layout feasibility study confirmed routing for key RF signals can be accommodated within new DUT spacing and probehead constraints
- Overall, 1x8 with 1-skipped die implementation looks possible!



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#### **Probehead Layout: Results (1)**

 Initial Bowing Analysis confirmed Max Y directional deformation 65 µm: goal is <50µm</li>



Design uses 1-piece ceramic body across all sites and stainless steel frame

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#### **Probehead Layout: Results (2)**

 Bowing Analysis after initial redesign to add strengthening ribs: Max Y directional deformation 67 µm, 54 µm at body



Additional SS support structures between DUT sites

#### **Probehead Layout: Results (3)**

 Bowing Analysis after further redesign: Max Y directional deformation 52 µm, 40 µm at body



#### **Probehead Layout: Follow-On Work**

- Complete signal routing for all 8 sites
- Tune spacing between loop-back structures and probehead attachment features
- Design shorter RF cables to meet IF loss budget
- Routing and component placement for 16-site layout



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# Summary

- Initial mmWave probe card design has been deployed and successfully used
- Design has evolved to meet new customer needs, improve usability and test efficiency
  - 35  $\Omega$  impedance for mmWave MB signals
  - Better probe head to probe card alignment
  - Denser multisite test pattern
- Each enhancement requires specific validation activities
- Additional design improvements are ongoing to further improve RF performance
- Thanks to all the Cohu and Synergie-CAD team members for their significant contributions to this project!